APPLICATIONS INFORMATION

CALIBRATED PERFORMANCE

Each ADXRS450 gyroscope uses internal EEPROM memory to store its temperature calibration information. The calibration information is encoded into the device during factory test. The calibration data is used to perform offset, gain, and self-test corrections over temperature. By storing this information internally, it removes the burden from the customer of performing system level temperature calibration.

MECHANICAL CONSIDERATIONS FOR MOUNTING

Mount the ADXRS450 in a location close to a hard mounting point of the PCB to the case. Mounting the ADXRS450 at an unsupported PCB location (that is, at the end of a lever, or in the middle of a trampoline), as shown in Figure 20, can result in apparent measurement errors because the gyroscope is subject to the resonant vibration of the PCB. Locating the gyroscope near a hard mounting point helps to ensure that any PCB resonances at the gyroscope are above the frequency at which harmful aliasing with the internal electronics can occur. To ensure that aliased signals do not couple into the baseband measurement range, design the module wherein the first system level resonance occurs at a frequency higher than 800 Hz.

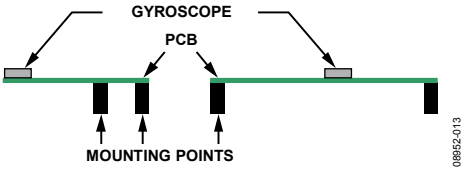

Figure 20. Incorrectly Placed Gyroscope

APPLICATIONS CIRCUITS

Figure 21 and Figure 22 show the recommended application circuits for the ADXRS450 gyroscope. These application circuits provide a connection reference for the available package types. Note that DV_{DD}, AV_{DD}, and P_{DD} are individually connected to ground through 1 µF capacitors; do not connect these supplies together. Additionally, an external diode and inductor must be connected for proper operation of the internal shunt regulator. These components (listed in Table 6) allow for the internal resonator drive voltage to reach its required level, as listed in the Specifications section.

Table 6. Internal Shunt Regulator Components

Component	Qty.	Description
Inductor	1	470 µH
Diode	1	>24 V breakdown voltage
Capacitor	3	1 µF
Capacitor	1	100 nF

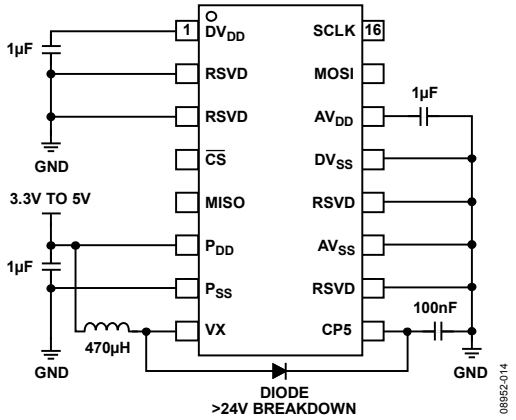

Figure 21. Recommended Applications Circuit, SOIC_CAV Package

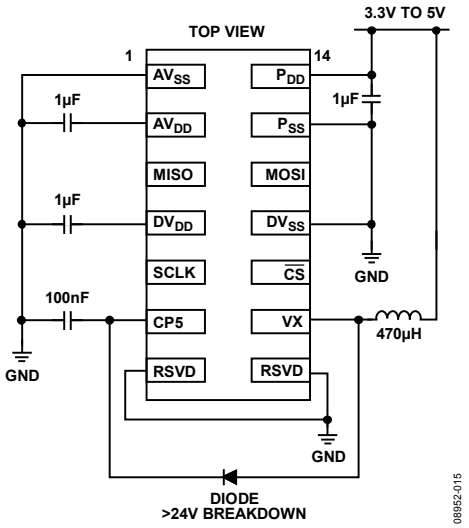

Figure 22. Recommended Applications Circuit, Ceramic LCC_V Package

ADXRS450 SIGNAL CHAIN TIMING

The ADXRS450 primary signal chain is shown in Figure 23; it is the series of necessary functional circuit blocks through which the rate data is generated and processed. This sequence of electromechanical elements determines how quickly the device is capable of translating an external rate input stimulus into an SPI word to be sent to the master device. The group delay, which is a function of the filter characteristic, is the time required for the output of the low-pass filter to be within 10% of the external rate input, and is seen to be ~4 ms. Additional delay can be observed due to the timing of SPI transactions and the population of the rate data into the internal device registers. Figure 23 anatomizes this delay, wherein the delay through each element of the signal chain is presented.