Table 3-18 below represents the 3-Tier scenario and the different placement courtyard sizes.

Table 3-18: Ball Grid Array Density Levels

Lead Part	Minimum (Least) Density Level C	Median (Nominal) Density Level B	Maximum (Most) Density Level A
Periphery Collapsing Ball	15% reduction below nominal ball diameter	20% reduction below nominal ball diameter	25% reduction below nominal ball diameter
Periphery Noncollapsing Ball or Column	5% increase above the nominal ball or column diameter	10% increase above the nominal ball or column diameter	15% increase above the nominal ball or column diameter
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.50	1.00	2.00
Ball Grid Array **(BGA)** Construction and land pattern development are described in 14.1 & 14.4			
Column Grid Array **(CGA)** Construction and land pattern development are described in 14.1.3 & 14.4			

The anatomy of the “Metric Via” is based on the 0.05mm universal grid for PCB design layout. The features of the metric via should always be sized in 0.05 increments –

- Pad Size
- Hole Size
- Solder Mask Size
- Plane Clearance (Anti-pad) Size
- Plane Thermal Relief ID and OD Size

The chart in Table 1 represents common via padstack feature sizes for various pitch BGA components.

Table 1: Common Via Padstacks

BGA Pin Pitch	VIA Name	Land Diameter	Finished Hole Dia	Plane Clearance	Solder Mask	Thermal ID	Thermal OD	Thermal Spoke Width
1.50 mm	VIA60-25-80	0.60	0.25	0.80	0.00	0.55	0.80	0.25 or None
1.50 mm	VIA55-25-75	0.55	0.25	0.75	0.00	0.55	0.75	0.25 or None
1.27 mm	VIA63-30-85	0.635	0.30	0.85	0.00	0.65	0.85	0.25 or None
1.00 mm	VIA55-25-75	0.55	0.25	0.75	0.00	0.55	0.75	0.25 or None
1.00 mm	VIA50-25-70	0.50	0.25	0.70	0.00	0.55	0.70	0.25 or None
0.80 mm	VIA45-20-65	0.45	0.20	0.65	0.00	0.50	0.65	0.20 or None
0.75 mm	VIA40-20-65	0.40	0.20	0.65	0.00	0.50	0.65	0.20 or None