Understanding Interleaved Boundary Conduction Mode PFC Converters

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Abstract—Boundary conduction mode power factor correction circuits are widely used in lower-power off-line power supplies. Their application at higher power levels is less practical due to the high amplitude of inductor ripple current, which is a significant source of power dissipation in the converter's boost inductor and power switch, placing a burden on the EMI filter size. Interleaving two of these boundary conduction mode converters mitigates the input filter problem and, to a certain extent, the high RMS currents carried by the semiconductor devices. Interleaved BCM PFC circuits are becoming popular in the industry. This paper analyzes the advantages of such solutions, highlights critical design issues related to power factor correction in general and to the specific requirements, and discusses potential solutions to control an interleaved boundary conduction mode power factor corrector.

I. INTRODUCTION

Boundary conduction mode (BCM) power factor correctors (PFC) have long been used for up to about 300W AC/DC supplies and lighting ballasts. At higher power levels, the continuous conduction mode boost is more appealing due to its lower ripple currents, consequent lower peak currents, and lower differential mode EMI. While the continuous conduction mode boost has all these benefits, it has many drawbacks as well. For example, the output rectifier is hard switched, leading to a large power loss and also a significant common-mode EMI signature. Expensive Silicon-Carbide diodes are sometimes used to speed up the reverse recovery, which reduces the EMI and increases efficiency.

In contrast, BCM mode power factor correctors switch the MOSFET on with zero current in the diode, offering a zero current switched (ZCS) turn-on, and inexpensive silicon rectifiers may be used. The trade off for ZCS and an inexpensive power stage is a variable switching frequency, as well as higher peak currents. One solution is to combine the best attributes of both topologies – to use an interleaved BCM converter. The interleaved BCM converter is made of two identical BCM converters, their operation phase shifted by 180º. The resulting converter has all the benefits of a single BCM converter, but reduces the peak currents by dividing the total output power, and therefore the inductor currents, between two phases.

II. BCM PFC CONVERTER PROPERTIES

A. Power Factor Correction Control Technique

A boundary conduction mode boost power factor converter is shown in Figure 1. The power stage topology is identical to any boost converter, with the addition of a zero current sense winding on the inductor. This winding allows the control circuit to detect when the boost inductor current has reached zero and a new switching cycle should be started.

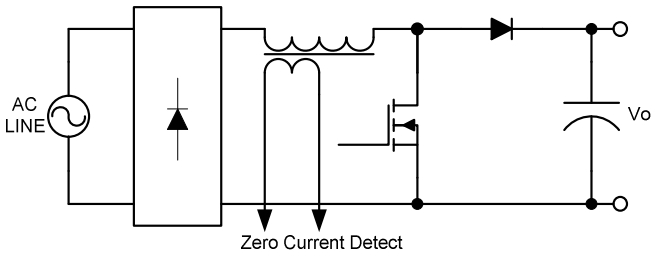

Fig. 1. Boundary Conduction Mode Boost PFC showing the sense winding on inductor.

To achieve near unity power factor correction with a BCM boost converter, a constant on-time control law is used. With constant on-time control, the MOSFET on-time is kept constant over an entire line cycle. Because the MOSFET is turned on with near zero current, the peak inductor current becomes proportional to the line voltage. Recognizing that the inductor current is triangular, the average value is also proportional to the peak, and thus the line voltage and unity power factor is achieved.

Figure 2 shows the gate voltage and inductor current waveforms for a BCM boost converter over a half line cycle. In this figure, the switching frequency has been made artificially low in order to show the wave shapes and frequency variation during a line cycle.

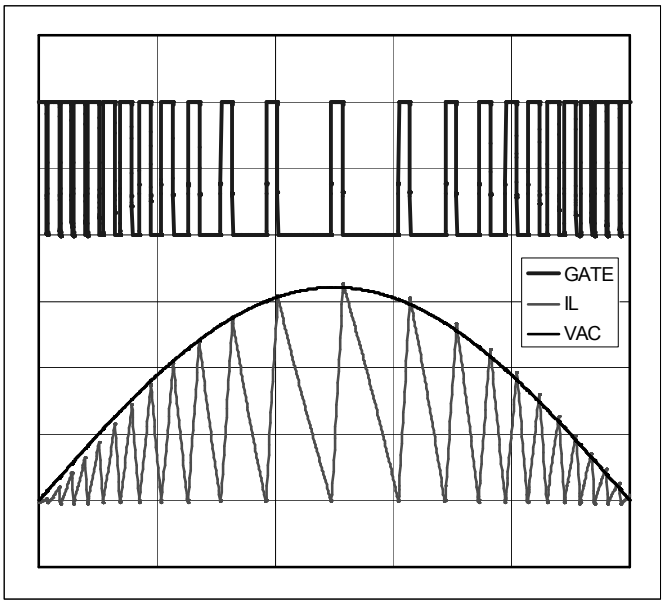

Fig. 2. BCM converter waveforms normalized to a half-line cycle: MOSFET gate voltage, inductor current, and AC line voltage.

B. Frequency Variation with AC Line Voltage, Output Power

The switching period of a continuous conduction mode boost converter is divided into two time intervals, on-time and off-time. The boundary conduction mode boost converter adds a third, often ignored but significant, time interval after the diode conduction time. This time interval is defined by the resonant frequency of the boost inductor and the parasitic capacitance on the switching node. Figure 3 shows the three distinct time intervals: on-time, off-time, and resonant time.

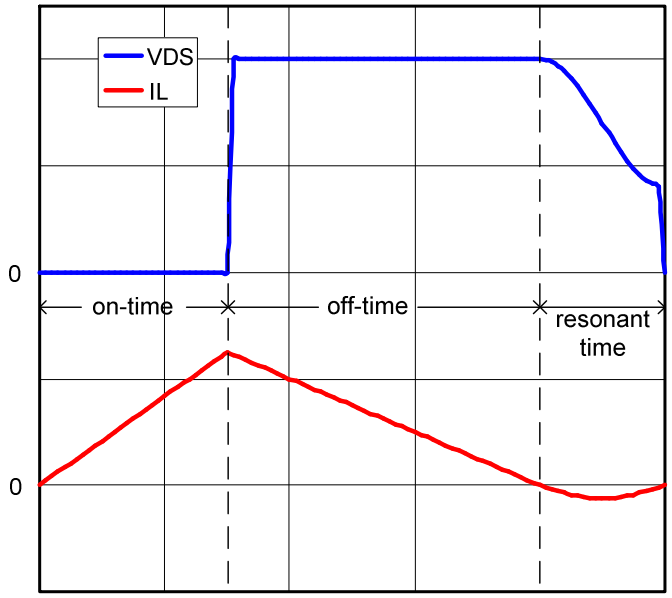

Fig. 3. MOSFET drain-to-source voltage and inductor current in BCM boost converter during a single switching cycle.

Although the on-time is held constant over a line cycle, the off-time varies with the instantaneous line voltage. When the MOSFET is switched off, the inductor current decays at a rate determined by the difference between the instantaneous output and input voltages. When the input voltage is at the peak of the line, the difference between the input and output voltages is smaller, giving a shallower down-slope to the inductor current and a longer off-time. This results in a much lower switching frequency at the peak of the AC line.

At the end of the off-time, the inductor current reaches zero and the boost diode becomes reverse biased. This natural commutation is a huge advantage to the BCM topology, as it allows inexpensive silicon diodes to be used. After the inductor current reaches zero, the converter enters into a resonant time interval during which the boost inductor resonates with the combined capacitance on the switching node. The driving voltage for this resonant tank is the difference between the output and instantaneous input voltage. When the input voltage is more than half of the output voltage, the switching node freely resonates about the input voltage, without the body diode of the boost MOSFET transistor ever clamping the resonant waveform. Because the voltage across the MOSFET is non-zero when the MOSFET is turned on, the capacitive energy is shunted to ground, increasing power dissipation in the MOSFET. To minimize this loss, the MOSFET should be switched on at the valley of the drain-to-source voltage. Since the valley in the resonant voltage occurs half a resonant cycle after the inductor current reaches zero, this time must be accounted for in the switching frequency calculation.

Using a sum of the on-time, off-time, and half the resonant period, a relationship between the switching period and the instantaneous input voltage can be found. The on time, t_{ON}, is found by equating input power to output power:

$$t_{ON} = \frac{2 \cdot L \cdot P_{OUT}}{\eta \cdot V^2_{IN,RMS}} \quad (1)$$

where:

P_{OUT} is the output power per phase (W),
L is the inductance of the phase inductor (H),
$V_{IN,RMS}$ is the RMS input voltage (V),
η is the power supply efficiency.

The off-time t_{OFF} is proportional to the on time:

$$t_{OFF} = \frac{V_{IN}(t)}{V_{OUT} - V_{IN}(t)} \cdot t_{ON} \quad (2)$$

where V_{OUT} is the output voltage. The resonant time is:

$$t_{HALF-RES} = \pi \sqrt{L \cdot C}_{RES} \quad (3)$$

where C_{RES} is the total resonant capacitance on the switching node. This capacitance includes the C_{OSS} of the MOSFET, junction capacitance of the boost diode, and parasitic winding capacitance of the inductor.

The switching period therefore is:

$$t_{SW} = t_{ON} + t_{OFF} + t_{HALF-RES} = \frac{V_{OUT}}{V_{OUT} - V_{IN}(t)} \cdot \frac{2 \cdot L \cdot P_{OUT}}{\eta \cdot V^2_{IN,RMS}} + \pi\sqrt{L \cdot C_{RES}} \quad (4)$$

This relationship between switching frequency and input voltage shows the same trend independent of power being transferred, with the maximum frequency at the zero crossings of the line and the minimum frequency at the peak of the line. Figure 4 shows the typical frequency deviation during a half-line cycle as a percentage of designed power, 50%, 75% and 100%.

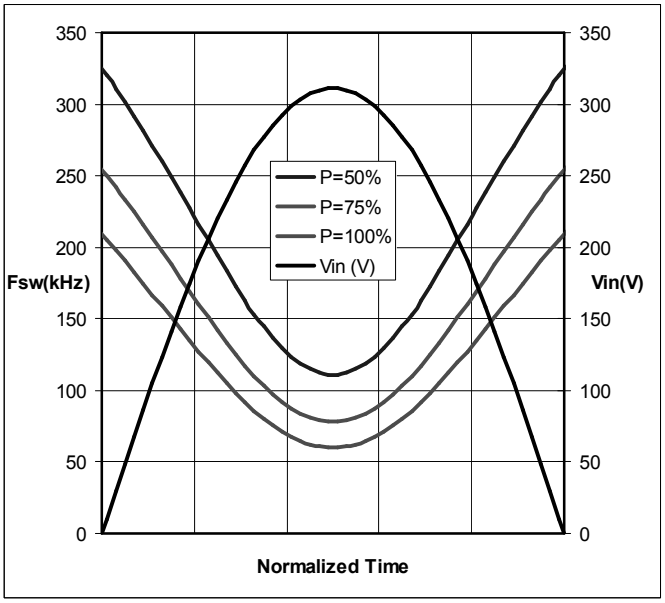

Fig. 4. Switching frequency vs. instantaneous input voltage for three power levels. Line voltage=220V RMS, output voltage=400V, L=390µH, resonant frequency=360kHz. Full output power is designed to be 200W.

A typical universal input PFC operates over a wide input voltage range, typically 85V to 265V RMS. Therefore, also look at how the minimum frequency of the converter changes over the entire input range. In Figure 5, the minimum switching frequency, which occurs at the peak of the line, is shown vs. the RMS input voltage for three output voltages. It is interesting to note that, depending on where the output voltage is set, the minimum switching frequency may occur at the minimum or at the maximum line voltage. The output set-point is particularly important for BCM converters, as setting the output voltage too low could prevent detection of zero current. When the output voltage is approximately 405V, the minimum switching frequency is the same for both low line ($85V_{AC}$) and high line ($265V_{AC}$).

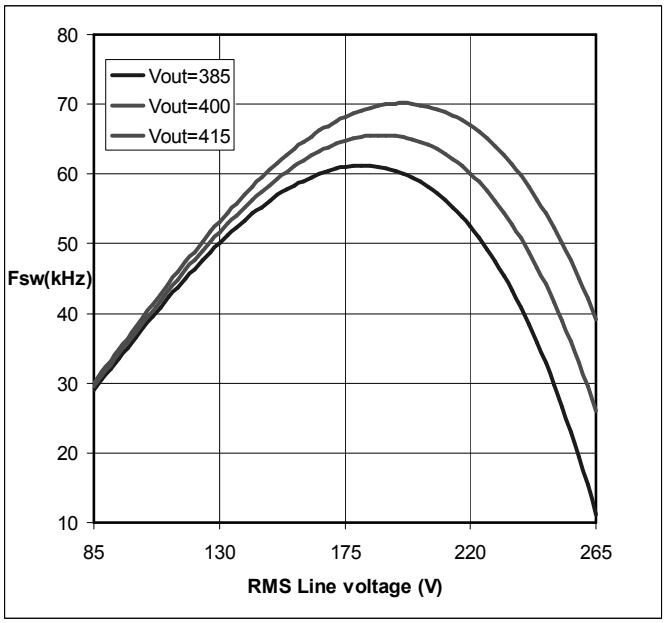

Fig. 5. Minimum switching frequency vs. RMS line voltage. L=390µH, resonant frequency=360kHz, P_{OUT}=200W.

With the variation of frequency over a switching cycle understood, how does the switching frequency vary with output power? This relationship is easy to understand by doubling the on-time and figuring the change in output power and switching period. In a BCM converter, the inductor stores a packet of energy during the MOSFET on-time and, during the off-time, this energy is then transferred to the output. Because the energy stored in the inductor is zero at the end of a switching period, all of the stored energy is transferred each switching cycle, making power transferred proportional to the switching frequency. With a constant on-time control law, the inductor current reaches a peak proportional to the input voltage. If the on-time is doubled, the peak current is doubled, and the energy stored in the inductor increases by a factor of four. At the same time, doubling the on-time also doubles the off-time; only the resonant frequency is constant. If the resonant time is ignored, doubling the on-time would halve the switching frequency, and therefore halve the power transferred. Although the inductor is storing four times the energy, output power is the product of energy times switching frequency. This means that doubling the on-time doubles the output power and halves the switching frequency. Because the switching period includes a half resonant period largely independent of on-time, the true switching period doesn't increase exactly in proportion to on-time. This error is quite small, but is included in Figure 6, which shows the relationship between output power, MOSFET on-time, and switching frequency.

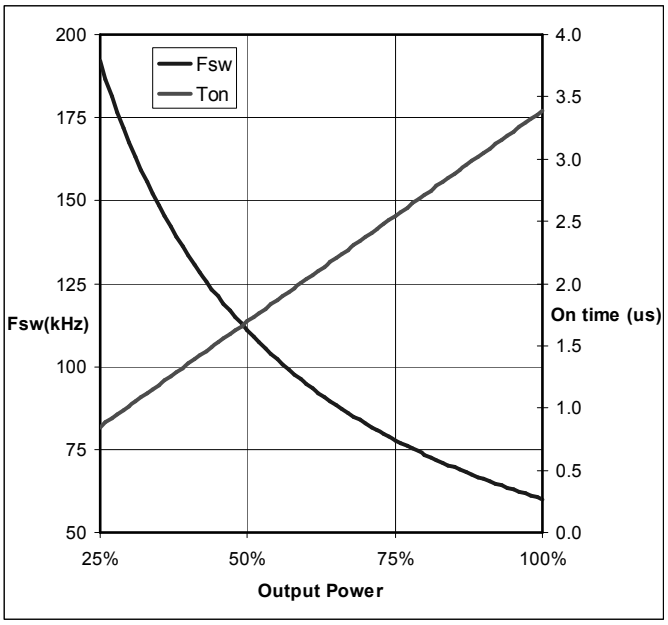

Fig. 6. Minimum switching frequency vs. output power. Line voltage=220V_{RMS}, output voltage=400V, L=390µH, resonant frequency=360kHz.

C. Second-Order Effects on Switching Frequency

When the input voltage is below half the output voltage, the switching node resonates from the output voltage until the MOSFET body diode clamps at ground. After the diode starts conducting, current is flowing backwards, i.e. source to drain, in the MOSFET body diode. Once the body diode starts conducting, the control IC interprets the change in the winding voltage as a valley in the normal resonant waveform, and starts an on-time cycle. The first portion of the on-time is essentially un-used to build inductor current, as the current is already flowing through the body diode and is increasing towards zero at the rate of V_{IN}/L. Because the control law is constant on-time and assumes zero inductor current at turn-on, the resulting peak inductor current is less than predicted. While the control loop corrects this by increasing on-time to maintain the same output power, the resulting frequency is lower than that predicted in Figure 4. This effect is especially noticeable around zero crossings, where the input voltage is nearly zero. An ideal control circuit is able to detect when the MOSFET body diode is conducting and not start an on-time period until the current has reached zero.

At low output power, the converter is switching with short on-times and, consequently, a low peak inductor current. When the MOSFET is first switched off, this peak inductor current goes to charging the resonant capacitance on the switching node. At some input voltage level, the energy stored in the inductor drops to a point where there is not enough energy stored to drive the resonant capacitor to the output voltage. At this critical input voltage level and below, the converter is not able to transfer any power to the output and all power factor correction is lost. The off-time is zero during this operating mode and, therefore, the switching period is made up of on-time and resonant time. Since at very low output power, the on-time is nearly zero; the switching frequency is only limited by the half resonant frequency of the converter. A good IC controller limits the maximum frequency allowed with a frequency clamp. During operation in the frequency clamp, the converter is operating in discontinuous conduction mode.

III. PARALLELING CONVERTERS

To increase the power capability of any converter, one possibility is to parallel two or more converter stages. The BCM boost converter topology is particularly suitable as the load sharing is inherent to the control technique and the conduction and switching losses are spread over two power stages. This increases the overall efficiency of the power train over using a single converter designed for twice the power.

A. Load Sharing, Conduction, and Switching Losses

When two smaller converters are paralleled to supply the same output power as a single converter, the individual power stages ideally carry half the current of the single converter. Since the RMS currents are proportional to the peak currents, the MOSFET, inductor, and diode RMS currents are half the value of those in the single converter. The prudent design would take the single MOSFET and divide it into two devices with twice the $R_{DS(ON)}$, the two inductors would have twice the DC resistance, and so on. In each of the paralleled converter power stages, the conduction losses, which are proportional to the RMS current squared, would be half that of the single converter. Additionally, these losses would be spread over twice as many devices, spreading the dissipated power and easing the thermal management of the design.

The assumption that the two converters share equal power is based on current being shared equally between the two power stages. In the BCM converter, this is simple to accomplish by controlling equal on-time for the two power stages. The power processed by each phase in the paralleled converter is dependent only on the inductor tolerance. In this case, the power sharing is proportional to the inductor mismatch.

When paralleling converters, the inductor used in a single converter is divided into two inductors. The next decision to be made is what minimum frequency is going to be used for each phase. The usual requirement is to avoid frequencies in the audible range, so each phase inductor must operate above the audible range of approximately 15-20kHz. Designed to this requirement, the inductors in the paralleled converter operate at one-half the peak current, but have twice the inductance of the single converter's inductor. Since the size of an inductor is largely proportional to the inductance times the square of the peak current, the parallel converter inductors are half the size of a single inductor.

As with the conduction losses, the switching losses theoretically divide equally between the two power stages. However, a practical advantage is gained by having two gate drivers driving two individual MOSFETs. By dividing the

MOSFET die area into two packages, as well has having the two discrete drivers, the turn-off times can be reduced by lowering the parasitic resistances in the gate drive loop. As the turn-off switching losses are proportional to the turn-off time, reducing the turn-off time reduces turn-off switching losses proportionately.

IV. Interleaving Converters

The primary drawback of paralleling converters is that the frequencies of the two converters are not identical. While the converters switch at frequencies very close to each other, any small parametric differences lead to a frequency difference called a "beat" frequency. This beat frequency appears in the input and output currents. For example, at times, the peak inductor currents would line up in phase, doubling the peak current seen at the EMI filter. By synchronizing the two converters phase shifted by 180º, the high-frequency ripple currents cancel and the EMI filter requirements of the converter are reduced.

When two converters are synchronized and interleaved, filtering the differential mode EMI at the input becomes much easier. When interleaved, the effective switching frequency seen at the input side of the converter doubles, while the peak current is theoretically halved. This reduction in the peak current varies over the line cycle, at the point when the duty cycle is equal to 50%, almost perfect ripple current cancellation is achieved, and the input current is DC. This point is at $V_{IN}=V_{OUT}/2$, which only occurs when operating at higher inputs, $220/240V_{AC}$. Since the primary EMI problem with the BCM converter is differential mode, interleaving yields great benefits on EMI filter size reduction.

V. Design Considerations

While the single BCM converter design is well understood, when two converters are interleaved, many design challenges arise. For the interleaved converter to function at its maximum potential, exact control of the two power stages should be exercised. This section details and explores the different control techniques used in control of interleaved BCM converters.

A. Zero-Crossing Detection

After a switching cycle is complete, the control IC must be able to detect when the inductor current decays to zero. This event is called zero crossing detection (ZCD) and uses a sense winding on the power inductor. While there are several ways of processing this information, all circuits need this winding for ZCD.

The simplest method of detecting a zero crossing uses a comparator threshold on the ZCD waveform. When the inductor current decays to zero, the diode turns off and the voltage across the sense winding voltage starts to decrease from its maximum. When the winding voltage reaches zero, the controller starts an on-time. The problem with this technique can be seen in Figure 7.

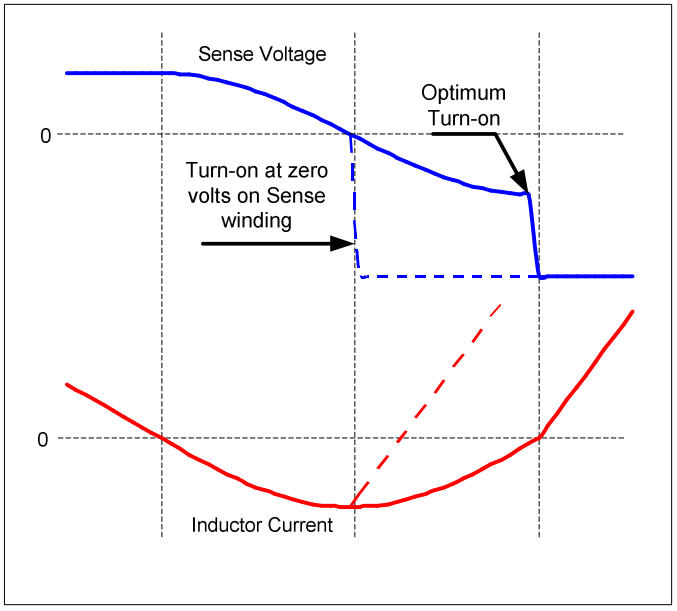

Fig. 7. Detailed sense winding voltage and inductor current showing optimal turn-on point.

When the voltage across the inductor is zero, the inductor current is actually at its maximum negative value. If the MOSFET turns on at this time, all the energy stored in the parasitic capacitance would be shunted to ground, resulting in power loss. If the turn-on can be delayed until the valley of the drain-to-source voltage, the minimum energy is dissipated and the maximum efficiency achieved.

An incremental improvement in efficiency can be made by adding a small R-C delay between the sense winding and the control IC. This delay can be tuned to align the turn-on of the MOSFET to the valley of the drain waveform. In this way, the MOSFET is turned on at a valley in the drain-to-source voltage, and optimum efficiency is achieved. Since this delay is tuned for the particular resonant frequency, any change in the power stage inductance or resonant capacitor and any timing error caused by the tolerance of the R-C network would result is sub-optimum efficiency.

Ideal results can be achieved when a true valley detection circuit eliminates the need for an external R-C delay. Instead of detecting a simple voltage level, the circuit senses a change in the slope of the sense voltage. First, the sense voltage is turned into a current by placing a resistor in series with it. Since the ZCD pin voltage is clamped to ground, the current can be thought of as a direct representation of the sense winding voltage. The peak of this current is detected internally; this corresponds to the valley of the drain-to-source waveform. At this instant, the MOSFET is switched on and the next switching cycle starts.

B. Output Voltage Selection

In Figure 5, the minimum switching frequency vs. RMS line voltage was shown and the significance of output voltage discussed. From this figure, the optimum output voltage is approximately 405V; this is the voltage at which the minimum switching frequency is the same for both high and low line voltages. There are other important reasons not to design the converter with a lower output voltage. In the BCM converter, the controller IC detects when the inductor current reaches zero by a sense winding on the power inductor. The voltage developed on this inductor winding is:

$$V_{SENSE} = \frac{N_{sense}}{N_P} \cdot (V_{OUT} - V_{IN}) \quad (5)$$

Therefore, the minimum sense voltage occurs at high AC line and the lowest output voltage. Typically there is some zero-crossing voltage threshold on the control IC that must be passed to start a new switching cycle. If the output voltage is programmed too low, this threshold might never be reached and the converter stops switching. If this occurs, all power transfer stops until the control IC enters restart timer mode and the input line voltage drops to a level where a valid zero-cross threshold is reached. Of course, power factor correction is lost and severe input line current distortion is present.

Note that, from Equation 5, the turns ratio can be adjusted to allow a design with a lower output voltage. While this is true, the resulting lower turns ratio presents a much wider voltage range to the control IC and the IC would have to operate over a larger dynamic range. All these considerations point to designing the converter with an output voltage set-point of at least 400V.

C. Limiting the Switching Frequency, Restart Timer

One of the first problems encountered with the BCM converter topology is how to limit the switching frequency. If care isn't taken, the converter can operate at frequencies low enough to drop into the audible range. Once any switching converter enters the audible frequency range, the magnetic components vibrate and emit undesirable audible noise. On the other end of the frequency scale, at low output power levels, the switching frequency increases to an undesirably high value, increasing switching and gate charge losses. Clearly some means must be used to limit the switching frequency under all operating conditions. This can be accomplished using internal timers. For instance, the maximum frequency can be limited to 500kHz and, if no zero current condition is detected, the restart timer retries at a rate of about 17kHz, staying above the audible frequency range. Note that both the frequency clamp and the restart timer are engaged only when the converter operates under unusual operating conditions. They are considered protection functions. While they are operational, power factor correction might not be possible and the line current might not follow the input voltage waveform.

The restart timer, and synchronization while operating in the restart timer mode, is critical to the operation of the BCM converter. For example, without the restart timer, the converter would never start switching. When operating in the restart timer mode, the peak current conducted in each phase is at its maximum, making perfect synchronization mandatory.

D. Synchronization, Matching On-time

The synchronization of the two converter stages is one of the most critical features of the control IC. While several methods can provide synchronization of interleaved converters, most are designed for fixed-frequency operation. The wide switching frequency range of the BCM converter requires careful consideration as to the method employed. Additionally, the two converters are constantly changing frequency as the input line voltage changes, so the synchronization loop must have reasonable bandwidth. Finally, the synchronization loop must be immune to switching noise and be robust in the noisy environment of a switching power supply.

The only synchronization technique found suitable is one that continuously measures the natural frequency of the two converter power stages, then generates phase-shifted synchronization pulses. In this manner, the period of each converter is measured and compared against the other channel's period and the channel with the lower measured frequency becomes the master. This "master" channel is then the time base to which the other channel is synchronized. Because the control circuit continuously measures the period of each channel, the master is determined every cycle, is transparent to the designer, and is totally autonomous. There is no need for a designated master or slave power stage as the control circuit determines this automatically. The dynamic range of the circuit is limited only by the implementation – that is, how long of a switching period can be measured. Since the design requires both a restart timer and a frequency clamp, the dynamic range is well defined and the circuit implementation is straightforward. As the previous switching period becomes the basis for the phase shifted synchronization signal, the control loop is quite fast, limited only by the switching frequency. Noise immunity is guaranteed because the circuit is measuring the switching period –the time duration between the start of an on-time and the arrival of the zero-cross signal.

Matching the on-time of the two converters is another critical function of the control IC. Small imbalances in the on-times quickly create large differences in both current balancing and switching frequency. Assuming the two phases have identical inductors, the load sharing between the two phases is directly proportional to the percentage mismatch in on-time. As a first order approximation, the switching period is proportional to the on-time. Suppose the on-time of one converter is longer by a small amount, say 3%. This phase has a period that is also 3% longer, meaning that the frequency is also lower by that percentage. It is easy to see why these two converters are difficult to synchronize.

E. Improved Charging Method for the Bias Capacitor

In many PFC converters, the IC is first started by charging its bias capacitor via a resistor from the rectified AC line or the boost output voltage. Once switching operation has commenced, a bootstrap winding on the PFC inductor or downstream converter takes over and supplies the current needed to power the IC and to switch the gates of the power MOSFETs. Once the converter is switching, the startup resistor continues to dissipate power, as the resistor is continuously in the circuit. While there are ways to switch the resistor out of the circuit after the controller comes alive, these all require a high voltage (>400V) semiconductor switch to switch out the startup resistor. Furthermore, this switch is floating on top of the IC's supply voltage, making its control a difficult proposition.

Power to the IC can be provided without a dedicated startup resistor. In the boost PFC topology, the output voltage is pre-charged to the peak line voltage by the boost diode. As soon as voltage is present at the output of the boost converter, current starts to flow through the feedback resistors from the boost output to GND. Using an external, low-voltage MOSFET in series with the lower resistor in the feedback divider, this current can be diverted to charge the V_{CC} bypass capacitor of the controller. The upper resistor becomes a current source used to charge the V_{CC} capacitor. To accomplish this, a switch internal to the IC connects the VCC and FB pins. As the V_{CC} voltage rises past the under-voltage lockout threshold, the 5V reference is turned on, which drives the external MOSFET gate and shorts the resistor divider to ground. At the same time, the switch connecting the FB pin to the V_{CC} bias is switched off and the FB pin reverts to its normal role of output voltage sensing. If, for whatever reason, the bias to the IC drops below the under-voltage lockout level, the startup process is repeated. A simplified circuit implementation for this startup method is shown in Figure 8.

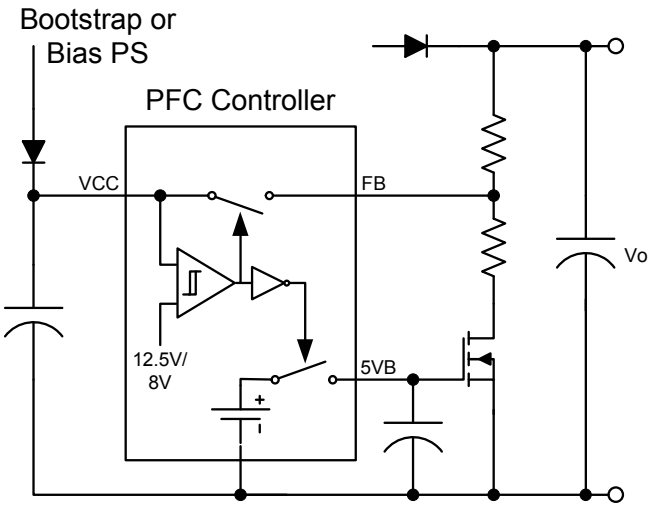

Fig. 8. Simplified start-up circuit using the output feedback resistors to provide a start-up charging current.

F. Sensing the Line Voltage, Voltage Feed Forward

A well-known problem in boost mode power factor correctors is that the voltage control loop is dependent on the input voltage. In particular, in boundary conduction mode power factor correctors using constant on-time control (i.e. voltage mode control) the output power is proportional to the square of the input RMS voltage:

$$P_{OUT} \cong \eta \cdot \frac{V_{IN,RMS}^2}{2 \cdot L} \cdot t_{ON} = \eta \cdot \frac{V_{IN,RMS}^2}{2 \cdot L} \cdot K \cdot V_{ERROR} \qquad (6)$$

where η is the efficiency of the power conversion, t_{ON} is the conduction time of the boost switch, V_{ERROR} is the output of the voltage error amplifier, and K is a proportionality factor (V/μs). Because of this dependency, as the RMS value of the input voltage changes, the error amplifier also must change to regulate the output voltage. This is particularly noticeable at lower line voltages and a circuit to feed-forward the line voltage is required to eliminate this dependency.

To overcome this issue, the input voltage is usually fed into an analog multiplier-divider circuit to generate a current reference signal inversely proportional to the square of the RMS input voltage. Analog multipliers have had problems when all the variables in semiconductor process, temperature drift, and offset are considered.

Based on Equation 6, another potential solution presents itself where the proportionality factor K can be made inversely proportional to the RMS input voltage. The on-time then becomes inversely proportional to the input voltage squared:

$$t_{ON} = K \cdot V_{ERROR} = \frac{K'}{V_{IN,PEAK}^2} \cdot V_{ERROR} \qquad (7)$$

Consequently, the output power of the converter would be independent of the input voltage. This proportionality opens the window for more sophisticated control of the supply, as the output of the error amplifier is now proportional to the output power of the converter.

G. Phase Control - Turning Off One Phase at Low Power

Once the decision has been made to interleave the two power stages, it becomes advantageous to switch one power stage off at lower power levels; this reduces power dissipation, primarily by reducing gate and switching losses. As the output power level decreases, the question is: at what power level to shed the second phase and operate a single phase? It is assumed the individual power stages would be designed for no more than half the total output power, so the phase shedding level would have to be below 50% of the maximum output power. On the other hand, regulatory guidelines mandate minimum efficiency levels at a fraction of the nominal output power, usually 25%. The phase should be shed before the output power decreases to the 25% power level to take advantage of the higher efficiency obtained by the single phase operation at these lower power levels.

When the error amplifier output is made proportional to the output power of the converter, the error signal is compared to fixed thresholds comparators. Appropriately chosen voltage levels can program the phase-shed threshold to 30%, and the phase-add threshold to 40% of total output power. The wide hysteresis is desired to prevent "chattering" when close to the power level thresholds.

A further detail about the phase shedding and adding process is changing the gain of the on-time modulator shown in Equation 7. If a phase is dropped without changing the gain, the error amplifier goes through a large signal transient because the on-time needs to be doubled since the power processed by the remaining phase doubles. Therefore, a circuit that can double the on-time instantaneously when the phase is shed and halve it when the phase is added, can ensure the error amplifier output remains constant through both transitions.

When the phase is shed, no changes to the synchronization circuitry are needed. However; when the phase is added, the on-time of the single channel needs to be halved. This nearly doubles that channel's switching frequency. To cope with this transient, the synchronization circuit must have a wide bandwidth and it might be necessary to add additional circuitry to ensure a smooth transition.

The circuit first changes the on-time, then measures the new, higher frequency switching period before adding the second phase, 180º phase shifted. This method provides a smooth transition from single-phase to two-phase operation, with no large spikes in the input current and perfect phase alignment between the interleaved power stages.

Figure 9 shows the two gate waveforms as well as the inductor phase currents when the phase is added.

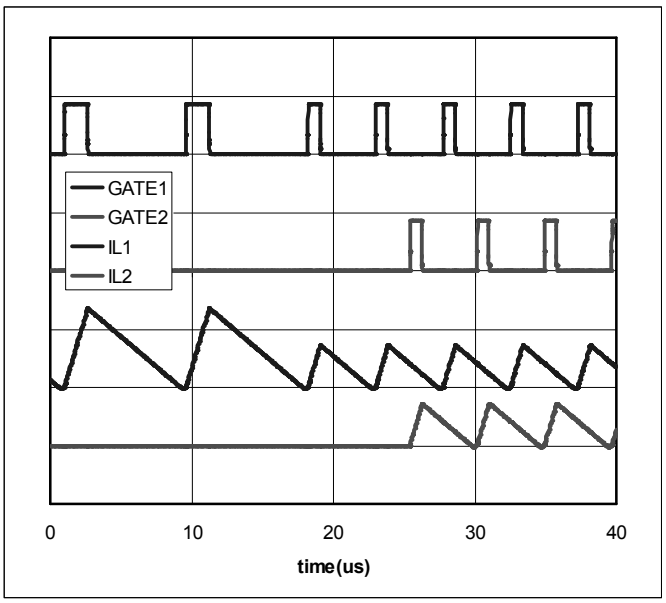

Fig. 9 Phase adding waveforms. Note the change in switching frequency and perfect synchronization when the second phase is started.

H. Soft-Start Considerations

The soft-start of any PFC converter presents a unique problem and, in this respect, the interleaved BCM PFC circuit is no different. Due to the input source, the line voltage is sinusoidal; significant energy is available only at the peaks of the line voltage and soft-start must be carefully managed to avoid saturating the inductor, entering into current limit, and to retain control of the process by the error amplifier.

When the line voltage is first applied to the boost PFC converter, the output capacitor charges near to the peak line voltage. Many conventional IC controllers use a current source fed into a large capacitor, which creates a ramp voltage that limits the converter on-time and soft starts the converter in open loop. Although this sounds like a plausible solution, in reality, while the line voltage is near the zero crossings, the soft-start capacitor continues to charge, the output voltage lags behind and the increasing difference at the inputs of the error amplifier pushes the voltage regulation loop towards saturation. A slow voltage loop, typical of the PFC designs will exhibit long recovery time which causes the output voltage to overshoot the nominal regulation voltage and often results in an over voltage shutdown.

A better way to soft-start a PFC converter is to employ closed-loop soft-start, where the reference of the error amplifier is gradually raised to the final value corresponding to the nominal output voltage and actively managed during the soft-start period to prevent the reference running away from the feedback voltage. Further improvement is achieved if the slope of the voltage reference is made a function of the error amplifier output voltage, i.e. the output power of the converter. The soft-start time is then modulated by the error amplifier output voltage, V_{ERROR}. Whenever the error signal increases above a preset threshold, indicating that the converter is close to its full power capability, the soft-start current is linearly decreased and the soft-start period prolonged. Since the charge current of the output capacitor is directly proportional to dV/dt, the resulting slower rise time of the output voltage reduces the output power the converter must deliver.

To maintain closed-loop operation for the period of startup, it is important to understand the role of current limiting while the output voltage of the converter is ramping. The problem is evident when the combined effects of the load current and the additional current needed to charge the output capacitor are considered. Assume that the converter has its current limit set at 120% of the nominal value. Starting the converter under full-load conditions seriously limits the current available to charge the output capacitor to about 20% of the nominal output current of the converter. Therefore, to ensure closed-loop operation and avoid current limiting, the output capacitor voltage should not be raised faster than the dV/dt defined by the maximum available current – not the current limit value – and the worst-case output capacitor value.

A practical implementation of an optimized startup circuit for the boost power factor converter is depicted in Figure 10.

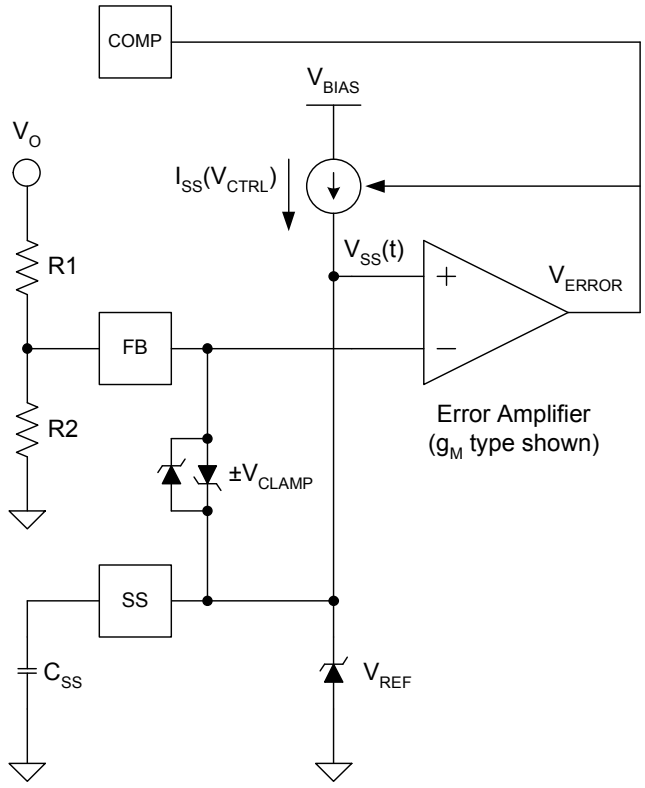

Fig. 10 Simplified schematic of the optimized PFC startup circuit.

The circuit consists of the error amplifier. Its inverting input monitors the output voltage and its non-inverting input is connected to the soft-start capacitor. The two inputs of the error amplifier are tied together by a bi-directional clamp circuit, which forces the soft-start capacitor voltage to stay – ±200mV, for example – around the feedback value. The current generator charging the soft-start capacitor is controlled by the error amplifier output.

At startup, the soft-start capacitor is quickly pre-charged by the internal clamp to within 200mV below the feedback voltage to minimize the startup delay. From this point, the soft-start current starts charging the soft-start capacitor. Whenever the COMP voltage increases above the 3V threshold, which represents approximately 70% of the rated output power capability of the converter, the soft-start current is linearly decreased.

The internal high current clamps between the FB and SS signals offer additional protection during soft-start. Suppose the soft-start capacitor is too small or the converter output voltage isn't increasing to keep pace with the soft-start voltage, as would happen around zero crossing of the line waveform. In this case, the soft-start voltage increases past the FB voltage. If nothing is done, the soft-start voltage would continue to increase and the converter would eventually be operating in an open-loop configuration. The clamp circuit prevents the soft-start voltage from exceeding the FB voltage by more than 200mV, preventing it from running away and, at the same time, prolongs the soft-start time.

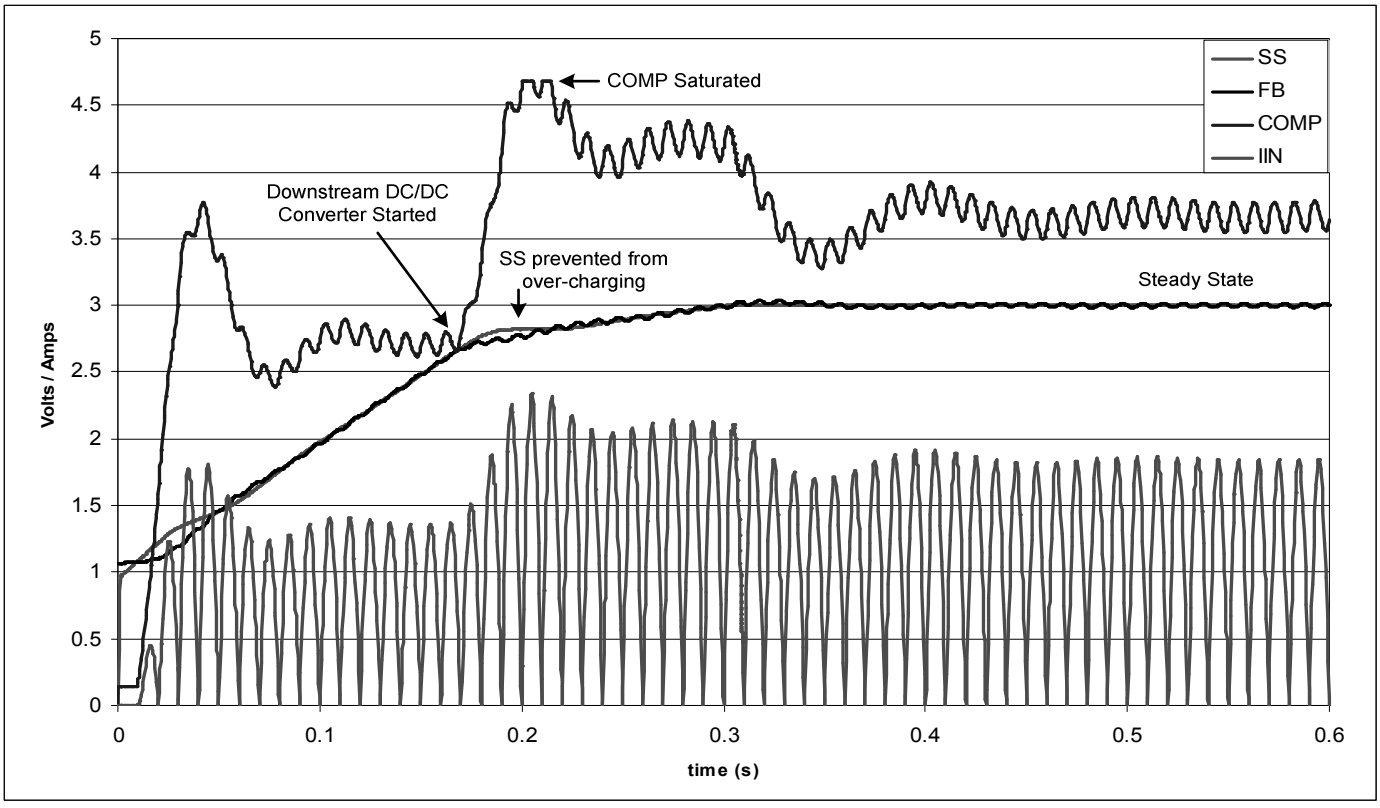

Fig. 11 Soft-start waveforms.

Typical waveforms demonstrating the operation of the optimized startup circuit are shown in Figure 11. At startup, the soft-start capacitor voltage is quickly charged slightly below the feedback voltage level, then the normal soft-start current takes over, as indicated by the slope change in the soft-start capacitor voltage. The feedback voltage remains flat until switching commences, approximately 10ms after startup. Since the error voltage starts from practically zero volts, energy transfer starts gradually. Output voltage starts to rise with a shallow slope since the power through put of the converter is limited. As shown in Fig. 11, the feedback waveform, i.e. the output voltage, is not following the reference; thus the error amplifier output races towards saturation. At about 30ms into the soft-start process, the error signal exceeds the 3V level and the soft-start current is being further reduced to slow down the soft-start and avoid saturation and current limiting. Around 50ms into soft-start, the feedback voltage catches up to the reference and the system finds equilibrium when the reference and the feedback signals ride together. The startup is fully controlled by the error amplifier and closed-loop operation is maintained.

Assuming that full power corresponds to an error voltage of about 4.5V, the roughly 2.6V average of the error signal between 70ms and 180ms indicates that the converter delivers approximately 60% of the rated output current just to charge the output capacitor. At 180ms, the downstream converter's soft-start commences and its input power must also be supported by the PFC converter. Consequently, the previously supported rate of rise at the boost output cannot be sustained. As the error amplifier tries to compensate for the increased load conditions, its output goes higher. At about 200ms, the error amplifier is saturated and the soft-start is practically suspended, reducing the current demand of the output capacitor to near zero. Due to the margin designed into most power converters, the excess power not used by the load slowly charges the output capacitor and the feedback signal eventually catches up with the voltage reference, as shown at 220ms in Figure 11. At that point, closed-loop operation is restored and soft-start continues with a significantly lower, sustainable slope.

It is noteworthy that when the soft-start process is completed, the converter's output and the reference voltage at the non-inverting input of the error amplifier reach their respective final values. The error amplifier must go through one final transition before it settles into steady-state operation. This can be observed around the 300ms mark when the error signal moves from 4.2V to 3.7V. At that point, the converter reaches its regulated output voltage and the charge current of the output capacitor becomes zero. This reduces the required output power and the corrective action of the error amplifier.

I. Current-Sense Protection of MOSFETs and Power-Loss Comparisons

Some method of limiting input current must be provided to protect the converter during fault modes. Most PFC converters use resistive sensing in two topologies regarding where the sense resistor(s) are placed, shown in Figure 12.

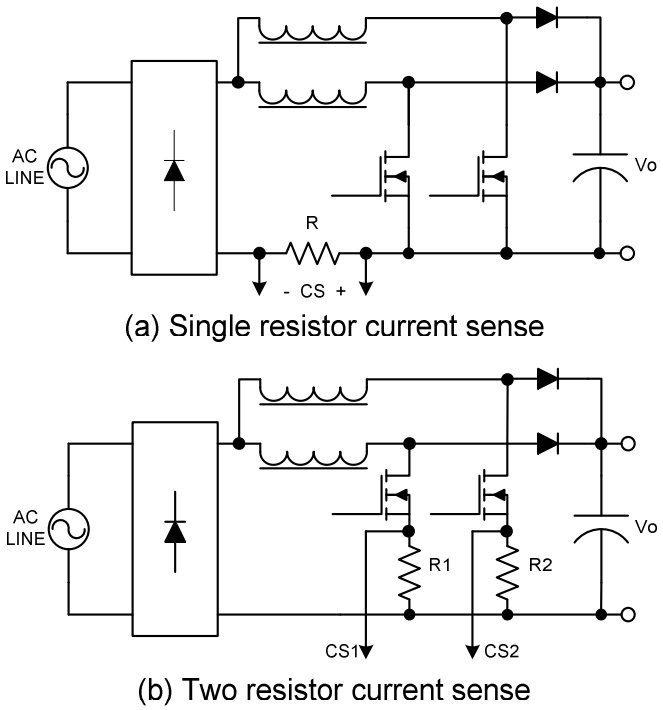

Fig. 12. Current sensing topologies. (a) Single resistor in series with the line voltage, (b) resistors in series with MOSFETs.

Perhaps more important than the topology itself, is a comparison of power dissipated using these two methods. Because the resistors are placed in different branches of the circuit, the RMS current is quite different and a careful study of the power dissipation is warranted.

When the sense resistor is placed in series with the line as in Figure 12(a), the resistor carries the rectified line current. The line current and power dissipation are shown in Equation 8.

$$I_{R,RMS} = \frac{P_{OUT}}{\eta \cdot V_{IN,RMS}}, \quad P_D = I_{R,RMS}^2 \cdot R \tag{8}$$

In this topology, the inrush current is sensed as well as the normal sum of the inductor currents. When selecting the peak current limit, Equation 8 only gives the RMS current, while the peak current is higher. Because the input voltage is less than half the output voltage, the duty cycle for each phase is greater than 50%, and the peak inductor currents add to a value greater than the single-phase peak inductor current according to Figure 13.

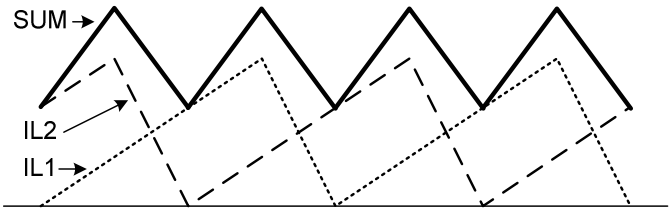

Fig. 13 Current waveforms in the single resistor sensing topology.

Equation 9 shows the peak inductor current for a single phase:

$$I_{L,PK} = \frac{\sqrt{2} \cdot P_{OUT,MAX}}{\eta \cdot V_{IN,MIN}} \tag{9}$$

where $P_{OUT,MAX}$ is the total output power of the converter. Because the duty cycle at minimum line voltage is greater than 50%, the peak inductor currents sum to a value of:

$$I_{L,SUM} = \frac{\frac{3}{2} \cdot V_{OUT} - 2\sqrt{2} \cdot V_{IN,MIN}}{V_{OUT} - \sqrt{2} \cdot V_{IN,MIN}} \cdot I_{L,PK} \tag{10}$$

When selecting the current sense resistor value, the inductor current sum must be used as shown in Equation 10.

In the second topology of Figure 12(b), two individual sense resistors are placed in series with the MOSFETs, which provide a local high-speed current limit path for each MOSFET. In this method, the sense resistor current is the same as the MOSFET drain current as shown in Equation 11:

$$I_{Q,RMS} = \frac{\sqrt{2} \cdot P_{OUT,MAX}}{\eta \cdot V_{IN,MIN}} \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2} \cdot V_{IN,MIN}}{9\pi \cdot V_{OUT}}} \tag{11}$$

The power dissipated for both resistors is:

$$P_D = I_{Q,RMS}^2 \cdot (R1 + R2) \tag{12}$$

Table I shows a comparison of these two topologies based on a 400W design example for the worst case power dissipations at minimum input voltage.

For a useful comparison the current sense thresholds have been selected the same. Peak Sense Current is the maximum current flowing through the individual current sense resistors.

TABLE I
CURRENT SENSING TOPOLOGY COMPARISON FOR 400W DESIGN AT VIN=85V

Parameter	Single Resistor	Two Resistor
V_{th}: Sensing Threshold	200mV	200mV
Peak Sense Current	9.5A	7.4A each
Resistor RMS current	5.2A	2.6A each
Sense Resistor Value	20mΩ	25mΩ each
Total Power Dissipation	0.54W	0.34W total

The RMS current values are for the individual resistors, while the last row is the total power dissipation, with 0.34W representing the sum of the power dissipated by R1 and R2.

As Table I demonstrates, using two individual current-sense elements in series with the boost transistor achieves lower overall power dissipation in the interleaved BCM PFC converter. Furthermore, it can provide tighter, independent, current protection for the MOSFET transistors.

J. Phase-Fail Detection

One interesting problem can arise in the interleaved BCM converter when one phase ceases to operate. This fault mode could be caused by a manufacturing problem, e.g. no gate resistor, or one of the power train components failing in an open circuit. Since the one power stage cannot supply the entire designed output power, some means of protection must be included to protect the remaining power train. Therefore, a simple logic circuitry is desirable to sense when either power stage ceases to switch. If this is detected, the control circuitry is put into the restart mode where the single working phase is operating at the restart timer frequency. Because the switching frequency is low, little power is delivered and the converter is self protecting.

VI. DESIGN EXAMPLE

As a design example, an interleaved BCM converter has been designed to these specifications:

$P_{OUT,MAX}$	400W
$V_{IN,RMS}$	85~265V
V_{OUT}	405V
Line Frequency	47~63 Hz
Minimum Switching Frequency	30kHz

When designing a BCM PFC converter, the first consideration is given to the design and sizing of the power inductors. The inductor value, along with the output power and input line voltage, determines the minimum switching frequency of the design. A standard practice is to place this minimum frequency higher than the highest audible frequency of 20kHz. Supposing a minimum switching frequency of $f_{SW,MIN}$, the inductor value can be found by rearranging Equation 4. The resonant portion of the period is ignored because the resonant time only represents approximately 5% of the switching period, and this estimates the inductor value:

$$L_{MAX} = \frac{\eta \cdot \left(V_{OUT} - \sqrt{2} \cdot V_{IN,RMS}\right) \cdot V_{IN,RMS}^2}{V_{OUT} \cdot f_{SW,MIN} \cdot P_{OUT,MAX}} = 380\mu H \tag{13}$$

The peak current in the inductor is then found from Equation 14:

$$I_{L,PK} = \frac{\sqrt{2} \cdot P_{OUT,MAX}}{\eta \cdot V_{IN,MIN}} = 7.4A \tag{14}$$

The above calculation assumes a minimum switching frequency, $f_{SW,MIN}$ of 30kHz. The first design compromise is maximizing the inductance gives the highest power factor,

while incurring higher resistive losses. An inductor of this value, with the ability to carry the required peak current, is excessively large and has high winding losses. If the inductance is reduced, a smaller number of turns, and therefore a smaller winding cross-section, is required, and the winding losses are reduced. As a compromise, the inductors are designed to be 220µH. Using 220µH as the inductor value, the minimum switching frequency is approximately 51kHz.

The output capacitor of the converter is sized to provide hold-up time during a line cycle drop out. The longest hold-up occurs when the line frequency is the lowest, while the worst-case voltage droop is at the highest output power. The minimum capacitance can be found by applying conservation of power at the output:

$$C_{OUT,MIN} = \frac{2 \cdot P_{OUT,MAX}}{\eta \cdot f_{LINE,MIN} \cdot \left(V_{OUT}^2 - V_{OUT,MIN}^2\right)} = 328\,\mu F \quad (15)$$

where $V_{OUT,MIN}$ is the minimum output voltage after a single cycle line drop out. In this example, $V_{OUT,MIN}$ is set to 320V. A capacitor with the closest standard value of 330µF would be chosen for this design.

The MOSFETs are selected for low conduction losses, although a compromise exists between low $R_{DS(ON)}$ and higher capacitance. When a MOSFET with an excessively low $R_{DS(ON)}$ is selected, the large capacitance of the MOSFET changes the resonant action on the switching node. In particular, around zero crossings in the line voltage, the line current is distorted because the energy stored in the parasitic capacitance is larger than the energy stored in the inductor. When the MOSFET turns off, the drain voltage does not reach the output voltage, and no energy is transferred to the output. This design compromise suggests that the line current has the least distortion if the MOSFET capacitance is minimized, while the power inductor has the maximum allowable value to stay above the minimum switching frequency set forth earlier. The trade-off is higher conduction losses in the inductor and in the MOSFETs, leading to lower efficiency, as well as larger inductor volume. The conduction losses in the MOSFET are found by multiplying the square of the RMS current in Equation 11 by the $R_{DS(ON)}$ of the device. As a compromise between conduction losses and line current distortion, the FDPF20N50 is selected. This MOSFET has a $R_{DS(ON)}$ of 230mΩ, the conduction losses at low input line, and maximum power of approximately 1.5W per MOSFET.

An advantage of the BCM topology is that the boost diodes can be standard ultra-fast diodes. The boost diodes dissipate power proportional to the average current times their forward voltage:

$$P_D = I_{D,AVG} \cdot V_F, \quad I_{D,AVG} = \frac{P_{OUT,MAX}}{2 \cdot V_{OUT}} \quad (16)$$

While the average diode current is small, the small diode conduction duty cycle results in a high peak diode current. As a result, the boost diode should be sized to carry the peak current calculated in Equation 14. For this design, the 8A, 600V FFP08H60S diode was selected.

Now that the power stage components are defined the controller can be set up. The resistive dividers to sense the input and output voltages can be calculated from the respective thresholds of the sense circuitry used for brownout and over-voltage protection or from the reference voltage of the error amplifier. Figure 14 shows the schematic of these circuits.

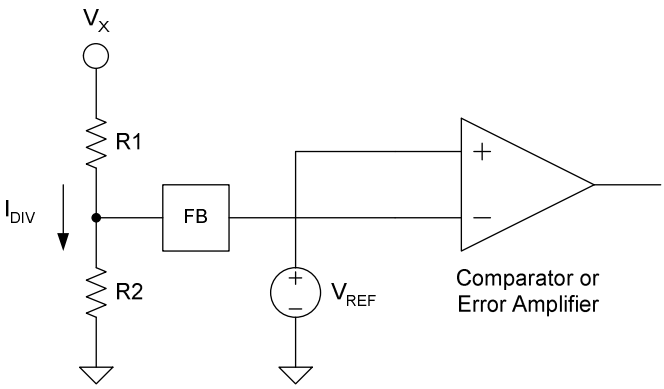

Fig. 14 Setting up high-voltage dividers.

V_{REF} is the voltage the divider must produce when V_X is at the desired voltage for the particular function. For high-voltage sensing, such as dividing down the input and output voltages, R2 might be implemented using two or three resistors connected in series to pass safety regulations. Since the dividers are connected to a high voltage, the maximum current of the divider must be carefully considered to minimize power dissipation. Equations 17 through 19 provide guidance to select the right resistor values.

$$I_{DIV} = \frac{P_{DIV}}{V_X} \quad (17)$$

where P_{DIV} is the total power dissipated by R1 and R2.

$$R2 = \frac{V_{REF}}{I_{DIV}} = \frac{V_{REF} \cdot V_X}{P_{DIV}} \quad (18)$$

$$R1 = \frac{V_X - V_{REF}}{I_{DIV}} = \frac{(V_X - V_{REF}) \cdot V_X}{P_{DIV}} \quad (19)$$

Equation 20 shows an alternative expression to calculate R1 from the R2 value calculated in Equation 18:

$$R1 = \left(\frac{V_X}{V_{REF}} - 1\right) \cdot R2 \quad (20)$$

Next, the zero current detect (ZCD) circuit is defined based on the simplified circuit diagram shown in Figure 15.

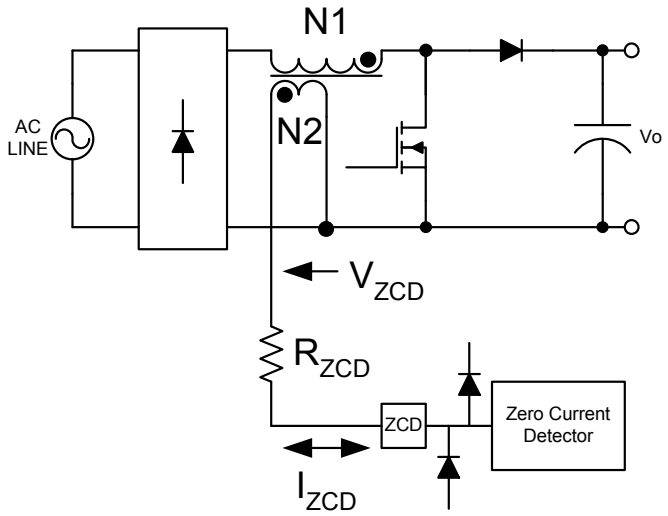

Fig. 15 Typical ZCD setup for BCM PFC controllers.

In its simplest implementation, zero current detection requires an auxiliary winding on the boost inductor and a resistor connecting the sense winding to the ZCD pin of the controller. The main purpose of this resistor is to limit the current into and out of the ZCD pin of the controller. The voltage is usually limited internal to the IC using various clamp circuits, which prevents the pin from exceeding its maximum voltage rating. In most controllers, the clamps hold the ZCD pin near GND. The sense voltage V_{ZCD} is limited by the operating conditions of the converter and the turns ratio of the sense winding, according to:

$$-2\cdot\sqrt{2}\cdot V_{IN,RMS,MAX}\cdot\frac{N2}{N1}\le V_{ZCD}\le V_O\cdot\frac{N2}{N1} \tag{21}$$

Since the output voltage must be higher than the peak of the input voltage, the maximum voltage across the ZCD resistor is applied when V_{ZCD} equals the reflected output voltage at the sense winding. The ZCD resistor value can be determined from the maximum current capability of the ZCD sense circuitry as:

$$R_{ZCD}\ge\frac{V_O}{I_{ZCD,MAX}}\cdot\frac{N2}{N1} \tag{22}$$

It is desirable to minimize the ZCD resistor value to diminish the effect of parasitic capacitances associated with the rest of the ZCD circuit.

Compensating the voltage loop of a PFC converter is well documented in the literature. A detailed analysis of the voltage regulation loop is beyond the scope of this paper and readily available in reference [4]. For completeness, Equation 23 shows a solution that gives a satisfactory result:

$$C_{COMP}=\frac{g_M\cdot R2}{0.04\cdot\pi\cdot f_{LINE}\cdot(R1+R2)} \tag{23}$$

where C_{COMP} is the compensation capacitor of a g_M-type error amplifier, g_M is its transconductance, R1 and R2 are the feedback network, as shown in Figure 14, and f_{LINE} is the input line frequency.

The next parameter calculated is the maximum on-time. The longest conduction period of the boost switch occurs at the minimum input voltage and at the peak of the line cycle. To compute this, the minimum input RMS voltage ($V_{IN,MIN}$), the converter's output voltage (V_O), the boost inductance (L), and the maximum output power (P_O), must be known. In addition, the expected efficiency of the converter, η, has to be estimated. The maximum on-time for this design is found by:

$$t_{ON,MAX}=\frac{L\cdot P_{OUT}}{\eta\cdot V_{IN,RMS}^2}=\frac{220\mu\cdot 400}{0.92\cdot 85^2}=13.2\mu s \tag{24}$$

Equation 24 is very similar to Equation 1 except a factor of two difference. It is the result of interleaving; $t_{ON,MAX}$ is defined as the maximum on-time of the boost switch for one phase. Since each phase is designed for half of the converter power rating, this introduces the factor-of-two difference. Calculate the maximum on-time to accommodate component tolerances in the design and potential imbalance in the power delivery between the interleaved channels. The controller is set up with 14.5µs of maximum on-time, a 10% margin. The maximum output power per phase is approximately 220W or 440W for the complete power supply.

Once the maximum on-time is defined, the current limit can be adjusted and the current-sense resistor value calculated. The highest peak current under normal operation, in regulation, is at minimum input voltage and at the peak of the line cycle. This peak current can be calculated as:

$$I_{L,PK}=\frac{\sqrt{2}\cdot V_{IN,RMS,MIN}}{L}\cdot t_{ON,MAX} \tag{25}$$

After substitutions, using 14.5µs on-time, Equation 25 yields a peak current value slightly below 8A for the design. The current sense resistor value is obtained by:

$$R_{CS}=\frac{V_{CS}}{I_{L,PK}}=\frac{0.2V}{8A}=0.025\Omega \tag{26}$$

Before the design is complete, the converter's startup dV/dt must be defined. The converter is designed for 440W output power, which translates to approximately 1.1A of maximum output current at 400V output. It is recommended that about 20% to 30% of this current be used to charge the output capacitor to avoid triggering over-current protection and loosing closed-loop operation when the downstream converter starts drawing current from the output. It is also a good compromise to ensure that the error amplifier has to make a relatively small adjustment when the capacitor charge current becomes zero upon entering regulation. The slope of the output voltage rise during startup should be set to:

$$\frac{dV}{dt}=\frac{0.3\cdot I_{O,MAX}}{C_O}=\frac{0.3\cdot 1.1A}{330\mu F}=1\frac{V}{ms} \tag{27}$$

Note that during startup, the output voltage increases with this constant slope; therefore, the startup time of the converter is a function of the input voltage. At low-line operation, the boost output capacitor is peak charged to approximately 150V.

It takes 255ms to reach the 405V nominal voltage. In case of high-line operation, the capacitor voltage starts from around 320V and reaches its final value in about 80ms. In either case, it is important to recognize that starting a PFC converter takes orders of magnitudes longer than the soft-start time of DC/DC power supplies.

VII. CONCLUSIONS

The interleaved boundary conduction mode PFC exploits the advantages of a single-stage BCM converter and adds the advantages of lower peak currents, higher effective switching frequency at the input and output terminals, as well as better thermal management. The topology extends the power range of single-stage BCM converters and allows design modularization where smaller BCM converters can be designed, interleaved, and replicated for higher power applications. Finally, the interleaved BCM converter has lower differential mode EMI than a single converter designed for the same output power.

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