

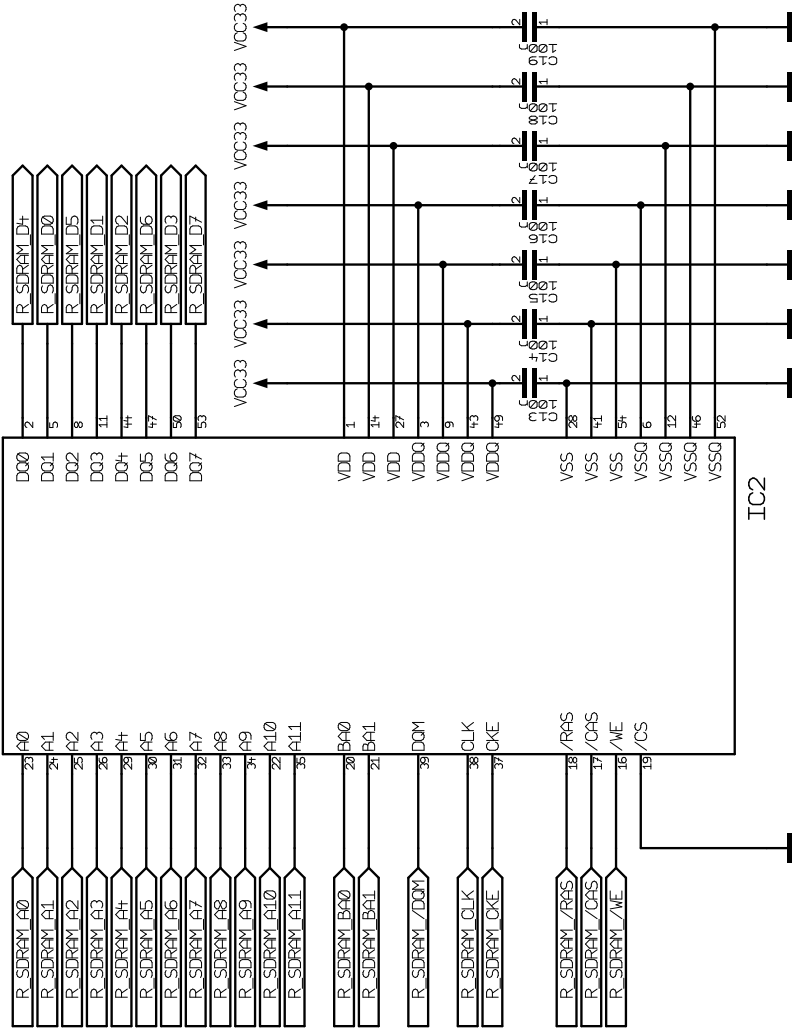
IC1

ATXMEGA128A1

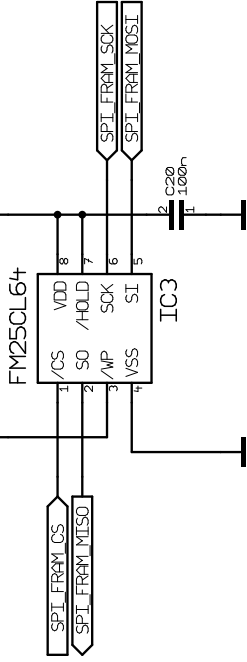
AREF	ADC0	AC0	PA0	35	D0	FPGA_DATA_OUT_CH1	
ADCC1	AC1	PA1	36	D1	FPGA_DATA_OUT_CH1		
DA00	ADC2	AC2	PA2	37	D2	FPGA_DATA_OUT_CH1	
DACC1	ADC3	AC3	PA3	38	D3	FPGA_DATA_OUT_CH1	
ADCC4	AC4	PA4	39	D4	FPGA_DATA_OUT_CH1		
ADCC5	AC5	PA5	100	D5	FPGA_DATA_OUT_CH1		
ADCC6	AC6	PA6	1	D6	FPGA_DATA_OUT_CH1		
ADCCout	ADC7	AC7	PA7	2	D7	FPGA_DATA_OUT_CH1	
AREF	ADC0	AC0	PB0	5	D0	FPGA_DATA_OUT_CH2	
ADCC1	AC1	PB1	6	D1	FPGA_DATA_OUT_CH2		
DA00	ADC2	AC2	PB2	7	D2	FPGA_DATA_OUT_CH2	
DACC1	ADC3	AC3	PB3	8	D3	FPGA_DATA_OUT_CH2	
TMS	ADCC4	AC4	PB4	9	D4	FPGA_DATA_OUT_CH2	
TDI	ADCC5	AC5	PB5	10	D5	FPGA_DATA_OUT_CH2	
TK	ADCC6	AC6	PB6	11	D6	FPGA_DATA_OUT_CH2	
ADCCout	TDD	ADC7	PB7	12	D7	FPGA_DATA_OUT_CH2	
OC0A	OC0ALS	SDA	PC0	15	TRIGGER_ARMED		
XCK0	OC0BLS	SOL	PC1	16	TRIGGER_READY		
OC0C	OC0BLS	RXD0	PC2	17	TRIGGER_TRIG'D		
OC0D	OC0BHS	TXD0	PC3	18	TRIGGER_AUTO		
OC1A	OC0CLS	/SS	PD4	19	FPGA_SERIAL_CLK		
XCK1	OC1B	OC00HS	MOSI	PC5	FPGA_SERIAL_DATA		
RXD1	OC0DLS	MISO	PC6	21	FPGA_SERIAL_LOAD		
EVout	CLKout	TXD1	OC0DHS	SOX	PC7	FPGA_RUN	
OC0A	SDA	PD0	25	FPGA_RD_CLK			
XCK0	SOL	PD1	26	FPGA_READY			
OC0C	RXD0	PD2	27	R/D_BEDIENEINLEIT			
OC0D	TXD0	PD3	28	T/D_BEDIENEINLEIT			
OC1A	/SS	PD4	29	SPT_TASTEN_LD			
XCK1	OC1B	MOSI	PD5				
RXD1	MISO	PD6	31	SPT_TASTEN_MISO			
EVout	CLKout	TXD1	SOX	PD7	SPT_TASTEN_SOX		
OC0A	SDA	PE0	35	ENCODER_YPOS_CH1_B			
XCK0	SOL	PE1	36	ENCODER_YPOS_CH1_A			
OC0C	RXD0	PE2	37	ENCODER_YPOS_CH2_B			
OC0D	TXD0	PE3	38	ENCODER_YPOS_CH2_A			
OC1A	/SS	PE4	39	SPT_FRAM_CS			
XCK1	OC1B	MOSI	PE5	SPT_FRAM_SOX			
RXD1	MISO	PE6	41	SPT_FRAM_MISO			
EVout	CLKout	TXD1	OC0DHS	CLK	PE7	SPT_FRAM_MOSI	
OC0A	SDA	PF0	45	RTC_SDA			
XCK0	SOL	PF1	46	RTC_SCL			
OC0C	RXD0	PF2	47	DISPLAY_BUSY			
OC0D	TXD0	PF3	48	DISPLAY_TXD			
OC1A	/SS	PF4	49	ENCODER_PRETRIGGER_B			
XCK1	OC1B	MOSI	PF5	ENCODER_PRETRIGGER_A			
RXD1	MISO	PF6	51	USB_FDT232RL_TXD			
TXD1	SOX	PF7	52	USB_FDT232RL_RXD			
LPC ALE12 2P1	LPC ALE1 2P1	LPC ALE1 2P1	99H ALE12 2P1	99H ALE1 2P1	ISRAM 2P1	PH0	SDRAM_AE
/WE1	/RE1	/WE1	/RE1	/RE1	/OAS	PH1	SDRAM_OAS
/ALE11	/ALE11	/ALE11	/ALE11	/ALE11	/RAS	PH2	SDRAM_RAS
/ALE21	/ALE21	/ALE21	/ALE21	/ALE21	/DOM	PH3	SDRAM_DOM
/CS0, A16	/CS0, A16	/CS0, A16	/CS0, A16	BA0	PH4	SDRAM_BA0	
/CS1, A17	/CS1, A17	/CS1, A17	/CS1, A17	BA1	PH5	SDRAM_BA1	
/CS2, A18	/CS2, A18	/CS2, A18	/CS2, A18	OK	PH6	SDRAM_OK	
/CS3, A19	/CS3, A19	/CS3, A19	/CS3, A19	CLK	PH7	SDRAM_CLK	
D0, A0, A8	D0, A0	D0, A0	D0	D0	D0	P30	SDRAM_D0
D1, A1, A9	D1, A1	D1, A1	D1	D1	D1	P31	SDRAM_D1
D2, A2, A10	D2, A2	D2, A2	D2	D2	D2	P32	SDRAM_D2
D3, A3, A11	D3, A3	D3, A3	D3	D3	D3	P33	SDRAM_D3
D4, A4, A12	D4, A4	D4, A4	D4	D4	A8	P34	SDRAM_A8
D5, A5, A13	D5, A5	D5, A5	D5	D5	A9	P35	SDRAM_A9
D6, A6, A14	D6, A6	D6, A6	D6	D6	A10	P36	SDRAM_A10
D7, A7, A15	D7, A7	D7, A7	D7	D7	A11	P37	SDRAM_A11
		A8	A8, A16	A0, A8	A0	PK0	SDRAM_A0
		A9	A9, A17	A1, A9	A1	PK1	SDRAM_A1
		A10	A2, A10, A18	A2, A10	A2	PK2	SDRAM_A2
		A11	A3, A11, A19	A3, A11	A3	PK3	SDRAM_A3
		A12	A4, A12, A20	A4, A12	A4	PK4	SDRAM_A4
		A13	A5, A13, A21	A5, A13	A5	PK5	SDRAM_A5
		A14	A6, A14, A22	A6, A14	A6	PK6	SDRAM_A6
		A15	A7, A15, A23	A7, A15	A7	PK7	SDRAM_A7

SDRAM

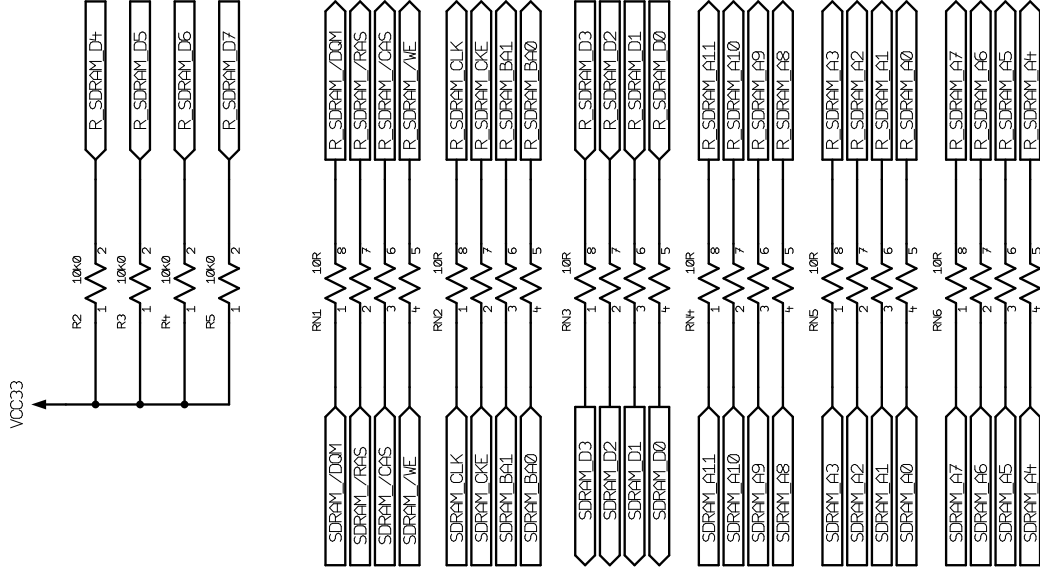
MT48LC16M8A2



FRAM



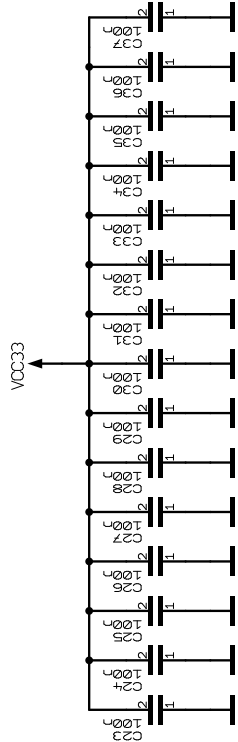
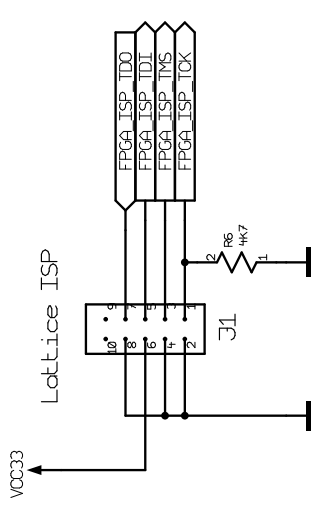
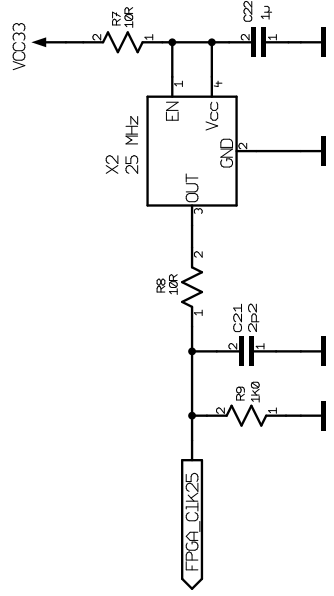
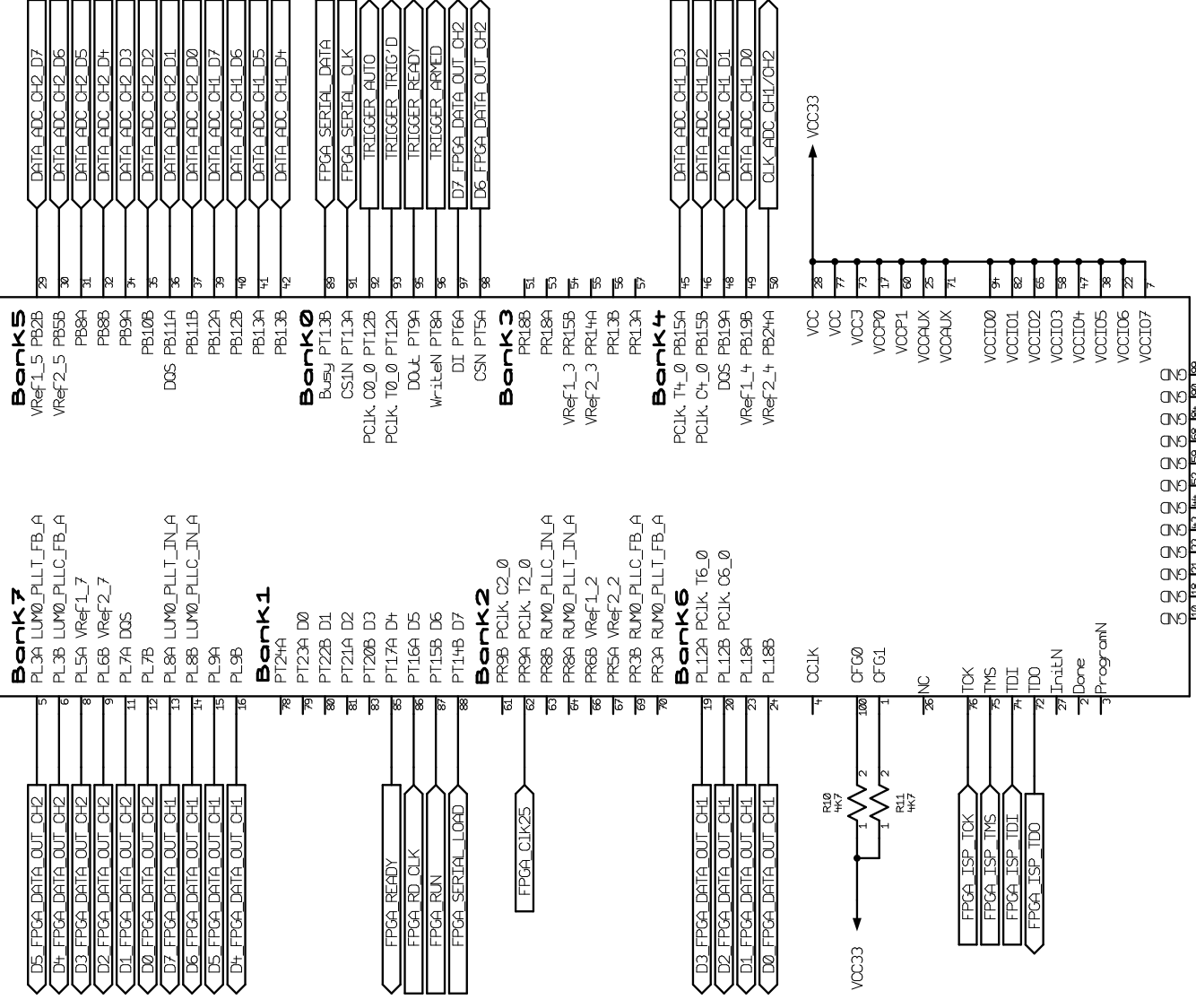
R-NETZWERK



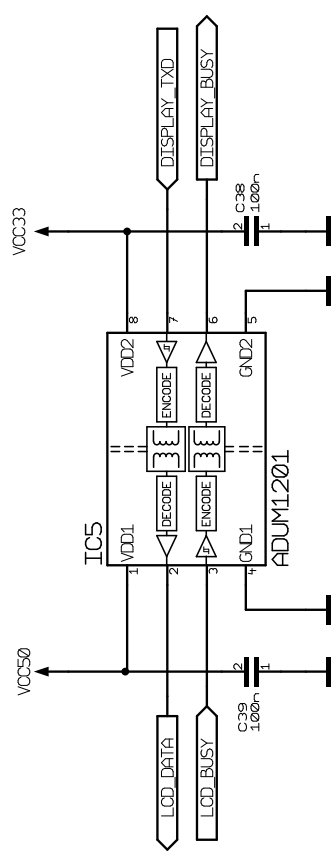
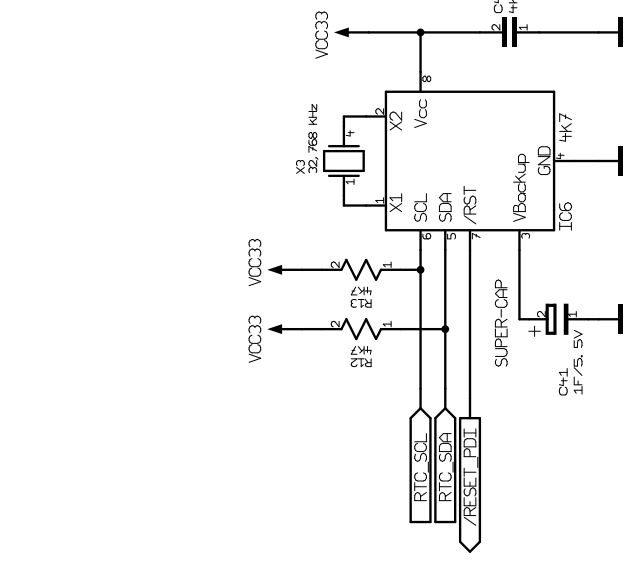
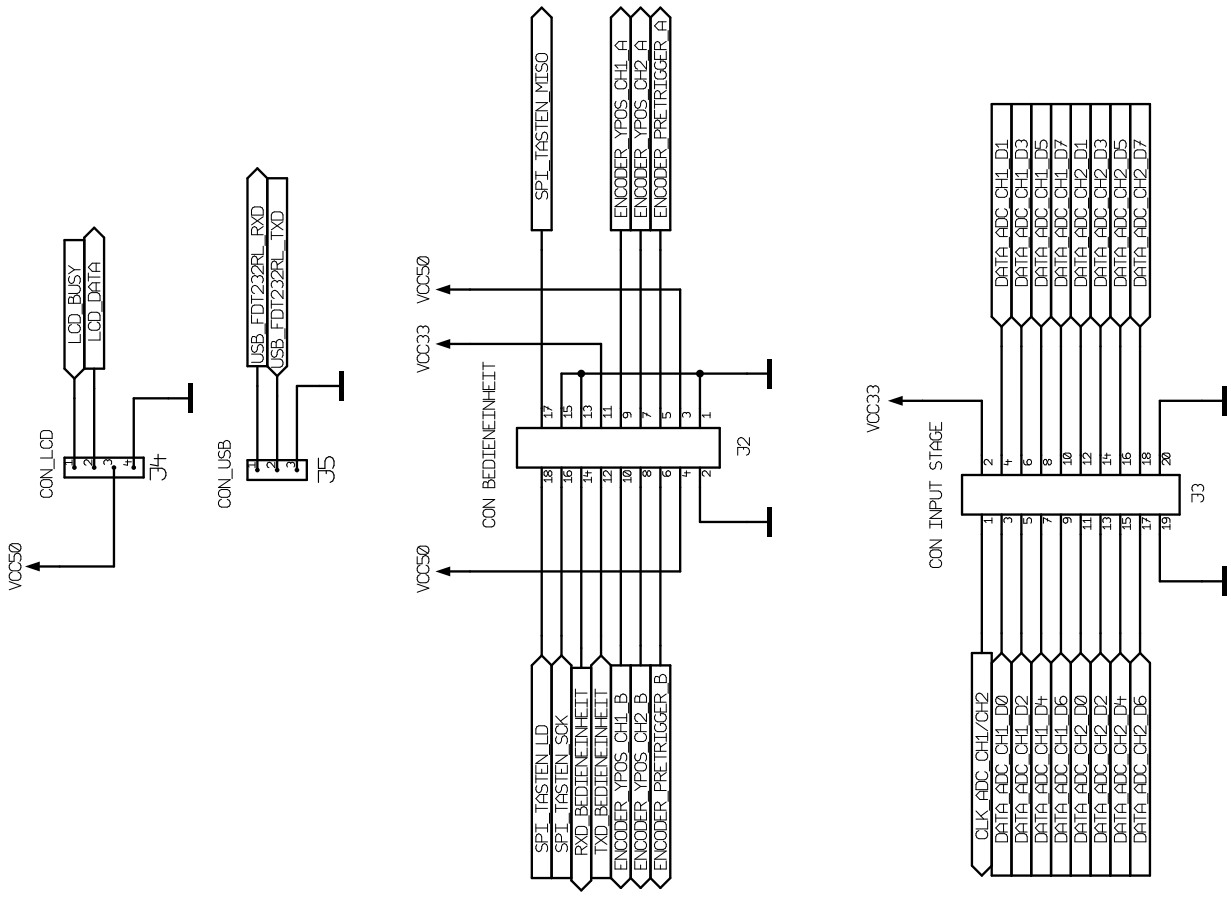
Maßstab	1. 03%	Zeichner	Steffen Hoerhold	Blatt	2 / 5
Änderung	19. 08. 11	Titel			
Ausgabe	19. 08. 11	DSO MAIN MEMORY			
Firma		Projekt DSO_MAIN_LAYOUT. T2001			

LATTICE XP3C

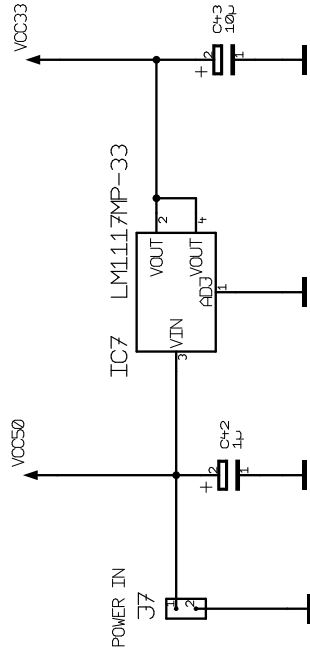
IC4



Maßstab	1. 03%	Zeichner	Steffen Hoerhold	Blatt	3 / 5
Änderung	19. 08. 11	Titel			
Ausgabe	19. 08. 11	DSO MAIN FPGA			
Fl.umo		Projekt			
		DSO_MAIN_LAYOUT.T2001			



Maßstab	1. 03%	Zeichner	Steffen Hoerhold	Blatt	4 / 5
Änderung	19. 08. 11	Titel			
Ausgabe	19. 08. 11	DSO MAIN ANSCHLUSS, RTC			
Firma		Projekt			
		DSO_MAIN_LAYOUT. T2001			



Maßstab 1: 03%

Zeichner Steffen Hoberhold

Blatt 5 / 5

Änderung 19. 08. 11

Titel

DSO MAIN VERSORGUNG

Ausgabe 19. 08. 11

Projekt

DSO_MAIN_LAYOUT. T2001

Firma