

AS8002

Solar Photovoltaic Inverter Measurement IC with Fast Over Current Detection

1 General Description

Power inverters in solar photovoltaic systems are often connected directly to the electricity grid in order to inject the created energy into the mains and act as an electricity supplier. This energy must comply with certain regulations that set the standard in terms of quality and safety which requires of accurate measurements.

The AS8002 is a highly accurate measurement IC that allows monitoring the generated energy with low cost shunt resistors or other sensors for the current and resistor dividers for the voltage.

This approach allows avoiding more expensive sensing devices while achieving the required accuracy for DC and AC measurements of current and voltage, as well as stability over the operating temperature range of the inverter.

The 12-bit ADC samples the voltage and current and provides their instantaneous values through an SPI interface.

The 12-bit ADC is preceded by low noise programmable gain amplifiers in order to accommodate different sensors.

The ADC has three multiplexed inputs, offering one secondary channel in addition to the main voltage and current.

The on-chip temperature sensor provides the inverter designer the option of temperature compensation for any of the measured parameters or functional blocks provided, over the full operating temperature range of the device.

The on-chip voltage reference is connected to the ADC and to REF.

An external crystal oscillator is not required as a high accuracy internal oscillator clock is available.

The independent over current interrupt detects a high current on the grid and allows the processor to open the switches without waiting for the ADC conversion.

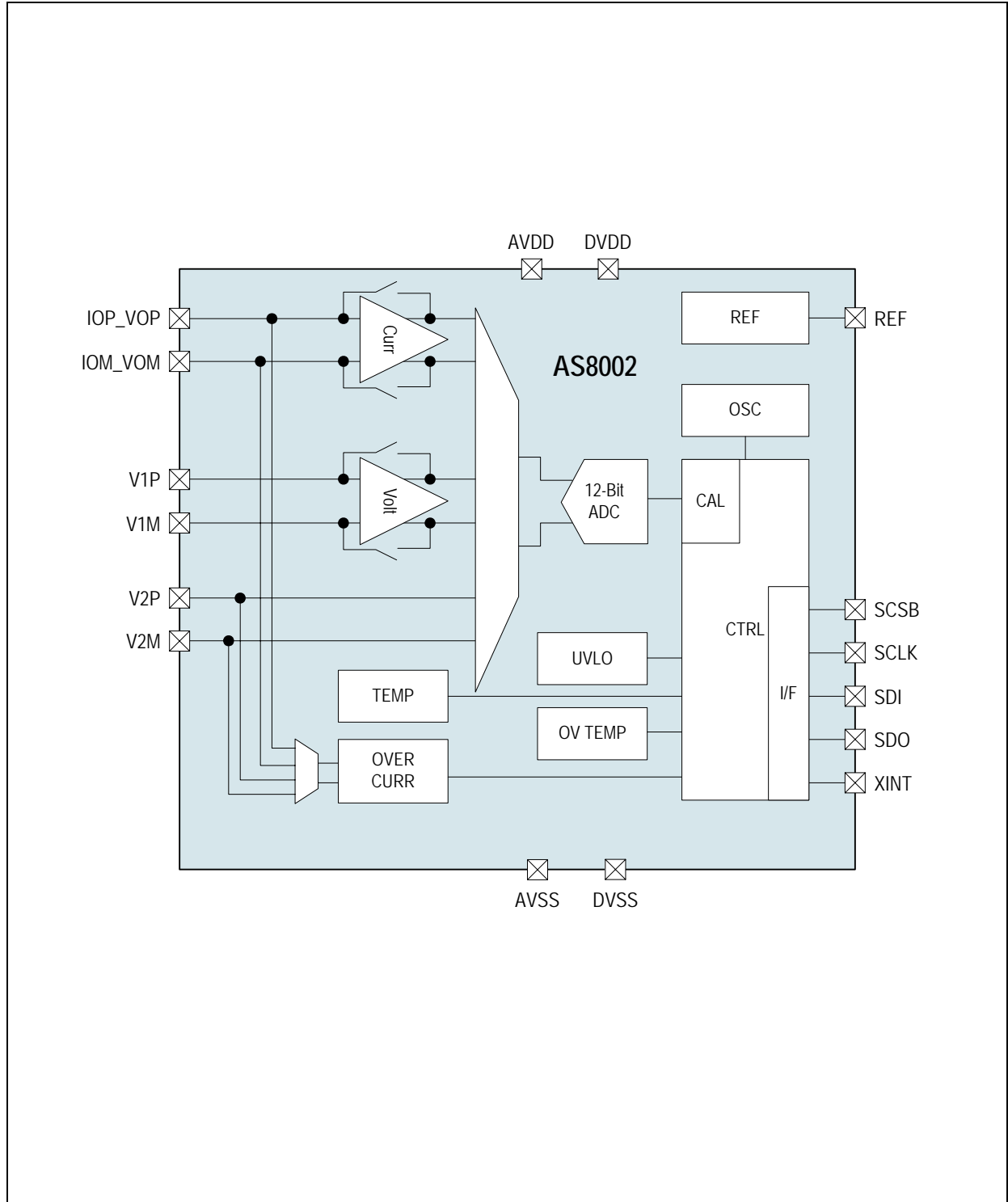
2 Key Features

- 12-Bit 100 kSPS ADCs for accurate voltage and current measurement
- Programmable gain amplifiers to accommodate for different sensors
- Three multiplexed inputs to the 12-Bit ADC for secondary measurements that require high accuracy and fast sampling rates
- On chip temperature sensor connected to one of the inputs of the multiplexer
- On-chip voltage reference with small temperature coefficient (10ppm/K typ). This reference is available at the pin REF.
- Low power on chip oscillator
- SPI compatible interface
- Internal registers for easy offset and gain compensation
- Interrupt alerts (including Under Voltage Lock-Out and Over Temperature)
- Independent programmable over current interrupt

3 Applications

The AS8002 is suitable for PV inverter grid monitoring, Wind inverter grid monitoring, Isolated voltage sensing, Uninterruptible Power supplies and Power conditioners.

Figure 1. AS8002 Block Diagram

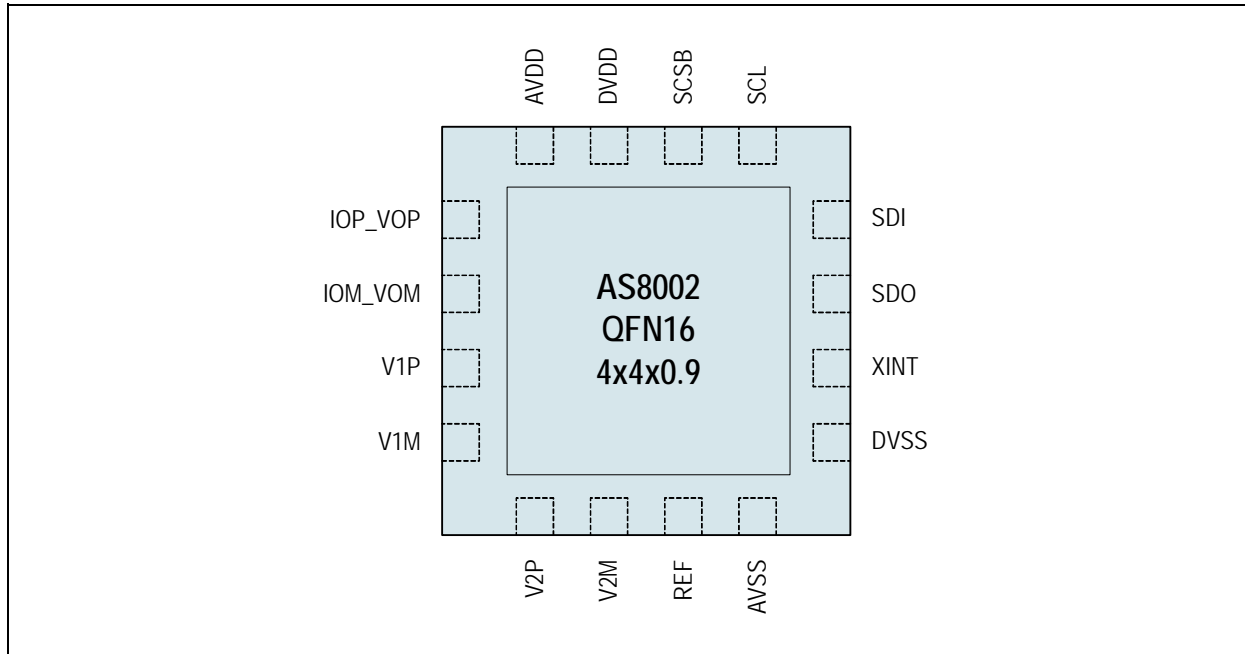


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4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

| Pin Name | Pin Number | Pin Type | Description |
|----------|------------|--------------------------|---|
| IOP_VOP | 1 | Analog pin | Analog Input Channel 0. Positive input of the differential analog input. |
| IOM_VOM | 2 | Analog pin | Analog Input Channel 0. Negative input of the differential analog input. |
| V1P | 3 | Analog pin | Analog Input Channel 1. Positive input of the differential analog input. |
| V1M | 4 | Analog pin | Analog Input Channel 1. Negative input of the differential analog input. |
| V2P | 5 | Analog pin | Analog Input Channel 2. Positive input of the differential analog input. |
| V2M | 6 | Analog pin | Analog Input Channel 2. Negative input of the differential analog input. |
| REF | 7 | Analog pin | Reference Positive Input Voltage. |
| AVSS | 8 | Supply pin | Ground reference for the analog circuitry. |
| DVSS | 9 | Supply pin | Ground reference for the digital circuitry. |
| XINT | 10 | Digital input/output pin | Interrupt pin, active low |
| SDO | 11 | Digital output pin | Serial peripheral interface (SPI): Serial Data Output |
| SDI | 12 | Digital input pin | Serial peripheral interface (SPI): Serial Data input |
| SCLK | 13 | Digital input pin | Serial peripheral interface (SPI): Serial Clock |
| SCSB | 14 | Digital input pin | Serial peripheral interface (SPI): Serial Chip Select (active low) |
| DVDD | 15 | Supply pin | Digital positive supply |
| AVDD | 16 | Supply pin | Analog positive supply |
| AVSS | PAD | Supply pin | Ground reference for the analog circuitry. |

Note: Pin number assignment is likely to change.

5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Block Electrical Characteristics](#) on page 6 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

| Parameter | Min | Max | Units | Comments |
|---|-------|----------------------|-------|---|
| DC supply voltage (V _{DD}) | -0.3 | +5.0 | V | AVDD, DVDD |
| Input pin voltage (V _{IN}) | -0.3 | V _{DD} +0.3 | V | |
| Electrostatic discharge (ESD) | -1000 | 1000 | V | Norm: MIL 883 E method 3015 |
| Storage temperature (T _{strg}) | -55 | 125 | °C | |
| Lead temperature profile (T _{body}) | | | | The reflow peak soldering temperature (body temperature) specified is in accordance with <i>IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"</i> . |
| Humidity non-condensing | 5 | 85 | % | |

6 Electrical Characteristics

6.1 Operating Conditions

Table 3. Operating Conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------|---------------------------------|----------------------------|------|-----|-----|-------|
| AVDD | Positive analog supply voltage | | 3.0 | 3.3 | 3.6 | V |
| AVSS | Negative analog supply voltage | | 0 | | 0 | V |
| A - D | Difference of supplies | AVDD – DVDD AVSS – DVSS | -0.1 | | 0.1 | V |
| DVDD | Positive digital supply voltage | | 3.0 | 3.3 | 3.6 | V |
| DVSS | Negative digital supply voltage | | 0 | | 0 | V |
| TAMB | Ambient temperature | | -40 | 25 | 125 | °C |
| ISUPP | Supply current | | | | 5 | mA |

6.2 Block Electrical Characteristics

AVDD=3.0V to 3.6V, TAMB= -40 to +125°C. Typical values at TAMB= +25°C and AVDD=3.3V (unless otherwise specified).

Table 4. Block Electrical Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|------------------------------------|---------------------------------------|--------|------|------------|-------|
| ADC DC Accuracy | | | | | | |
| RES | Resolution | | | | 12 | Bits |
| INL | Integral Nonlinearity | | -0.99 | | +0.99 | LSB |
| DNL | Differential Nonlinearity | Guaranteed No Missed Codes to 12 Bits | -0.99 | | +0.99 | LSB |
| OFS | Offset Error | | | ±0.6 | ±4 | LSB |
| OFSM | Offset Error Match | | | ±0.1 | | LSB |
| GAIN | Gain Error | | | | ±4 | LSB |
| GAINM | Gain Error Match | | | ±0.1 | | LSB |
| ADC Dynamic Specifications f_{IN}=10 kHz Sine Wave Input | | | | | | |
| SINAD | Signal to Noise = Distortion Ratio | f _{IN} = 10kHz | | 71 | | dB |
| SNR | Signal-to-Noise Ratio | | | 72 | | dB |
| THD | Total Harmonic Distortion | | | -78 | | dB |
| SFDR | Spurious-Free Dynamic Range | | | 84 | | dB |
| CCISOL | Channel-to-Channel Isolation | f _{IN} = 40kHz | | -79 | | dB |
| FPBW | Full Power Bandwidth | at 3dB | | 35 | | MHz |
| FLBW | | at 0.1dB | | 3.6 | | |
| ADC Analog Inputs of the Analog-to-Digital Converter | | | | | | |
| VX+ – VX- | Differential Input Voltage Ranges | | -VREF | | VREF | V |
| VCMIN | Input Common Mode Voltage | | VREF/2 | | VDD-VREF/2 | V |
| AILEAK | DC Leakage Current | | -1 | | +1 | µA |
| AIIZT | Input Capacitance | Track mode | | TBD | | pF |
| AIIZH | | Hold mode | | TBD | | pF |
| ADC Conversion Rate | | | | | | |
| t _{CONV} | Conversion Time | Running from the internal oscillator | | | 10 | µs |

Table 4. Block Electrical Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-------------------------------------|---------------------------------|--|------------|------|----------|------------------|
| $t_{ACQUISITION}$ | Track-and-Hold Acquisition Time | | | | TBD | μs |
| TPUT | Throughput Rate | | 100 | | | KSPS |
| APERTURE | Aperture Delay | | | 4 | | ns |
| JITTER | Aperture Jitter | | | 50 | | ps |
| Reference Output | | | | | | |
| RFRNG | Range | Typical accuracy \pm TBD% | | 2.5 | | V |
| RFTC | Internal Reference Drift | | | 10 | | ppm/ $^{\circ}C$ |
| Programmable Gain Amplifiers | | | | | | |
| AMPGAIN0 | Gain channel 0 | Programmable | 2 | | 64 | V/V |
| VVO_I0 | Input level 0 | Differential, with gain of 64 | | 14 | 20 | mV _p |
| AMPGAIN1 | Gain channel 1 | Programmable | 2 | c | 8 | V/V |
| VV1 | Input level 1 | Differential, with gain of 6 | | 150 | 212 | mV _p |
| AMPOFFED | Offset error drift | | -20 | | 20 | μV |
| AMPGAINED | Gain error drift | | -0.1 | | 0.1 | % |
| AMPTHD | Total harmonic distortion | | | TBD | | |
| Temperature Sensor | | | | | | |
| TEMPAERR | Absolute Error (trimmed) | | -5 | | +5 | $^{\circ}C$ |
| TEMPRERR | Relative Error (trimmed) | | -3 | | +3 | $^{\circ}C$ |
| TEMPRNG | Temperature Range | | -40 | | 85 | $^{\circ}C$ |
| TEMPRES | Resolution | | | 0.75 | | $^{\circ}C/LSB$ |
| Internal Oscillator | | | | | | |
| OSCFREQ | Frequency | | | 10 | | MHz |
| OSCERROR | Relative Error | | -10 | | +10 | % |
| Over Current | | | | | | |
| OVCURRD LAY | Reaction Time | From chip input to output | | | 2 | μs |
| OVCURR ROR | Relative Error | For threshold lower than 50mV | -20 | | +20 | % |
| | | For threshold higher than 50mV | -10 | | +10 | |
| Under Voltage Lock Out | | | | | | |
| UVLOHI | High Threshold | | | 2.85 | | V |
| UVLOHYST | Hysteresis | | | 0.1 | | V |
| Digital Inputs | | | | | | |
| V _{IH} | Input High Voltage | | 0.7xDVDD | | | V |
| V _{IL} | Input Low Voltage | | | | 0.3xDVDD | V |
| I _{IN} | Input Current | V _{IN} =0V or DVDD | -1 | | +1 | μA |
| C _{IN} | Input Capacitance | | | 15 | | pF |
| Digital Outputs | | | | | | |
| V _{OH} | Output High Voltage | I _{SOURCE} = 200 μA ; DVDD = 3 to 3.6V | DVDD - 0.2 | | | V |
| V _{OL} | Output Low Voltage | I _{SINK} = 200 μA | | | 0.4 | V |

Table 4. Block Electrical Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------|-------------------------|---|------------------|-----|-----|-------|
| Coding | Output Coding | | Two's complement | | | |
| Power Requirements | | | | | | |
| V _{DD} | Positive Supply Voltage | | 3 | | 3.6 | V |
| I _{DD} | | AVDD = 3V, f _{SAMPLE} = 100ksps Input amplifier OFF | | 650 | | μA |
| | | AVDD = 3V, f _{SAMPLE} = 100ksps Input amplifier ON | | | 5 | mA |
| | | Full shutdown mode (Off mode) | | | 1 | μA |

7.1 Operating Modes

When the supply voltage is below the threshold V_{POR} , the AS8002 is in Reset mode. Once the supply voltage is higher than V_{POR} , the AS8002 goes into Off mode during its initialization time t_{INIT} . In this mode, the current consumption is reduced and only the Control register can be read or written. Once the register bit `chip_en` has been set to 1, the chip goes into On mode and can be normally used after t_{WAKEUP} . The chip can go immediately back to Off mode by setting `chip_en` to 0.

Table 5. Characteristics

| Parameter | Description | Min | Max | Unit |
|--------------|-----------------------|-----|-----|---------|
| V_{POR} | POR threshold voltage | | 2.6 | V |
| t_{INIT} | Initialization time | | 3 | ms |
| t_{WAKEUP} | Wake up time | | 300 | μ s |

7.2 SPI Interface

The 16-bit SPI interface enables read / write access to the register blocks and is compatible to a standard micro controller interface, using SPI Mode 3 (SCLK initial state = high, data latched with rising edge of SCLK).

The SPI module is active as soon as pin `SCSB` is pulled low. The AS8002 is then ready to read the 8-bit SPI address on the `SDI` input with every rising edge of `SCLK` and writes on its `SDO` output with the falling edge of `SCLK`. After 16 clock cycles `SCSB` has to be set back to high status in order to reset the interface for the next read/write cycle.

The address is split into an upper 7 bit address (`addr[0...6]`) and a lower 8th bit (`R/W`) containing the read/write information.

Writing data to the AS8002 is established by setting the `R/W` bit to 0. The 8 bits following this bit on `SDI` contain the data to be written into the address specified in the first 8 bits.

Reading data is established by setting the `R/W` bit to 1. The 8 bits following this bit on `SDO` contain the data from the address specified in the first 8 bits on `SDI`.

7.3 SPI Interface Data Transfer Protocol

Figure 4. Write Mode

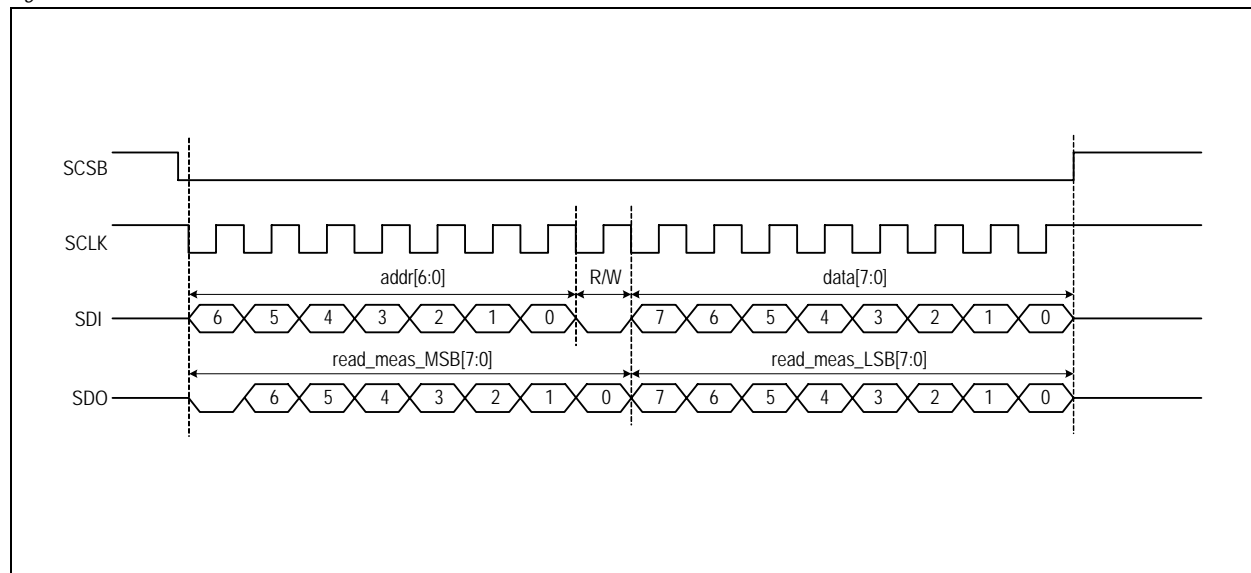
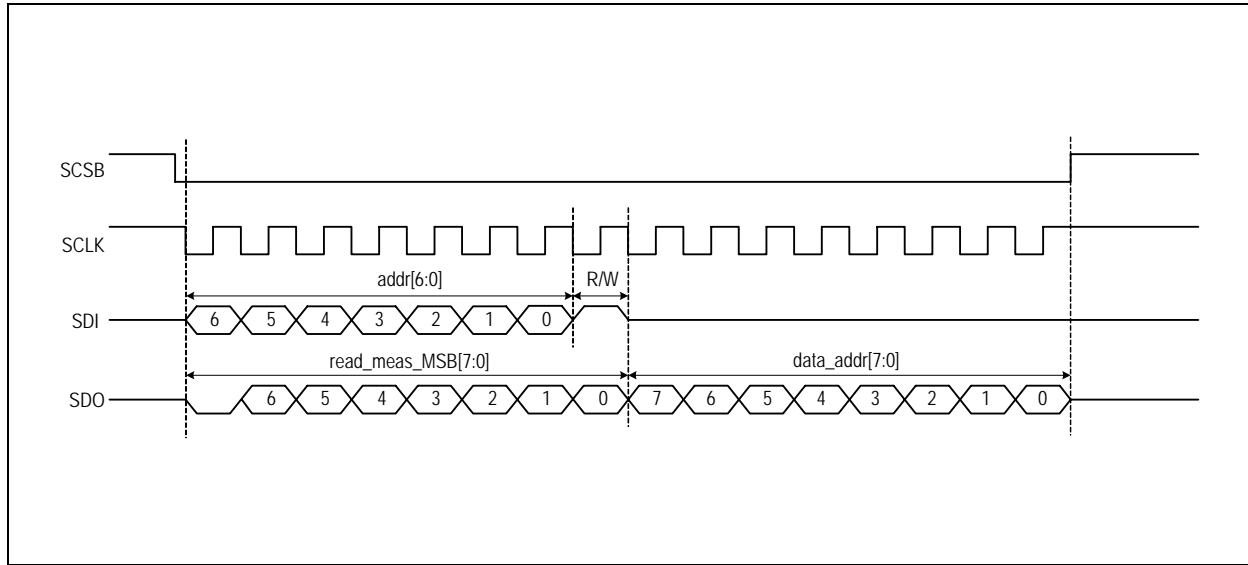


Figure 5. Read Mode



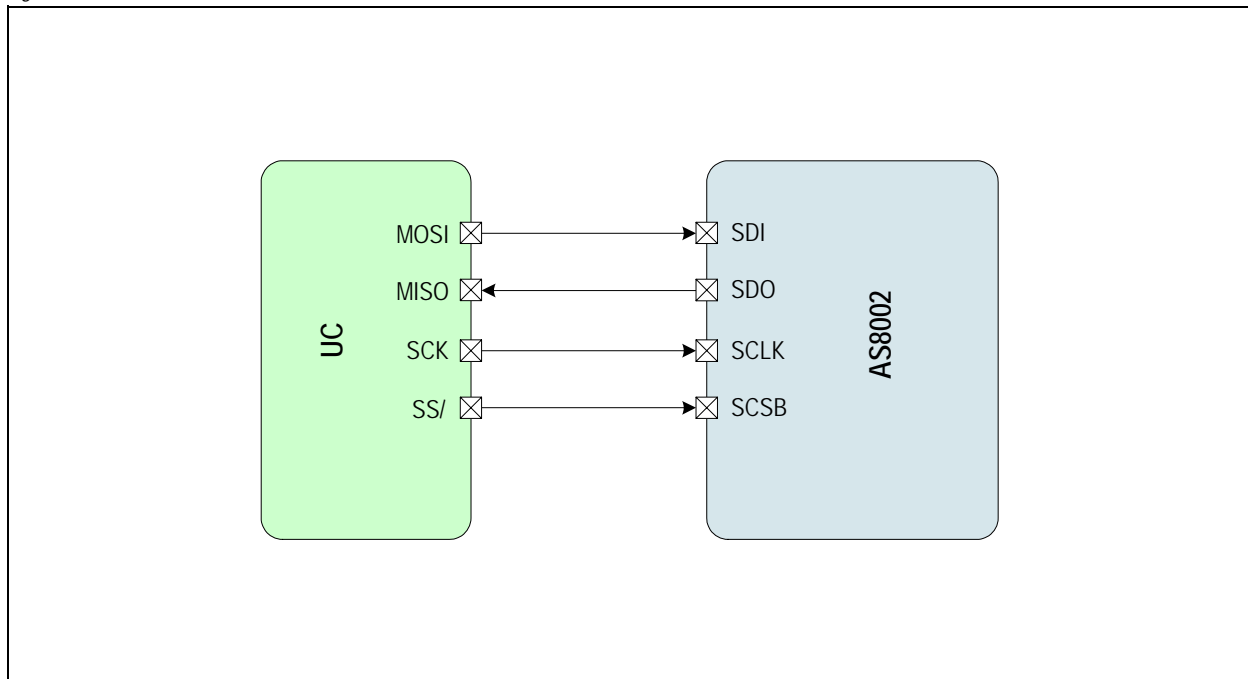
The interface of the AS8002 corresponds to a 4-wire SPI where each data transfer is composed of 16 bits. Each 16-bit transfer of the SDI is divided into a 7-bit address word indicating the target register, one R/W bit indicating the operation to be done and a 8-bit word data indicating the data to be written.

The data transferred in SDO is also composed of 16 bits. These can be divided into the 8 MSBs which correspond to the 8 MSBs of the last conversion run by the ADC plus 8 LSBs which clock out the data that has been requested by the SDI in that same cycle. This allows for a given read register to be addressed and read in the same 16-bit transfer.

7.4 SPI Hardware Connection

Figure 6 shows a basic interconnection diagram of an AS8002 device with a host controller. Data transmission is enabled with signal SCSB (SS/), the serial clock is applied at pin SCLK (SCK). Data is shifted into the AS8002 via signal SDI (MOSI) and read from the AS8002 via signal SDO (MISO).

Figure 6. AS8002 and the Controller



7.5 SPI Timing

Figure 7. Timing Diagram

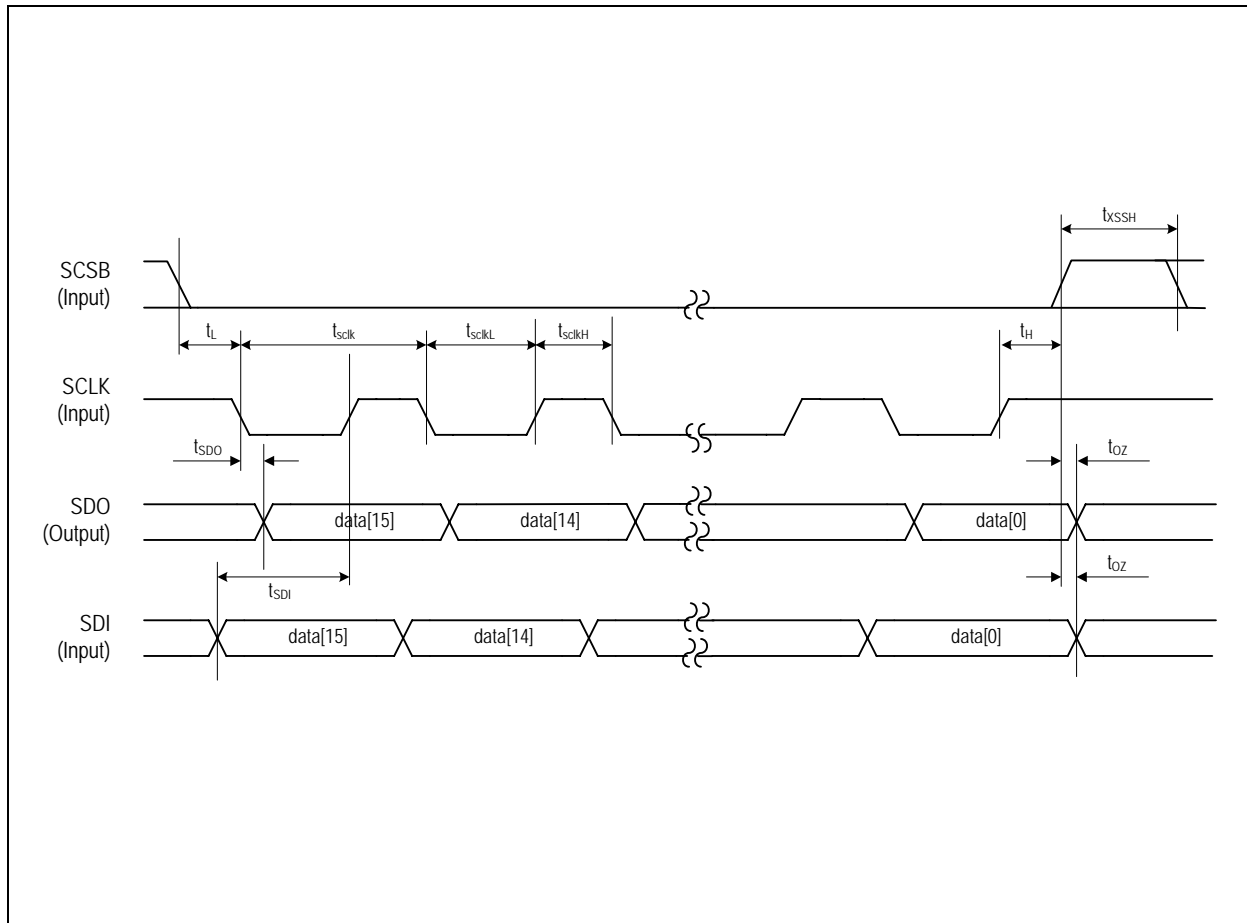


Table 6. Timing Characteristics

| Parameter | Description | Min | Max | Unit |
|-------------|---|----------------|-----|------|
| t_L | Time between SCSB falling edge and SCK rising edge | 350 | | ns |
| t_{SCLK} | Serial clock period | 100 | | ns |
| t_{SCLKL} | Low period of serial clock | 50 | | ns |
| t_{SCLKH} | High period of serial clock | 50 | | ns |
| t_H | Time between last falling edge of SCK and rising edge of SCSB | $t_{SCLK} / 2$ | | ns |
| t_{XSSH} | High time of SCSB between two transmissions | 350 | | ns |
| t_{SDI} | Data input valid to rising clock edge | 20 | | ns |
| t_{SDO} | SCLK falling edge to data output valid | | 20 | ns |

Note: The data on SDO initially reflects the data corresponding to the previous command on SDI. Hence, in write mode, the full 16-bit data of a measurement can be read.

7.6 Measurement Example

The following example shows a simple way to alternately read the voltage and current values:

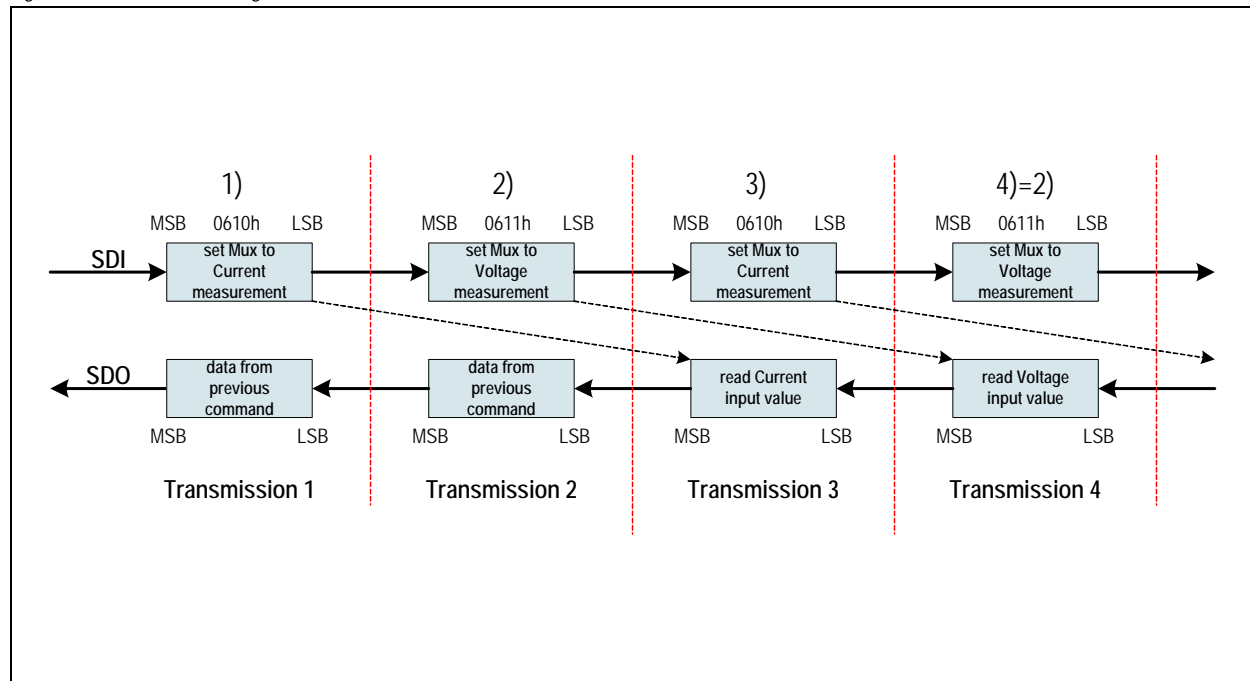
Bits [b2:b0] in Addr 03h control the ADC input multiplexer:

| Name | Addr | Default | Content | | | | | | | |
|-------------------|------|---------|---------|----|----|--------|----|----|--|----|
| | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Input Multiplexer | 03h | 00h | | | | adc_en | | | mux_sel[2:0] 0: Current channel PGA output 1: Voltage channel PGA output | |

- Select the Current channel input (IOM, IOP) : 0610h
 - Set the Address [A6:A0] to 03h,
 - Set the R/W bit to 0 (write mode) and the data to **10h** (adc_en = 1, mux_sel = 0)
 - In parallel to writing the 16-bit data on SDI, a set of 16-bit data can be read on SDO, which contains the data from the second to last command.
- Select the Voltage channel input (V1M, V1P) : 0611h
 - Set the Address [A6:A0] to 03h,
 - Set the R/W bit to 0 (write mode) and the data to **11h** (adc_en = 1, mux_sel = 1)
 - In parallel to writing the 16-bit data on SDI, a set of 16-bit data can be read on SDO, which contains the data from the second to last command.
- Change the input multiplexer back to Current channel input (IOM, IOP) : 0610h
 - Repeat the sequence 1 above: addr = 03h, data = 10h,
 - The 16-bit current input data from the second to last invoked command (1 above) can be read on SDO.
- Loop sequences 2 and 3

Note: In sequence 2, the 16-bit voltage input data from the second to last command can be read on SDO.

Figure 8. Measurement Diagram



Note: The 16-bit input data from the voltage and current measurements contain the ADC data in the lower 12 bits and two status bits in the upper 4 bits (see Register Map Table on page 15).

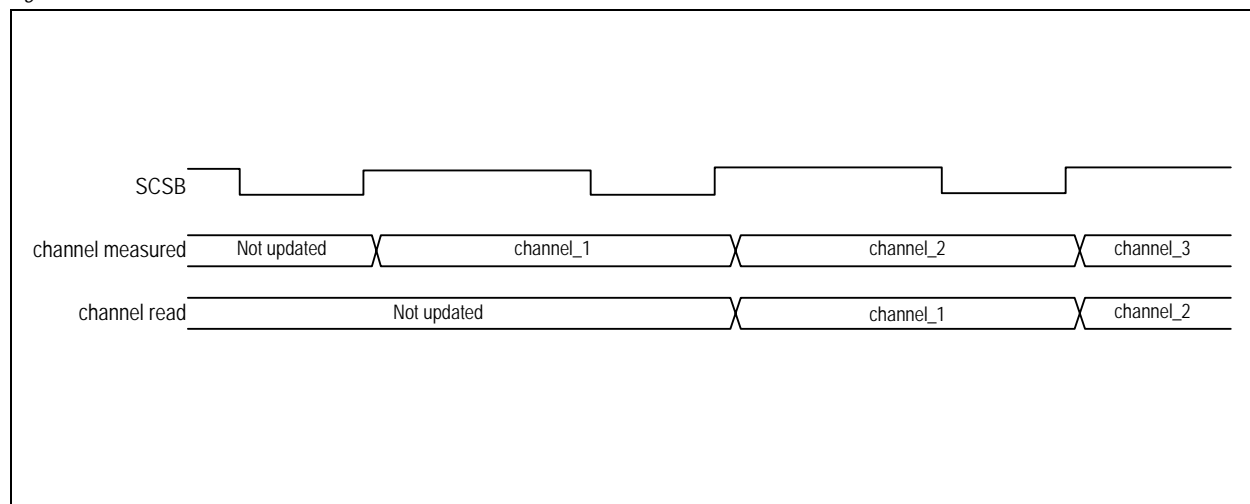
Table 7. Current and Voltage Measurements

| Name | Content | | | | |
|---------------------|---------|------------------|--------------------|-----|-----------|
| | b15 | b14 | b13 | b12 | b11:b0 |
| Current Measurement | 0 | warning_detected | interrupt_detected | X | curr_meas |
| Voltage Measurement | 0 | warning_detected | interrupt_detected | X | volt_meas |

7.7 Measurement Control and Calibration

The conversion starts on SCSB falling edge when `adc_en` is a 1. The value of the result of the conversion can be read at the next SPI write command 10µs later.

Figure 9. ADC Burst Mode



Read_meas will be transferred to the Current, Voltage or Auxiliary measurement upon `mux_sel[2:0]` value – `curr_meas`, `volt_meas` or `aux_meas`.

Calibration is done according to the formulas:

For current channel:

$$read_meas = adc_meas * (1024 + pga_curr_gain_cal) / 1024 \quad (EQ 1)$$

For voltage channel:

$$read_meas = adc_meas * (1024 + pga_volt_gain_cal) / 1024 \quad (EQ 2)$$

For auxiliary channel:

$$read_meas = adc_meas * (1024 + aux_gain_cal) / 1024 \quad (EQ 3)$$

Note: The Raw ADC results are also available in the registers and are called `adc_meas[11:0]`

7.8 Interrupts

When an over current, an under voltage or an over temperature occurs the bit `warning_detected` is set to 1.

The interrupt state is present on `interrupt_detected` and on the pin XINT.

The statuses are available in the register Interrupt Status. It contains the bits `over_current_int_en`, `under_voltage_int_en`, `over_temp_int_en`.

The generation of the interrupt can be enabled or disabled in the register "Interrupt Enable". It contains the bits `over_current_int_i`, `under_voltage_int_i`, `over_temp_int_i`.

Values of the register **Interrupt Status** are kept until this register is read.

7.9 Register Map Table

Table 8. Register Map

| Name | Addr | Default | Content | | | | | | | |
|------------------------------------|------|---------|-------------------------|----------------------------|-------------------------|--------------------|-----------------|----------------------------------|------------------------------|-------------------------------|
| | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Control | 01h | 00h | | over_ current_ annel | over_ current_ en | adc_ref_ en | pga_ volt_en | pga_ curr_en | temp_ sensor_ en | chip_en |
| PGA Gain | 02h | 00h | pga_volt_gain[1:0] | | | pga_curr_gain[4:0] | | | | |
| Input Multiplexer | 03h | 00h | | | | adc_en | | mux_sel[2:0] | | |
| Over Temperature Threshold | 04h | FFh | over_temp_thres[7:0] | | | | | | | |
| Interrupt Enable | 05h | 00h | | | | | | over_ current_ int_ _en | under_ voltage_ int_en | over_ temp_ int_ _en |
| Over Current Range | 06h | FFh | over_current_range[7:0] | | | | | | | |
| | | | | | | | | | | |
| Current Measurement MSB | 10h | 00h | 0 | warning_ detected | interrupt_ detected | X | curr_meas[11:8] | | | |
| Current Measurement LSB | 11h | 00h | curr_meas[7:0] | | | | | | | |
| Voltage Measurement MSB | 12h | 00h | 0 | warning_ detected | interrupt_ detected | X | volt_meas[11:8] | | | |
| Voltage Measurement LSB | 13h | 00h | volt_meas[7:0] | | | | | | | |
| Auxiliary Measurement MSB | 14h | 00h | 0 | warning_ detected | interrupt_ detected | X | aux_meas[11:8] | | | |
| Auxiliary Measurement LSB | 15h | 00h | aux_meas[7:0] | | | | | | | |
| Temperature Measurement | 16h | 00h | temp[7:0] | | | | | | | |
| Interrupt Status | 17h | 00h | | | | | | over_ current_ i | under_ voltage_ i | over_ temp_ i |
| ASIC ID 1 | 18h | 02h | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| ASIC ID 2 | 19h | 5Xh | 0 | 1 | 0 | 1 | X | X | X | X |
| Raw ADC Results MSB | 1Ah | 00h | 0 | warning_ detected | interrupt_ detected | X | adc_meas[11:8] | | | |
| Raw ADC Results LSB | 1Bh | 00h | adc_meas[7:0] | | | | | | | |
| | | | | | | | | | | |
| PGA Current Gain Calibration | 3Ah | 00h | pga_curr_gain_cal[7:0] | | | | | | | |
| PGA Voltage Gain Calibration | 3Bh | 00h | pga_volt_gain_cal[7:0] | | | | | | | |
| Auxiliary Channel Gain Calibration | 3Ch | 00h | aux_gain_cal[7:0] | | | | | | | |

Note: Highlighted registers are Read only registers (bits).

7.10 Register Description

Table 9. 01h

| Address: 01h | | Control Register | | |
|-----------------|----------------------|--|--------|---|
| | | Controls the power on and off of the internal blocks | | |
| Bit | Bit Name | Default | Access | Description |
| 0 | chip_en | 0h | R/W | 0: Chip in complete power off 1: Chip on |
| 1 | temp_sensor_en | 0h | R/W | 0: Temperature sensor disabled 1: Temperature sensor enabled |
| 2 | pga_curr_en | 0h | R/W | 0: Current channel PGA disabled 1: Current channel PGA enabled |
| 3 | pga_volt_en | 0h | R/W | 0: Voltage channel PGA disabled 1: Voltage channel PGA enabled |
| 4 | adcref_en | 0h | R/W | 0: Internal ADC reference voltage off 1: Internal ADC reference voltage on Note: This bit must be set to allow ADC measurements. |
| 5 | over_current_en | 0h | R/W | 0: Over current detector disabled 1: Over current detector enabled |
| 6 | over_current_channel | 0h | R/W | 0: Over current detector connected to inputs IOP_VOP and IOM_VOM 1: Over current detector connected to inputs V2P and V2M |

Table 10. 02h

| Address: 02h | | PGA Gain Register | | |
|-----------------|---------------|---|--------|---|
| | | Controls the gain of the current and voltage channel PGAs | | |
| Bit | Bit Name | Default | Access | Description |
| 4:0 | pga_curr_gain | 00h | R/W | Gain for current channel is given by the formula: $2^{pga_curr_gain+2}$ (EQ 4) |
| 7:6 | pga_volt_gain | 0h | R/W | Gain for voltage channel is given by the formula: $2^{pga_volt_gain+2}$ (EQ 5) |

Table 11. 03h

| Address: 03h | | Input Multiplexer Register | | |
|-----------------|----------|---|--------|---|
| | | Controls the ADC and select the channel to be converted | | |
| Bit | Bit Name | Default | Access | Description |
| 2:0 | mux_sel | 00h | R/W | Select the input to be converted: 0: Current channel PGA output 1: Voltage channel PGA output 2: V2P and V2M 3: AVDD and AVSS 4: IOP_VOP and IOM_VOM 5: V1P and V1M 6: Reserved 7: Reserved |
| 4 | adc_en | 0h | R/W | Enable the ADC conversion that will start on the next SCSB falling edge |

Table 12. 04h

| Address: 04h | | Over Temperature Threshold Register | | |
|-----------------|-----------------|--|--------|--|
| | | Set the over temperature threshold value | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | over_temp_thres | FFh | R/W | Over temperature detection is triggered when temp value is higher than over_temp_thres |

Table 13. 05h

| Address: 05h | | Interrupt Enable Register | | |
|-----------------|----------------------|-----------------------------------|--------|---|
| | | Separately enables the interrupts | | |
| Bit | Bit Name | Default | Access | Description |
| 0 | over_temp_int_en | 0h | R/W | 0: Interrupt due to over temperature is disabled 1: Interrupt due to over temperature is enabled |
| 1 | under_voltage_int_en | 0h | R/W | 0: Interrupt due to under voltage is disabled 1: Interrupt due to under voltage is enabled |
| 2 | over_current_int_en | 0h | R/W | 0: Interrupt due to over current is disabled 1: Interrupt due to over current is enabled |

Table 14. 06h

| Address: 06h | | Over Current Range Register | | |
|-----------------|--------------------|---|--------|---|
| | | Set the over current comparators absolute threshold voltage | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | over_current_range | FFh | R/W | The threshold voltage is given by the formula: $over_current_range * 1m \quad (EQ 6)$ Where: over_current_range should be higher than 10h |

Table 15. 10h

| Address: 10h | | Current Measurement MSB Register | | |
|-----------------|--------------------|---|--------|--|
| | | Gives measured value of current (MSB) and status of warnings and interrupts | | |
| Bit | Bit Name | Default | Access | Description |
| 3:0 | curr_meas[11:8] | 0h | R | MSB of current channel measurement, value is given as 2's complement number by the formula: $I = curr_meas * 1.22m / (Rshunt * curr_gain) \quad (EQ 7)$ |
| 5 | interrupt detected | 0h | R | Same value as XINT (complemented) 0: No interrupt detected 1: Interrupt is detected |
| 6 | warning detected | 0h | R | Over temperature, under voltage or over current detected 0: No warning detected 1: Warning detected |

Table 16. 11h

| Address: 11h | | Current Measurement LSB Register | | |
|-----------------|----------------|---------------------------------------|--------|--|
| | | Gives measured value of current (LSB) | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | curr_meas[7:0] | 0h | R | LSB of current channel measurement, value is given as 2's complement number by the formula: $I = \text{curr_meas} * 1.22\text{m} / (\text{Rshunt} * \text{curr_gain})$ (EQ 8) |

Table 17. 12h

| Address: 12h | | Voltage Measurement MSB Register | | |
|-----------------|--------------------|---|--------|--|
| | | Gives measured value of voltage (MSB) and status of warnings and interrupts | | |
| Bit | Bit Name | Default | Access | Description |
| 3:0 | volt_meas[11:8] | 0h | R | MSB of voltage channel measurement, value is given as 2's complement number by the formula: $\text{volt_meas} * 1.22\text{m} / \text{volt_gain}$ (EQ 9) |
| 5 | interrupt detected | 0h | R | Same value as XINT (complemented) 0: No interrupt detected 1: Interrupt is detected |
| 6 | warning detected | 0h | R | Over temperature, under voltage or over voltage detected 0: No warning detected 1: Warning detected |

Table 18. 13h

| Address: 13h | | Voltage Measurement LSB Register | | |
|-----------------|----------------|---------------------------------------|--------|---|
| | | Gives measured value of voltage (LSB) | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | volt_meas[7:0] | 0h | R | LSB of voltage channel measurement, value is given as 2's complement number by the formula: $\text{volt_meas} * 1.22\text{m} / \text{volt_gain}$ (EQ 10) |

Table 19. 14h

| Address: 14h | | Auxiliary Measurement MSB Register | | |
|-----------------|--------------------|---|--------|--|
| | | Gives measured value of auxiliary channel (MSB) and status of warnings and interrupts | | |
| Bit | Bit Name | Default | Access | Description |
| 3:0 | aux_meas[11:8] | 0h | R | MSB of auxiliary channel measurement, value is given as 2's complement number by the formula: $\text{aux_meas} * 1.22\text{m}$ (EQ 11) |
| 5 | interrupt detected | 0h | R | Same value as XINT (complemented) 0: No interrupt detected 1: Interrupt is detected |
| 6 | warning detected | 0h | R | Over temperature, under auxiliary or over auxiliary detected 0: No warning detected 1: Warning detected |

Table 20. 15h

| Address: 15h | | Auxiliary Measurement LSB Register | | |
|-----------------|---------------|---|--------|---|
| | | Gives measured value of auxiliary channel (LSB) | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | aux_meas[7:0] | 0h | R | LSB of auxiliary channel measurement, value is given as 2's complement number by the formula: $\text{aux_meas} * 1.22\text{m}$ (EQ 12) |

Table 21. 16h

| Address: 16h | | Temperature Measurement Register | | |
|-----------------|----------|-------------------------------------|--------|---|
| | | Gives measured value of temperature | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | temp | 0h | R | Temperature value (in °C) is given by the formula: $92 + \text{temp} * 3/4$ (EQ 13) |

Table 22. 17h

| Address: 17h | | Interrupt Status Register | | |
|-----------------|-----------------|---------------------------------------|--------|--|
| | | Gives status of each interrupt source | | |
| Bit | Bit Name | Default | Access | Description |
| 0 | over_temp_i | 0h | R | 0: over temperature not detected 1: over temperature detected |
| 1 | under_voltage_i | 0h | R | 0: under voltage not detected 1: under voltage detected |
| 2 | over_current_i | 0h | R | 0: over current not detected 1: over current detected |

Table 23. 18h

| Address: 18h | | ASIC ID 1 Register | | |
|-----------------|----------|------------------------------|--------|---------------------|
| | | Provides Chip identification | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | asic_id | 02h | R | Chip identification |

Table 24. 19h

| Address: 19h | | ASIC ID 2 Register | | |
|-----------------|--------------|------------------------------|--------|--|
| | | Provides chip version number | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | asic_version | 5Xh | R | 50h: Chip version 0 51h: Chip version 1 |

Table 25. 1Ah

| Address: 1Ah | | Raw ADC Results MSB Register | | |
|-----------------|--------------------|---|--------|--|
| | | Gives measured value of the ADC (MSB) and status of warnings and interrupts | | |
| Bit | Bit Name | Default | Access | Description |
| 3:0 | adc_meas[11:8] | 0h | R | MSB of raw ADC measurement, value is given as 2's complement number by the formula: $\text{adc_meas} * 1.22\text{m}$ (EQ 14) |
| 5 | interrupt detected | 0h | R | Same value as XINT (complemented) 0: No interrupt detected 1: Interrupt is detected |
| 6 | warning detected | 0h | R | Over temperature, under voltage or over current detected 0: No warning detected 1: Warning detected |

Table 26. 1Bh

| Address: 1Bh | | Raw ADC Results LSB Register | | |
|-----------------|---------------|---------------------------------------|--------|--|
| | | Gives measured value of raw ADC (LSB) | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | adc_meas[7:0] | 0h | R | LSB of raw ADC measurement, value is given as 2's complement number by the formula: $\text{adc_meas} * 1.22\text{m}$ (EQ 15) |

Table 27. 3Ah

| Address: 3Ah | | PGA Current Gain Calibration Register | | |
|-----------------|-------------------|---|--------|--|
| | | Set value of correction coefficient for current measurement | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | pga_curr_gain_cal | 00h | R/W | Correct the measured current value multiplying it by the following factor, where pga_curr_gain_cal is a number defined as 2's complement: $(1024 + \text{pga_curr_gain_cal}) / 1024$ (EQ 16) |

Table 28. 3Bh

| Address: 3Bh | | PGA Voltage Gain Calibration Register | | |
|-----------------|-------------------|---|--------|--|
| | | Set value of correction coefficient for voltage measurement | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | pga_volt_gain_cal | 00h | R/W | Correct the measured voltage value multiplying it by the following factor, where pga_volt_gain_cal is a number defined as 2's complement: $(1024 + \text{pga_volt_gain_cal}) / 1024$ (EQ 17) |

Table 29. 3Ch

| Address: 3Ch | | Auxiliary Channel Gain Calibration Register | | |
|-----------------|--------------|---|--------|--|
| | | Set value of correction coefficient for auxiliary measurement | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | aux_gain_cal | 00h | R/W | Correct the measured value of the auxiliary channel multiplying it by the following factor, where aux_gain_cal is a number defined as 2's complement: $(1024 + \text{aux_gain_cal}) / 1024$ (EQ 18) |

8 Application Information

Table 30 provides examples of Gain selection of Channel 1 for different shunt resistors and maximum RMS currents.

Table 30. Gain Selection

| Shunt Resistor Value | Sensing RMS Current (A) | Recommended Linear Gain for Channel 1 for ADC to work in 80% of dynamic range |
|----------------------|-------------------------|---|
| 7.5 mΩ | 1.5 | Gain1 = 64 |
| 10 mΩ | 1.5 | Gain1 = 48 |
| 5 mΩ | 3 | Gain1 = 48 |
| 7.5 mΩ | 3 | Gain1 = 32 |
| 10 mΩ | 3 | Gain1 = 24 |
| 5 mΩ | 6 | Gain1 = 24 |
| 7.5 mΩ | 6 | Gain1 = 16 |
| 10 mΩ | 6 | Gain1 = 12 |

8.1 Application Hints

Grounding and Layout. The analog and digital supplies of the AS8002 (AVDD, DVDD, AVSS, DVSS) are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The printed circuit board (PCB) that houses the AS8002 should be designed such that the analog and digital sections are separated and confined to certain areas on the board. This design facilitates the use of ground planes that can be easily separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. All VSS pins of the AS8002 should be sunk in the ground plane. Digital and analog ground planes should be joined in only one spot. If the AS8002 is in a system where multiple devices require an AVSS and DVSS connection, this connection should still be made at one point only; a star ground point that should be established as close as possible to the ground pins on the AS8002.

Avoid running digital lines under the device as this couples noise into the chip. However, the analog ground plane should be allowed to run under the AS8002 to avoid noise coupling. The power supply lines to the AS8002 should use as large trace width as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Likewise, the positive supply pins AVDD and DVDD should be connected only at one common star point close the output of the power supply. For best performance of the analog blocks of the AS8002, it is important to have a clean, noise-free supply voltage at AVDD.

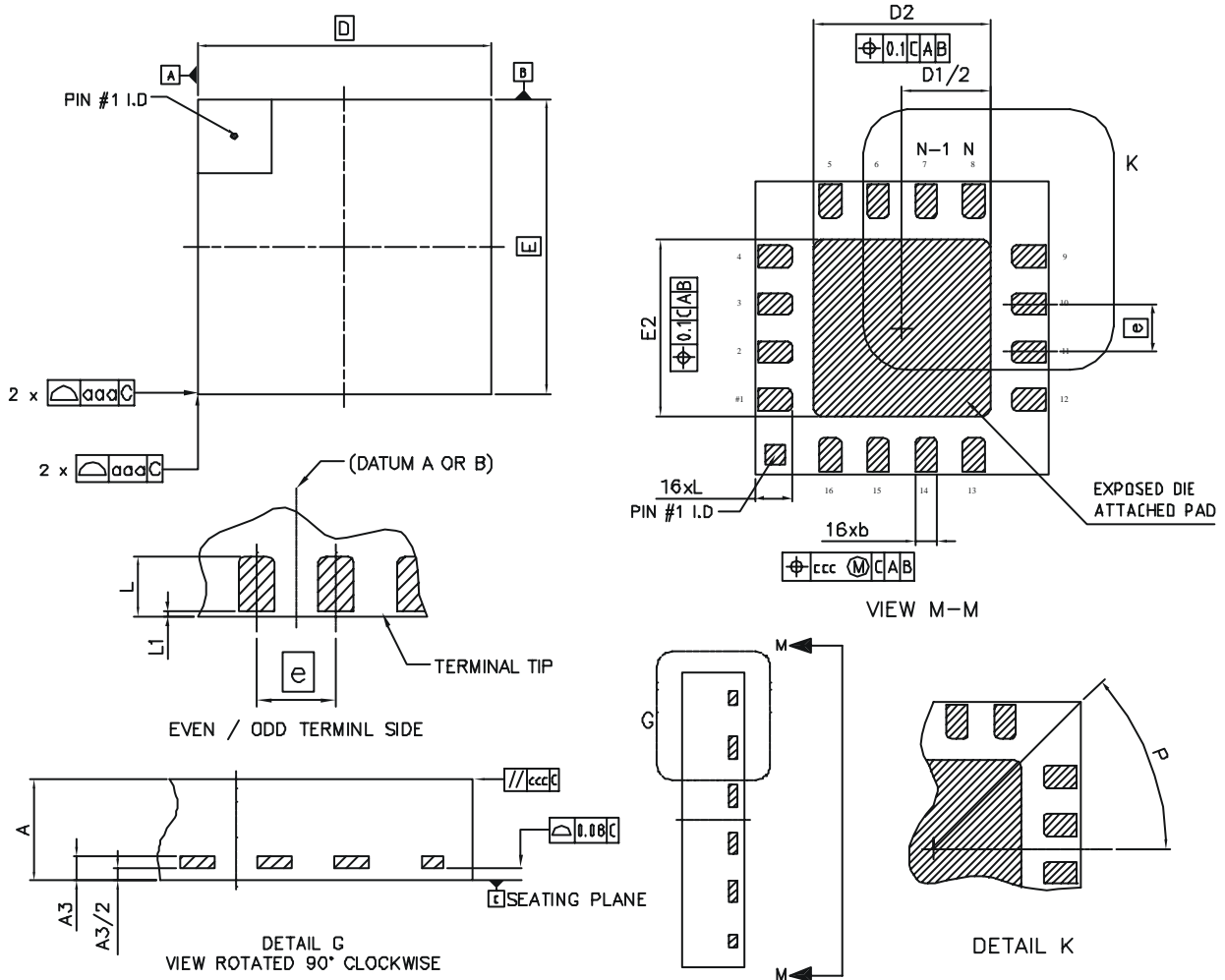
To avoid radiating noise to other sections of the board, fast switching signals, such as clocks, should be shielded with digital ground, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feedthrough within the board, traces on opposite sides of the board should run at right angles to each other. A microstrip technique is the best method but is not always possible with a double sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the opposite side.

Good decoupling is also important. All analog supplies should be decoupled with 10μF ceramic capacitors in parallel with 0.1μF capacitors to GND. Refer to [Typical Application Circuit \(page 9\)](#). To achieve the best results from these decoupling components, they must be placed as close as possible to the device. The 0.1μF capacitors should have low effective series resistance (ESR) and low effective series inductance (ESI), such as common ceramic types or surface-mount types. These low ESR and ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

9 Package Drawings and Markings

The device is available in a 16-pin QFN (4x4x0.9mm) package.

Figure 10. 16-pin QFN (4x4x0.9mm) Package



| Symbol | Min | Typ | Max |
|--------|-----------|------|------|
| A | 0.75 | 0.85 | 0.95 |
| A1 | 0.203 REF | | |
| b | 0.25 | 0.30 | 0.35 |
| D | 4.00 BSC | | |
| E | 4.00 BSC | | |
| D2 | 2.30 | 2.40 | 2.50 |
| E2 | 2.30 | 2.40 | 2.50 |

| Symbol | Min | Typ | Max |
|--------|----------|------|------|
| e | 0.65 BSC | | |
| L | 0.40 | 0.50 | 0.60 |
| L1 | | | 0.10 |
| P | 45° BSC | | |
| aaa | 0.15 | | |
| ccc | 0.10 | | |

Notes:

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters, angles are in degrees.
3. Dimension b applies to metallized terminal and is measured between 0.25 and 0.30mm from terminal tip. Dimension $L1$ represents terminal full back from package edge up to 0.1mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

Revision History

| Revision | Date | Owner | Description |
|----------|--------------|-------|---|
| 1.0 | 14 May, 2010 | jja | Initial revision |
| 1.1 | 25 Aug, 2010 | spo | Updated the following in Register Map (page 15) : 1) Register bit b4 at address 01 (previously under_voltage_en) is now adc_ref_en 2) ASIC ID 2 register value is now 5Xh |
| | | | |

Note: Typos may not be explicitly mentioned under revision history.

10 Ordering Information

The devices are available as the standard products shown in [Table 31](#).

Table 31. Ordering Information

| Ordering Code | Description | Delivery Form | Package |
|---------------|-----------------------------|--|------------------------|
| AS8002 AQFP | Temperature: -40°C to 125°C | Tape & Reel in Dry Pack; 6000 pieces / reel | 16-pin QFN (4x4x0.9mm) |

Note: All products are RoHS compliant and Pb-free.

Buy our products or get free samples online at ICdirect: <http://www.austriamicrosystems.com/ICdirect>

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