SLAS491F – AUGUST 2005 – REVISED MARCH 2011

- **Low Supply Voltage Range 1.8 V to 3.6 V**
- **Ultralow Power Consumption**
  - **Active Mode: 220 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.5 μA**
  - **Off Mode (RAM Retention): 0.1 μA**
- **Five Power-Saving Modes**
- **Ultrafast Wake-Up From Standby Mode in Less Than 1 μs**
- **16-Bit RISC Architecture, 62.5 ns Instruction Cycle Time**
- **Basic Clock Module Configurations:**
  - **Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to ±1%**
  - **Internal Very Low Power LF Oscillator**
  - **32-kHz Crystal**
  - **External Digital Clock Source**
- **16-Bit Timer_A With Two Capture/Compare Registers**
- **On-Chip Comparator for Analog Signal Compare Function or Slope A/D (MSP430x20x1 only)**
- **10-Bit 200-ksps A/D Converter With Internal Reference, Sample-and-Hold, and Autoscan (MSP430x20x2 only)**
- **16-Bit Sigma-Delta A/D Converter With Differential PGA Inputs and Internal Reference (MSP430x20x3 only)**
- **Universal Serial Interface (USI) Supporting SPI and I2C (MSP430x20x2 and MSP430x20x3 only)**
- **Brownout Detector**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **On-Chip Emulation Logic With Spy-Bi-Wire Interface**
- **Family Members Include:**
  - **MSP430F2001: 1KB + 256B Flash Memory 128B RAM**
  - **MSP430F2011: 2KB + 256B Flash Memory 128B RAM**
  - **MSP430F2002: 1KB + 256B Flash Memory 128B RAM**
  - **MSP430F2012: 2KB + 256B Flash Memory 128B RAM**
  - **MSP430F2003: 1KB + 256B Flash Memory 128B RAM**
  - **MSP430F2013: 2KB + 256B Flash Memory 128B RAM**
- **Available in a 14-Pin Plastic Small-Outline Thin Package (TSSOP), 14-Pin Plastic Dual Inline Package (PDIP), and 16-Pin QFN**
- **For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide***

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1μs.

The MSP430x20xx series is an ultralow-power mixed signal microcontroller with a built-in 16-bit timer, and ten I/O pins. In addition the MSP430x20x1 has a versatile analog comparator. The MSP430x20x2 and MSP430x20x3 have built-in communication capability using synchronous protocols (SPI or I2C), and a 10-bit A/D converter (MSP430x20x2) or a 16-bit sigma-delta A/D converter (MSP430x20x3).

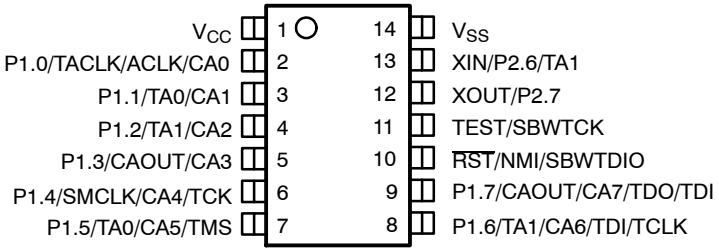
Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system. Stand alone RF sensor front end is another area of application.

AVAILABLE OPTIONS

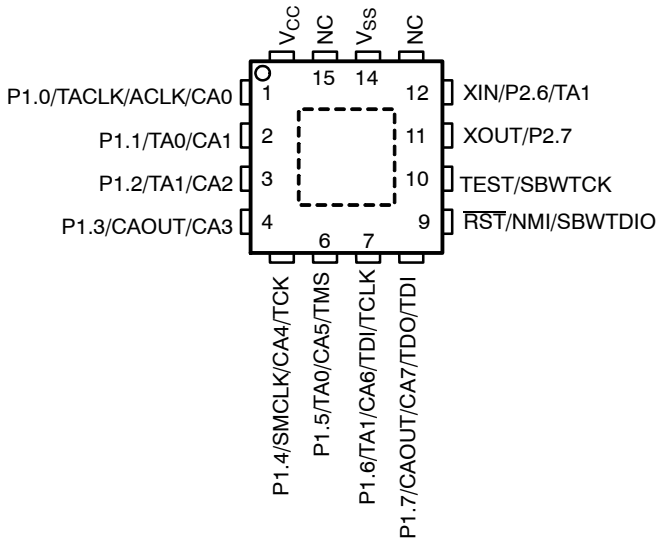
T_A	PACKAGED DEVICES		
	PLASTIC 14-PIN TSSOP (PW)	PLASTIC 14-PIN DIP (N)	PLASTIC 16-PIN QFN (RSA)
–40°C to 85°C	MSP430F2001IPW MSP430F2011IPW MSP430F2002IPW MSP430F2012IPW MSP430F2003IPW MSP430F2013IPW	MSP430F2001IN MSP430F2011IN MSP430F2002IN MSP430F2012IN MSP430F2003IN MSP430F2013IN	MSP430F2001IRSA MSP430F2011IRSA MSP430F2002IRSA MSP430F2012IRSA MSP430F2003IRSA MSP430F2013IRSA
–40°C to 105°C	MSP430F2001TPW MSP430F2011TPW MSP430F2002TPW MSP430F2012TPW MSP430F2003TPW MSP430F2013TPW	MSP430F2001TN MSP430F2011TN MSP430F2002TN MSP430F2012TN MSP430F2003TN MSP430F2013TN	MSP430F2001TRSA MSP430F2011TRSA MSP430F2002TRSA MSP430F2012TRSA MSP430F2003TRSA MSP430F2013TRSA

device pinout, MSP430x20x1

PW or N PACKAGE
(TOP VIEW)



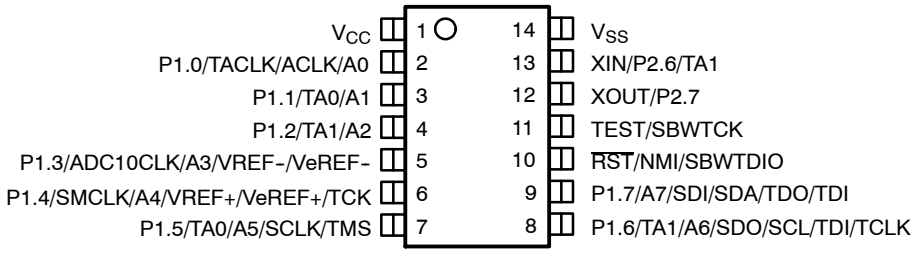
RSA PACKAGE
(TOP VIEW)



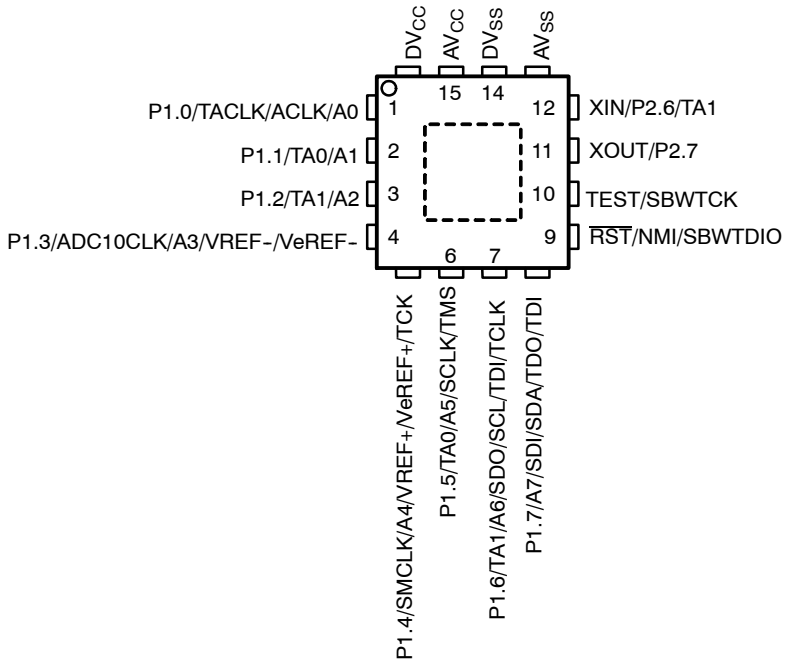
NOTE: See port schematics section for detailed I/O information.

device pinout, MSP430x20x2

PW or N PACKAGE
(TOP VIEW)



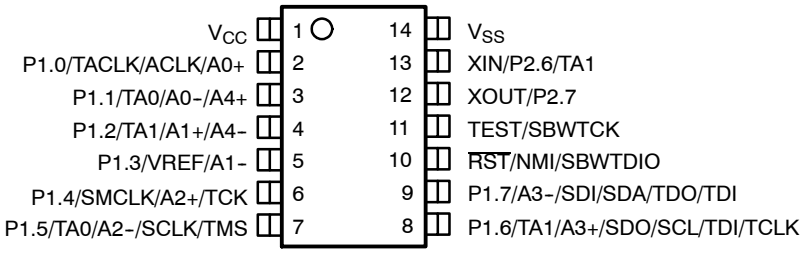
RSA PACKAGE
(TOP VIEW)



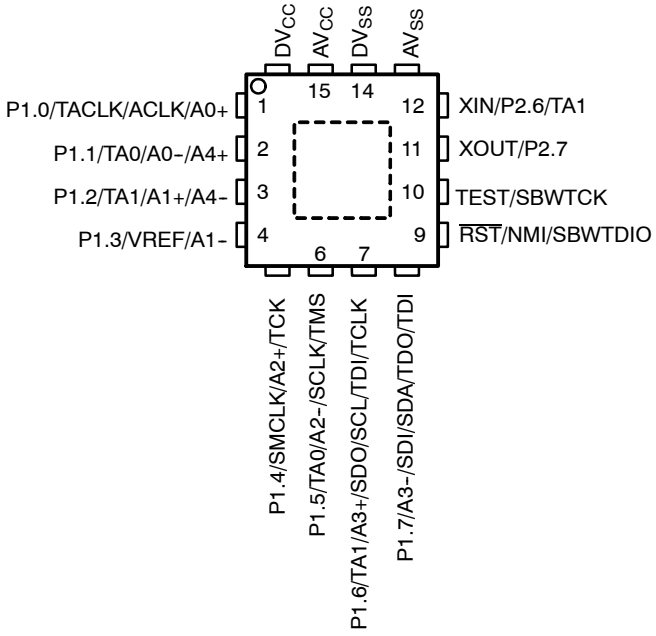
NOTE: See port schematics section for detailed I/O information.

device pinout, MSP430x20x3

PW or N PACKAGE
(TOP VIEW)

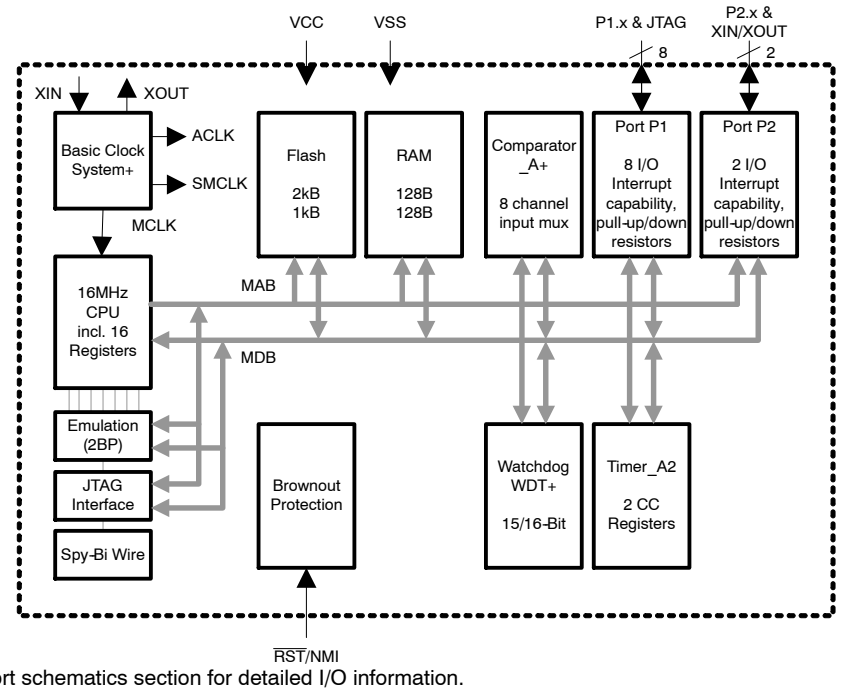


RSA PACKAGE
(TOP VIEW)



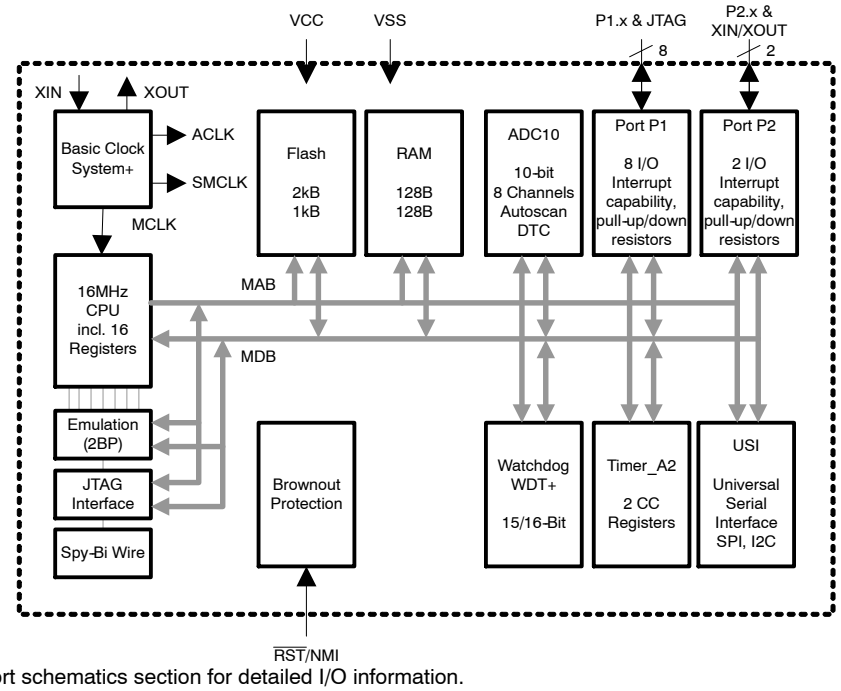
NOTE: See port schematics section for detailed I/O information.

functional block diagram, MSP430x20x1



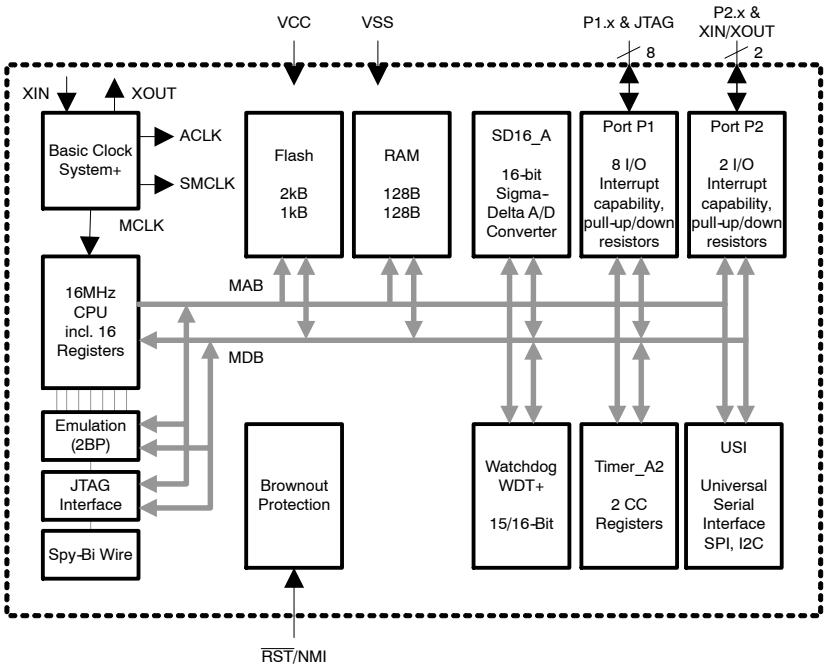
NOTE: See port schematics section for detailed I/O information.

functional block diagram, MSP430x20x2



NOTE: See port schematics section for detailed I/O information.

functional block diagram, MSP430x20x3



NOTE: See port schematics section for detailed I/O information.

Terminal Functions, MSP430x20x1

TERMINAL				DESCRIPTION
NAME	PW or N NO.	RSA NO.	I/O	
P1.0/TACLK/ACLK/CA0	2	1	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input ACLK signal ouput Comparator_A+, CA0 input
P1.1/TA0/CA1	3	2	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output Comparator_A+, CA1 input
P1.2/TA1/CA2	4	3	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output Comparator_A+, CA2 input
P1.3/CAOUT/CA3	5	4	I/O	General-purpose digital I/O pin Comparator_A+, output / CA3 input
P1.4/SMCLK/C4/TCK	6	5	I/O	General-purpose digital I/O pin SMCLK signal output Comparator_A+, CA4 input JTAG test clock, input terminal for device programming and test
P1.5/TA0/CA5/TMS	7	6	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output Comparator_A+, CA5 input JTAG test mode select, input terminal for device programming and test
P1.6/TA1/CA6/TDI/TCLK	8	7	I/O	General-purpose digital I/O pin Timer_A, compare: Out1 output Comparator_A+, CA6 input JTAG test data input or test clock input during programming and test
P1.7/CAOUT/CA7/TDO/TDI†	9	8	I/O	General-purpose digital I/O pin Comparator_A+, output / CA7 input JTAG test data output terminal or test data input during programming and test
XIN/P2.6/TA1	13	12	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin Timer_A, compare: Out1 output
XOUT/P2.7	12	11	I/O	Output terminal of crystal oscillator General-purpose digital I/O pin
$\overline{\text{RST}}$/NMI/SBWTDIO	10	9	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/SBWTCK	11	10	I	Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
V_{CC}	1	16		Supply voltage
V_{SS}	14	14		Ground reference
NC	NA	13, 15		Not connected
QFN Pad	NA	Package Pad	NA	QFN package pad connection to V_{SS} recommended.

† TDO or TDI is selected via JTAG instruction.

NOTE: If XOUT/P2.7 is used as an input, excess current will flow until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

Terminal Functions, MSP430x20x2

TERMINAL				DESCRIPTION
NAME	PW, or N NO.	RSA NO.	I/O	
P1.0/TACLK/ACLK/A0	2	1	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input ACLK signal ouput ADC10 analog input A0
P1.1/TA0/A1	3	2	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output ADC10 analog input A1
P1.2/TA1/A2	4	3	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output ADC10 analog input A2
P1.3/ADC10CLK/ A3/VREF–/VeREF–	5	4	I/O	General-purpose digital I/O pin ADC10 conversion clock output ADC10 analog input A3 Input for negative external reference voltage/negative internal reference voltage output
P1.4/SMCLK/A4/VREF+/VeREF+/ TCK	6	5	I/O	General-purpose digital I/O pin SMCLK signal output ADC10 analog input A4 Input for positive external reference voltage/positive internal reference voltage output JTAG test clock, input terminal for device programming and test
P1.5/TA0/A5/SCLK/TMS	7	6	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output ADC10 analog input A5 USI: external clock input in SPI or I2C mode; clock output in SPI mode JTAG test mode select, input terminal for device programming and test
P1.6/TA1/A6/SDO/SCL/TDI/TCLK	8	7	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1B input, compare: Out1 output ADC10 analog input A6 USI: Data output in SPI mode; I2C clock in I2C mode JTAG test data input or test clock input during programming and test
P1.7/A7/SDI/SDA/TDO/TDI†	9	8	I/O	General-purpose digital I/O pin ADC10 analog input A7 USI: Data input in SPI mode; I2C data in I2C mode JTAG test data output terminal or test data input during programming and test
XIN/P2.6/TA1	13	12	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin Timer_A, compare: Out1 output
XOUT/P2.7	12	11	I/O	Output terminal of crystal oscillator General-purpose digital I/O pin
$\overline{\text{RST}}$/NMI/SBWTDIO	10	9	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/SBWTCK	11	10	I	Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
V_{CC}	1	NA		Supply voltage
V_{SS}	14	NA		Ground reference

† TDO or TDI is selected via JTAG instruction.

NOTE: If XOUT/P2.7 is used as an input, excess current will flow until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

Terminal Functions, MSP430x20x2 (Continued)

TERMINAL				DESCRIPTION
NAME	PW, or N NO.	RSA NO.	I/O	
DV_{CC}	NA	16		Digital supply voltage
AV_{CC}	NA	15		Analog supply voltage
DV_{SS}	NA	14		Digital ground reference
AV_{SS}	NA	13		Analog ground reference
QFN Pad	NA	Package Pad	NA	QFN package pad connection to V_{SS} recommended.

Terminal Functions, MSP430x20x3

TERMINAL				DESCRIPTION
NAME	PW, or N NO.	RSA NO.	I/O	
P1.0/TACLK/ACLK/A0+	2	1	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input ACLK signal ouput SD16_A positive analog input A0
P1.1/TA0/A0–/A4+	3	2	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output SD16_A negative analog input A0 SD16_A positive analog input A4
P1.2/TA1/A1+/A4–	4	3	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output SD16_A positive analog input A1 SD16_A negative analog input A4
P1.3/VREF/A1–	5	4	I/O	General-purpose digital I/O pin Input for an external reference voltage/internal reference voltage output (can be used as mid-voltage) SD16_A negative analog input A1
P1.4/SMCLK/A2+/TCK	6	5	I/O	General-purpose digital I/O pin SMCLK signal output SD16_A positive analog input A2 JTAG test clock, input terminal for device programming and test
P1.5/TA0/A2–/SCLK/TMS	7	6	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output SD16_A negative analog input A2 USI: external clock input in SPI or I2C mode; clock output in SPI mode JTAG test mode select, input terminal for device programming and test
P1.6/TA1/A3+/SDO/SCL/TDI/TCLK	8	7	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1B input, compare: Out1 output SD16_A positive analog input A3 USI: Data output in SPI mode; I2C clock in I2C mode JTAG test data input or test clock input during programming and test
P1.7/A3–/SDI/SDA/TDO/TDI†	9	8	I/O	General-purpose digital I/O pin SD16_A negative analog input A3 USI: Data input in SPI mode; I2C data in I2C mode JTAG test data output terminal or test data input during programming and test

† TDO or TDI is selected via JTAG instruction.

Terminal Functions, MSP430x20x3 (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	PW, or N NO.	RSA NO.		
XIN/P2.6/TA1	13	12	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin Timer_A, compare: Out1 output
XOUT/P2.7	12	11	I/O	Output terminal of crystal oscillator General-purpose digital I/O pin
$\overline{\text{RST}}$/NMI/SBWTDIO	10	9	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/SBWTCK	11	10	I	Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
V_{CC}	1	NA		Supply voltage
V_{SS}	14	NA		Ground reference
DV_{CC}	NA	16		Digital supply voltage
AV_{CC}	NA	15		Analog supply voltage
DV_{SS}	NA	14		Digital ground reference
AV_{SS}	NA	13		Analog ground reference
QFN Pad	NA	Package Pad	NA	QFN package pad connection to V_{SS} recommended.

NOTE: If XOUT/P2.7 is used as an input, excess current will flow until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 ---> R5
Single operands, destination only	e.g., CALL R8	PC -->(TOS), R8--> PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 --> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)--> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) --> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) --> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) --> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) --> R11 R10 + 2--> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 --> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 1 (LPM1);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
    DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2);
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3);
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4);
  - CPU is disabled
    ACLK is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator is disabled
    Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh–0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (e.g., flash is not programmed) the CPU will go into LPM4 immediately after power-up.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Timer+ Flash key violation PC out-of-range (see Note 1)	PORIFG RSTIFG WDTIFG KEYV (see Note 2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (see Notes 2 and 4)	(non)-maskable, (non)-maskable, (non)-maskable	0FFFCh	30
			0FFFAh	29
			0FFF8h	28
Comparator_A+ (MSP430x20x1 only)	CAIFG (see Note 3)	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer_A2	TACCR0 CCIFG (see Note 3)	maskable	0FFF2h	25
Timer_A2	TACCR1 CCIFG. TAIFG (see Notes 2 and 3)	maskable	0FFF0h	24
			0FFEEh	23
			0FFECh	22
ADC10 (MSP430x20x2 only)	ADC10IFG (see Note 3)	maskable	0FFEAh	21
SD16_A (MSP430x20x3 only)	SD16CCTL0 SD16OVIFG, SD16CCTL0 SD16IFG (see Notes 2 and 3)	maskable		
USI (MSP430x20x2, MSP430x20x3 only)	USIIFG, USISTTIFG (see Notes 2 and 3)	maskable	0FFE8h	20
I/O Port P2 (two flags)	P2IFG.6 to P2IFG.7 (see Notes 2 and 3)	maskable	0FFE6h	19
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 2 and 3)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
(see Note 5)			0FFDEh ... 0FFC0h	15 ... 0, lowest

NOTES: 1. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h–01FFh) or from within unused address ranges.
2. Multiple source flags
3. Interrupt flags are located in the module
4. (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
5. The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE: Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE: Oscillator fault enable
NMIIE: (Non)maskable interrupt enable
ACCVIE: Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h								

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG: Set on Watchdog Timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.
OFIFG: Flag set on oscillator fault
RSTIFG: External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power-up
PORIFG: Power-On Reset interrupt flag. Set on V_{CC} power-up.
NMIIFG: Set via $\overline{RST}$/NMI-pin

Address	7	6	5	4	3	2	1	0
03h								

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is Reset or Set by PUC.
	rw-(0,1):	Bit can be read and written. It is Reset or Set by POR.
		SFR bit is not present in device

memory organization

		MSP430F200x	MSP430F201x
Memory Main: interrupt vector Main: code memory	Size Flash Flash	1KB Flash 0FFFFh-0FFC0h 0FFFFh-0FC00h	2KB Flash 0FFFFh-0FFC0h 0FFFFh-0F800h
Information memory	Size Flash	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h
RAM	Size	128 Byte 027Fh – 0200h	128 Byte 027Fh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

flash memory

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0–n.
  Segments A to D are also called *information memory.*
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x2xx Family User's Guide.*

oscillator and system clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator and an internal digitally-controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

DCO Calibration Data (provided from factory in flash info memory segment A)			
DCO Frequency	**Calibration Register**	**Size**	**Address**
1 MHz	CALBC1_1MHZ	byte	010FFh
	CALDCO_1MHZ	byte	010FEh
8 MHz	CALBC1_8MHZ	byte	010FDh
	CALDCO_8MHZ	byte	010FCh
12 MHz	CALBC1_12MHZ	byte	010FBh
	CALDCO_12MHZ	byte	010FAh
16 MHz	CALBC1_16MHZ	byte	010F9h
	CALDCO_16MHZ	byte	010F8h

brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

digital I/O

There is one 8-bit I/O port implemented—port P1—and two bits of I/O port P2:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and the two bits of port P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pull-up/pull-down resistor.

WDT+ watchdog timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Timer_A2

Timer_A2 is a 16-bit timer/counter with two capture/compare registers. Timer_A2 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A2 Signal Connections (MSP43020x1 only)							
Input Pin Number		Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number	
PW, N	RSA					PW, N	RSA
2 - P1.0	1 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
2 - P1.0	1 - P1.0	$\overline{\text{TACLK}}$	INCLK				
3 - P1.1	2 - P1.1	TA0	CCI0A	CCR0	TA0	3 - P1.1	2 - P1.1
		ACLK (internal)	CCI0B			7 - P1.5	6 - P1.5
		V_{SS}	GND				
		V_{CC}	V_{CC}				
4 - P1.2	3 - P1.2	TA1	CCI1A	CCR1	TA1	4 - P1.2	3 - P1.2
		CAOUT (internal)	CCI1B			8 - P1.6	7 - P1.6
		V_{SS}	GND			13 - P2.6	12 - P2.6
		V_{CC}	V_{CC}				

Timer_A2 Signal Connections (MSP430F20x2, MSP430F20x3)							
Input Pin Number		Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number	
PW, N	RSA					PW, N	RSA
2 - P1.0	1 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
2 - P1.0	1 - P1.0	$\overline{\text{TACLK}}$	INCLK				
3 - P1.1	2 - P1.1	TA0	CCI0A	CCR0	TA0	3 - P1.1	2 - P1.1
7 - P1.5	6 - P1.5	ACLK (internal)	CCI0B			7 - P1.5	6 - P1.5
		V_{SS}	GND				
		V_{CC}	V_{CC}				
4 - P1.2	3 - P1.2	TA1	CCI1A	CCR1	TA1	4 - P1.2	3 - P1.2
8 - P1.6	7 - P1.6	TA1	CCI1B			8 - P1.6	7 - P1.6
		V_{SS}	GND			13 - P2.6	12 - P2.6
		V_{CC}	V_{CC}				

Comparator_A+ (MSP430x20x1 only)

The primary function of the comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

USI (MSP430x20x2 and MSP430x20x3 only)

The universal serial interface (USI) module is used for serial data communication and provides the basic hardware for synchronous communication protocols like SPI and I2C.

ADC10 (MSP430x20x2 only)

The ADC10 module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and data transfer controller, or DTC, for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.

SD16_A (MSP430x20x3 only)

The SD16_A module supports 16-bit analog-to-digital conversions. The module implements a 16-bit sigma-delta core and reference generator. In addition to external analog inputs, internal V_{CC} sense and temperature sensors are also available.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
ADC10 (MSP430x20x2 only)	ADC control 0 ADC control 1 ADC memory ADC data transfer start address	ADC10CTL0 ADC10CTL1 ADC10MEM ADC10SA	01B0h 01B2h 01B4h 01BCh
SD16_A (MSP430x20x3 only)	General Control Channel 0 Control Interrupt vector word register Channel 0 conversion memory	SD16CTL SD16CCTL0 SD16IV SD16MEM0	0100h 0102h 0110h 0112h
Timer_A	Capture/compare register Capture/compare register Timer_A register Capture/compare control Capture/compare control Timer_A control Timer_A interrupt vector	TACCR1 TACCR0 TAR TACCTL1 TACCTL0 TACTL TAIV	0174h 0172h 0170h 0164h 0162h 0160h 012Eh
Flash Memory	Flash control 3 Flash control 2 Flash control 1	FCTL3 FCTL2 FCTL1	012Ch 012Ah 0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
ADC10 (MSP430x20x2 only)	Analog enable ADC data transfer control register 1 ADC data transfer control register 0	ADC10AE ADC10DTC1 ADC10DTC0	04Ah 049h 048h
SD16_A (MSP430x20x3 only)	Channel 0 Input Control Analog Enable	SD16INCTL0 SD16AE	0B0h 0B7h
USI (MSP430x20x2 and MSP430x20x3 only)	USI control 0 USI control 1 USI clock control USI bit counter USI shift register	USICTL0 USICTL1 USICKCTL USICNT USISR	078h 079h 07Ah 07Bh 07Ch
Comparator_A+ (MSP430x20x1 only)	Comparator_A+ port disable Comparator_A+ control 2 Comparator_A+ control 1	CAPD CACTL2 CACTL1	05Bh 05Ah 059h
Basic Clock System+	Basic clock system control 3 Basic clock system control 2 Basic clock system control 1 DCO clock frequency control	BCSCTL3 BCSCTL2 BCSCTL1 DCOCTL	053h 058h 057h 056h
Port P2	Port P2 resistor enable Port P2 selection Port P2 interrupt enable Port P2 interrupt edge select Port P2 interrupt flag Port P2 direction Port P2 output Port P2 input	P2REN P2SEL P2IE P2IES P2IFG P2DIR P2OUT P2IN	02Fh 02Eh 02Dh 02Ch 02Bh 02Ah 029h 028h
Port P1	Port P1 resistor enable Port P1 selection Port P1 interrupt enable Port P1 interrupt edge select Port P1 interrupt flag Port P1 direction Port P1 output Port P1 input	P1REN P1SEL P1IE P1IES P1IFG P1DIR P1OUT P1IN	027h 026h 025h 024h 023h 022h 021h 020h
Special Function	SFR interrupt flag 2 SFR interrupt flag 1 SFR interrupt enable 2 SFR interrupt enable 1	IFG2 IFG1 IE2 IE1	003h 002h 001h 000h

absolute maximum ratings†

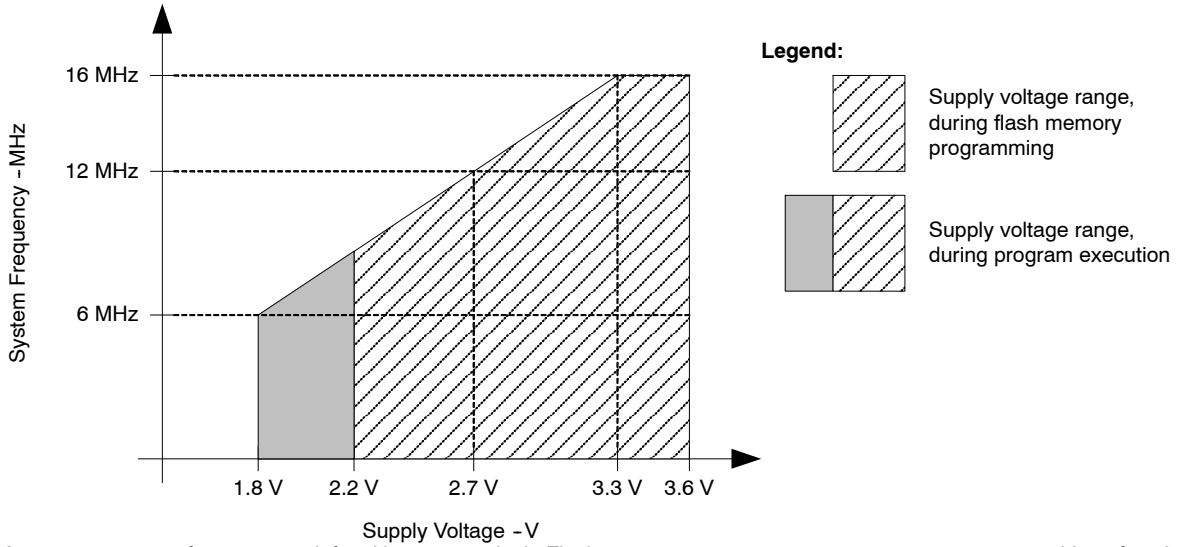
Voltage applied at V_{CC} to V_{SS} . . . . . –0.3 V to 4.1 V
Voltage applied to any pin (see Note 2) . . . . . –0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature, T_{stg} (unprogrammed device, see Note 3) . . . . . –55°C to 150°C
Storage temperature, T_{stg} (programmed device, see Note 3) . . . . . –40°C to 150°C

NOTES: 1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
3. Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

recommended operating conditions

		MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC}		1.8		3.6	V
Supply voltage during program/erase flash memory, V_{CC}		2.2		3.6	V
Supply voltage, V_{SS}			0		V
Operating free-air temperature range, T_A	I Version	–40		85	°C
	T Version	–40		105	°C
Processor frequency f_{SYSTEM} (Maximum MCLK frequency)	V_{CC} = 1.8 V, Duty Cycle = 50% ±10%	dc		6	MHz
	V_{CC} = 2.7 V, Duty Cycle = 50% ±10%	dc		12	
	V_{CC} ≥ 3.3 V, Duty Cycle = 50% ±10%	dc		16	

NOTES: 1. The MSP430 CPU is clocked directly with MCLK.
Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
2. Modules might have a different maximum input clock specification. Refer to the specification of the respective module in this data sheet.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Save Operating Area

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

active mode supply current (into V_{CC}) excluding external current (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
$I_{AM, 1MHz}$	Active mode (AM) current (1MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 1MHz$, $f_{ACLK} = 32,768Hz$, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		220	270	µA
				3 V		300	370	
$I_{AM, 1MHz}$	Active mode (AM) current (1MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 1MHz$, $f_{ACLK} = 32,768Hz$, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		190		µA
				3 V		260		
$I_{AM, 4kHz}$	Active mode (AM) current (4kHz)	$f_{MCLK} = f_{SMCLK} =$ $f_{ACLK} = 32,768Hz/8 = 4,096Hz$, $f_{DCO} = 0Hz$, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	-40–85°C	2.2 V		1.2	3	µA
			105°C	2.2 V			6	
			-40–85°C	3 V		1.6	4	
			105°C	3 V			7	
$I_{AM,100kHz}$	Active mode (AM) current (100kHz)	$f_{MCLK} = f_{SMCLK} = f_{DCO(0, 0)} \approx 100kHz$, $f_{ACLK} = 0Hz$, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1	-40–85°C	2.2 V		37	50	µA
			105°C	2.2 V			60	
			-40–85°C	3 V		40	55	
			105°C	3 V			65	

NOTES: 1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
2. The currents are characterized with a Micro Crystal CC4V–T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9pF.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – active mode supply current (into V_{CC})

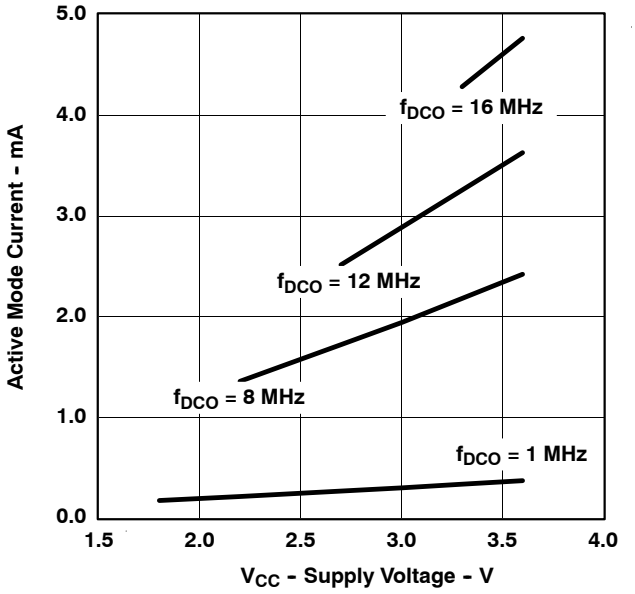


Figure 2. Active mode current vs V_{CC}, T_A = 25°C

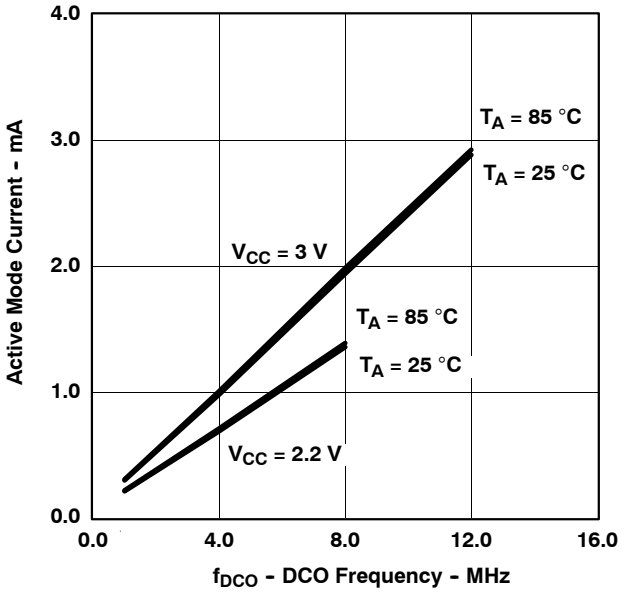


Figure 3. Active mode current vs DCO frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

low power mode supply currents (into V_{CC}) excluding external current (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
$I_{LPM0, 1MHz}$	Low-power mode 0 (LPM0) current, see Note 3	f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO}$ = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		65	80	µA
				3 V		85	100	
$I_{LPM0, 100kHz}$	Low-power mode 0 (LPM0) current, see Note 3	f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO(0, 0)} \approx$ 100 kHz, f_{ACLK} = 0 Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1		2.2 V		37	48	µA
				3 V		41	52	
I_{LPM2}	Low-power mode 2 (LPM2) current, see Note 4	$f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	-40–85°C	2.2 V		22	29	µA
			105°C				31	
			-40–85°C	3 V		25	32	
			105°C				34	
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current, see Note 4	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = 32,768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		0.7	1.2	µA
			25°C			0.7	1.0	
			85°C			1.4	2.3	
			105°C			3	6	
			-40°C	3 V		0.9	1.2	µA
			25°C			0.9	1.2	
			85°C			1.6	2.8	
			105°C			3	7	
$I_{LPM3,VLO}$	Low-power mode 3 current, (LPM3) see Note 4	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		0.4	0.7	µA
			25°C			0.5	0.7	
			85°C			1.0	1.6	
			105°C			2	5	
			-40°C	3 V		0.5	0.9	µA
			25°C			0.6	0.9	
			85°C			1.3	1.8	
			105°C			2.5	6	
I_{LPM4}	Low-power mode 4 (LPM4) current, see Note 5	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	-40°C	2.2 V/3 V		0.1	0.5	µA
			25°C			0.1	0.5	
			85°C			0.8	1.5	
			105°C			2	4	

NOTES: 1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
2. The currents are characterized with a Micro Crystal CC4V–T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9pF.
3. Current for brownout and WDT clocked by SMCLK included.
4. Current for brownout and WDT clocked by ACLK included.
5. Current for brownout included.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – Ports P1 and P2

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45		0.75	V_{CC}
			2.2 V	1.00		1.65	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25		0.55	V_{CC}
			2.2 V	0.55		1.20	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} – V_{IT-})		2.2 V	0.2		1.0	V
			3 V	0.3		1.0	
R_{Pull}	Pull-up/pull-down resistor	For pullup: $V_{IN} = V_{SS}$; For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input Capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

inputs – Ports P1 and P2

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag, (see Note 1)	2.2 V/3 V	20			ns

NOTES: 1. An external signal sets the interrupt flag every time the minimum interrupt puls width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

leakage current – Ports P1 and P2

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	see Notes 1 and 2	2.2 V/3 V			±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of the digital port pins is measured individually. The port pin is selected for input and the pull-up/pull-down resistor is disabled.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1 and P2

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1.5 mA (see Notes 1)	2.2 V	V_{CC}–0.25		V_{CC}	V
		$I_{(OHmax)}$ = –6 mA (see Notes 2)	2.2 V	V_{CC}–0.6		V_{CC}	
		$I_{(OHmax)}$ = –1.5 mA (see Notes 1)	3 V	V_{CC}–0.25		V_{CC}	
		$I_{(OHmax)}$ = –6 mA (see Notes 2)	3 V	V_{CC}–0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1.5 mA (see Notes 1)	2.2 V	V_{SS}		V_{SS}+0.25	V
		$I_{(OLmax)}$ = 6 mA (see Notes 2)	2.2 V	V_{SS}		V_{SS}+0.6	
		$I_{(OLmax)}$ = 1.5 mA (see Notes 1)	3 V	V_{SS}		V_{SS}+0.25	
		$I_{(OLmax)}$ = 6 mA (see Notes 2)	3 V	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
2. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

output frequency – Ports P1 and P2

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kOhm (see Note 1 and 2)	2.2 V			10	MHz
			3 V			12	MHz
f_{Port_CLK}	Clock output frequency	P2.0/ACLK, P1.4/SMCLK, C_L = 20 pF (see Note 2)	2.2 V			12	MHz
			3 V			16	MHz

NOTES: 1. A resistive divider with 2 times 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
2. The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – outputs

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

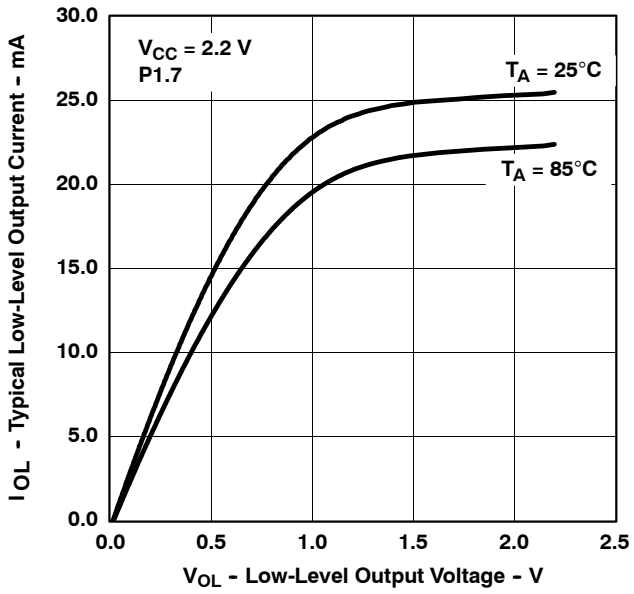


Figure 4

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

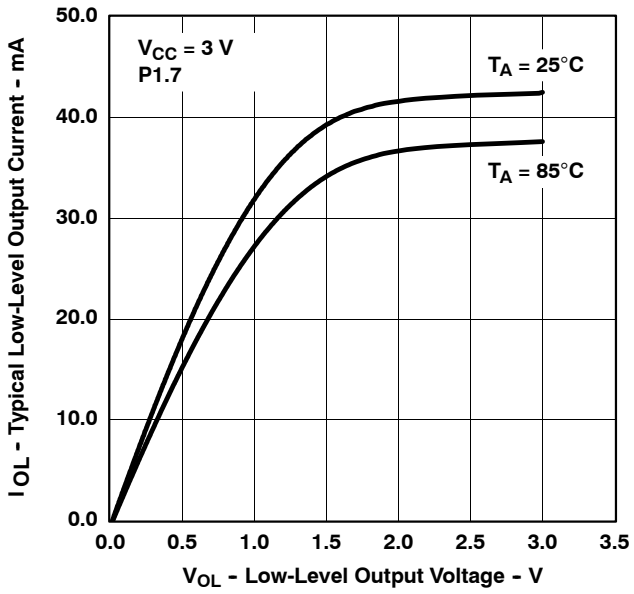


Figure 5

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

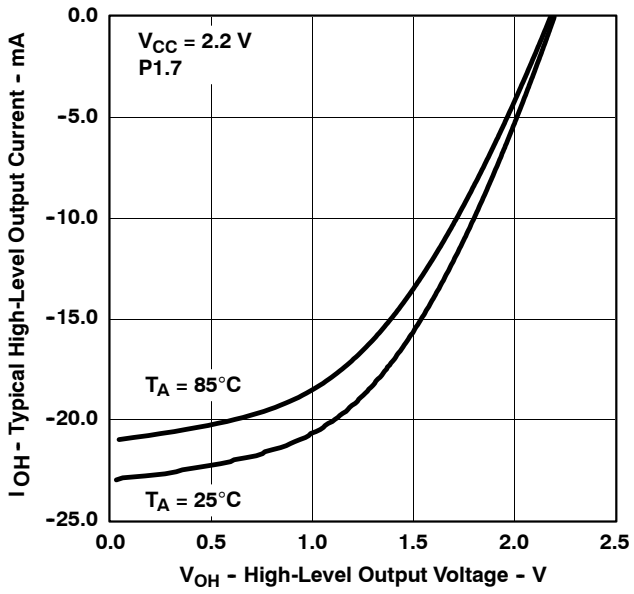


Figure 6

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

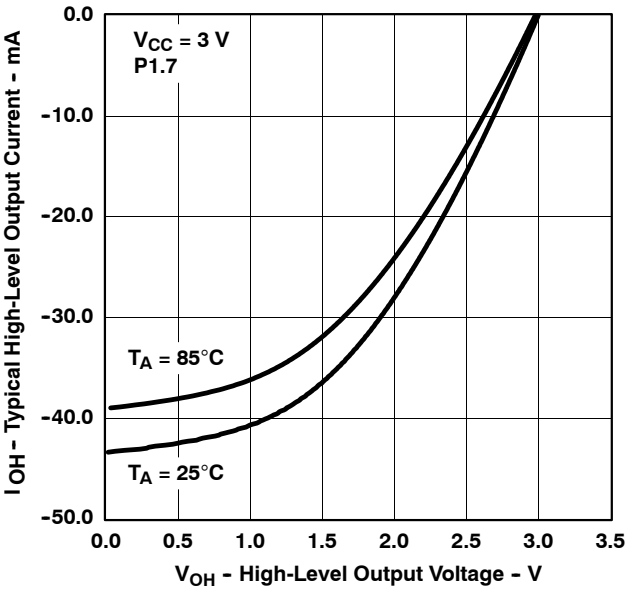


Figure 7

NOTE: One output loaded at a time.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	(see Figure 8)	$dV_{CC}/dt \le 3$ V/s			$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	(see Figure 8 through Figure 10)	$dV_{CC}/dt \le 3$ V/s				1.71	V
$V_{hys(B\_IT-)}$	(see Figure 8)	$dV_{CC}/dt \le 3$ V/s		70	130	210	mV
$t_{d(BOR)}$	(see Figure 8)					2000	μs
$t_{(reset)}$	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally		2.2 V/3 V	2			μs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8V.

2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

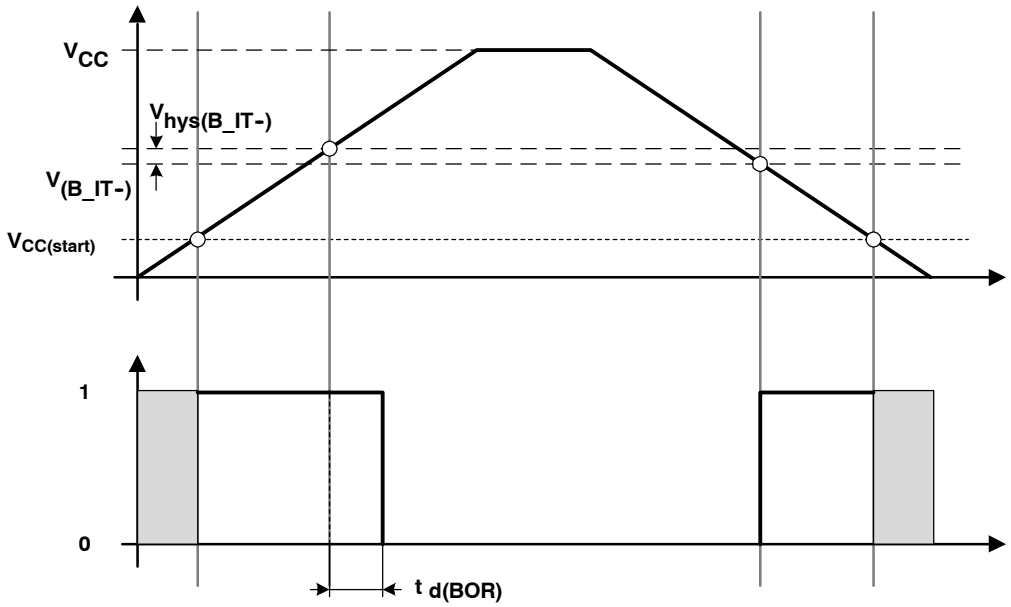


Figure 8. POR/Brownout Reset (BOR) vs Supply Voltage

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – POR/brownout reset (BOR)

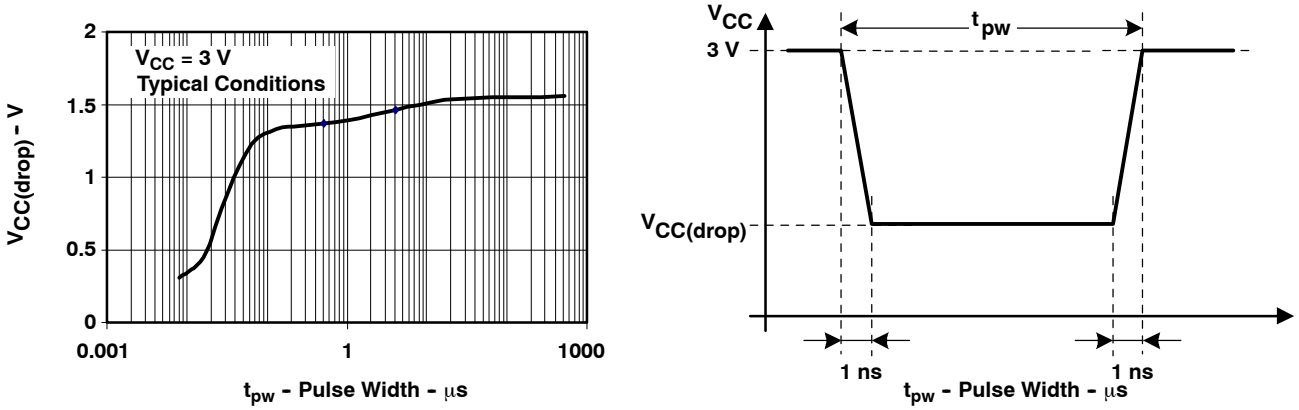


Figure 9. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

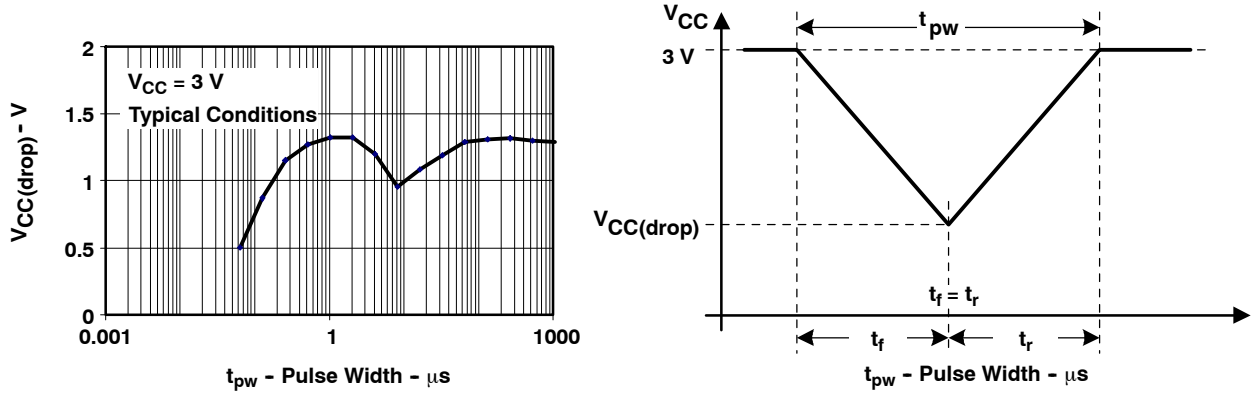


Figure 10. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO frequency

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
Vcc	Supply voltage range	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	V
		RSELx = 15		3.0		3.6	V
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	2.2 V/3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	2.2 V/3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	2.2 V/3 V	0.10		0.20	MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	2.2 V/3 V	0.14		0.28	MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	2.2 V/3 V	0.20		0.40	MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	0.28		0.54	MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	2.2 V/3 V	0.39		0.77	MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	2.2 V/3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	2.2 V/3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	2.2 V/3 V	1.10		2.10	MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	2.2 V/3 V	1.60		3.00	MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	2.2 V/3 V	2.50		4.30	MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	2.2 V/3 V	3.00		5.50	MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	2.2 V/3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	2.2 V/3 V	6.00		9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	2.2 V/3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V			1.55	ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V	1.05	1.08	1.12	ratio
Duty Cycle		Measured at P1.4/SMCLK	2.2 V/3 V	40	50	60	%

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

calibrated DCO frequencies – tolerance at calibration

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
Frequency tolerance at calibration			25°C	3 V	–1	±0.2	+1	%
$f_{CAL(1MHz)}$	1MHz calibration value	BCSCTL1= CALBC1_1MHZ DCOCTL = CALDCO_1MHZ Gating time: 5ms	25°C	3 V	0.990	1	1.010	MHz
$f_{CAL(8MHz)}$	8MHz calibration value	BCSCTL1= CALBC1_8MHZ DCOCTL = CALDCO_8MHZ Gating time: 5ms	25°C	3 V	7.920	8	8.080	MHz
$f_{CAL(12MHz)}$	12MHz calibration value	BCSCTL1= CALBC1_12MHZ DCOCTL = CALDCO_12MHZ Gating time: 5ms	25°C	3 V	11.88	12	12.12	MHz
$f_{CAL(16MHz)}$	16MHz calibration value	BCSCTL1= CALBC1_16MHZ DCOCTL = CALDCO_16MHZ Gating time: 2ms	25°C	3 V	15.84	16	16.16	MHz

calibrated DCO frequencies – tolerance over temperature 0°C – +85°C

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
1 MHz tolerance over temperature			0–85°C	3.0 V	–2.5	±0.5	+2.5	%
8 MHz tolerance over temperature			0–85°C	3.0 V	–2.5	±1.0	+2.5	%
12 MHz tolerance over temperature			0–85°C	3.0 V	–2.5	±1.0	+2.5	%
16 MHz tolerance over temperature			0–85°C	3.0 V	–3.0	±2.0	+3.0	%
$f_{CAL(1MHz)}$	1MHz calibration value	BCSCTL1= CALBC1_1MHZ DCOCTL = CALDCO_1MHZ Gating time: 5ms	0–85°C	2.2 V	0.970	1	1.030	MHz
				3.0 V	0.975	1	1.025	MHz
				3.6 V	0.970	1	1.030	MHz
$f_{CAL(8MHz)}$	8MHz calibration value	BCSCTL1= CALBC1_8MHZ DCOCTL = CALDCO_8MHZ Gating time: 5ms	0–85°C	2.2 V	7.760	8	8.400	MHz
				3.0 V	7.800	8	8.200	MHz
				3.6 V	7.600	8	8.240	MHz
$f_{CAL(12MHz)}$	12MHz calibration value	BCSCTL1= CALBC1_12MHZ DCOCTL = CALDCO_12MHZ Gating time: 5ms	0–85°C	2.2 V	11.70	12	12.30	MHz
				3.0 V	11.70	12	12.30	MHz
				3.6 V	11.70	12	12.30	MHz
$f_{CAL(16MHz)}$	16MHz calibration value	BCSCTL1= CALBC1_16MHZ DCOCTL = CALDCO_16MHZ Gating time: 2ms	0–85°C	3.0 V	15.52	16	16.48	MHz
				3.6 V	15.00	16	16.48	MHz

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

calibrated DCO frequencies – tolerance over supply voltage V_{CC}

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
1 MHz tolerance over V_{CC}			25°C	1.8 V – 3.6 V	–3	±2	+3	%
8 MHz tolerance over V_{CC}			25°C	1.8 V – 3.6 V	–3	±2	+3	%
12 MHz tolerance over V_{CC}			25°C	2.2 V – 3.6 V	–3	±2	+3	%
16 MHz tolerance over V_{CC}			25°C	3.0 V – 3.6 V	–3	±2	+3	%
$f_{CAL(1MHz)}$	1MHz calibration value	BCSCTL1= CALBC1_1MHZ DCOCTL = CALDCO_1MHZ Gating time: 5ms	25°C	1.8 V – 3.6 V	0.970	1	1.030	MHz
$f_{CAL(8MHz)}$	8MHz calibration value	BCSCTL1= CALBC1_8MHZ DCOCTL = CALDCO_8MHZ Gating time: 5ms	25°C	1.8 V – 3.6 V	7.760	8	8.240	MHz
$f_{CAL(12MHz)}$	12MHz calibration value	BCSCTL1= CALBC1_12MHZ DCOCTL = CALDCO_12MHZ Gating time: 5ms	25°C	2.2 V – 3.6 V	11.64	12	12.36	MHz
$f_{CAL(16MHz)}$	16MHz calibration value	BCSCTL1= CALBC1_16MHZ DCOCTL = CALDCO_16MHZ Gating time: 2ms	25°C	3.0 V – 3.6 V	15.00	16	16.48	MHz

calibrated DCO frequencies – overall tolerance

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
1 MHz tolerance overall			I: -40–85°C T: -40–105°C	1.8 V – 3.6 V	–5	±2	+5	%
8 MHz tolerance overall			I: -40–85°C T: -40–105°C	1.8 V – 3.6 V	–5	±2	+5	%
12 MHz tolerance overall			I: -40–85°C T: -40–105°C	2.2 V – 3.6 V	–5	±2	+5	%
16 MHz tolerance overall			I: -40–85°C T: -40–105°C	3.0 V – 3.6 V	–6	±3	+6	%
$f_{CAL(1MHz)}$	1MHz calibration value	BCSCTL1= CALBC1_1MHZ DCOCTL = CALDCO_1MHZ Gating time: 5ms	I: -40–85°C T: -40–105°C	1.8 V – 3.6 V	0.950	1	1.050	MHz
$f_{CAL(8MHz)}$	8MHz calibration value	BCSCTL1= CALBC1_8MHZ DCOCTL = CALDCO_8MHZ Gating time: 5ms	I: -40–85°C T: -40–105°C	1.8 V – 3.6 V	7.600	8	8.400	MHz
$f_{CAL(12MHz)}$	12MHz calibration value	BCSCTL1= CALBC1_12MHZ DCOCTL = CALDCO_12MHZ Gating time: 5ms	I: -40–85°C T: -40–105°C	2.2 V – 3.6 V	11.40	12	12.60	MHz
$f_{CAL(16MHz)}$	16MHz calibration value	BCSCTL1= CALBC1_16MHZ DCOCTL = CALDCO_16MHZ Gating time: 2ms	I: -40–85°C T: -40–105°C	3.0 V – 3.6 V	15.00	16	17.00	MHz

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – calibrated 1MHz DCO frequency

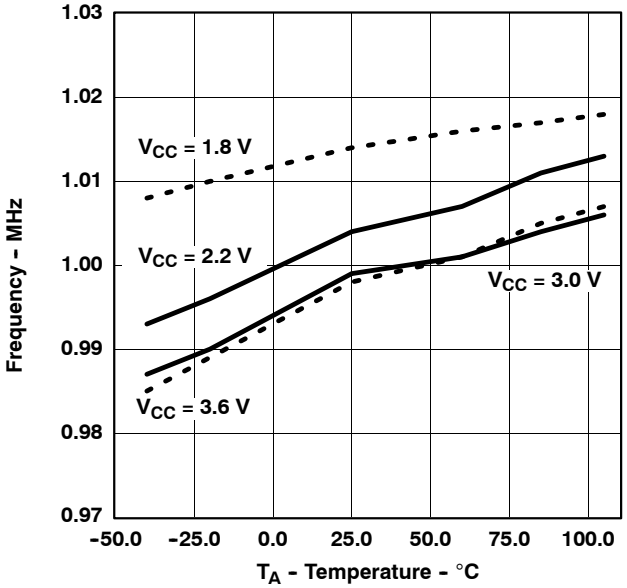


Figure 11. Calibrated 1 MHz Frequency vs. Temperature

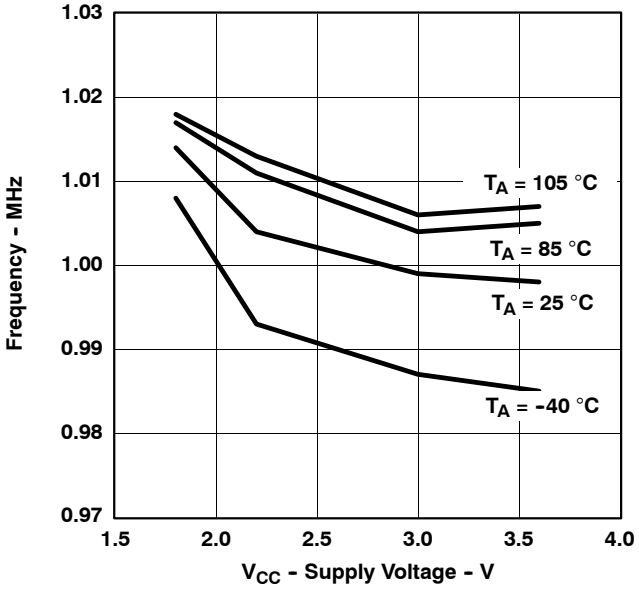


Figure 12. Calibrated 1 MHz Frequency vs. V_{CC}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

wake-up from lower power modes (LPM3/4)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4 (see Note 1)	BCSCTL1= CALBC1_1MHZ DCOCTL = CALDCO_1MHZ	2.2 V/3 V			2	µs
		BCSCTL1= CALBC1_8MHZ DCOCTL = CALDCO_8MHZ	2.2 V/3 V			1.5	
		BCSCTL1= CALBC1_12MHZ DCOCTL = CALDCO_12MHZ	2.2 V/3 V			1	
		BCSCTL1= CALBC1_16MHZ DCOCTL = CALDCO_16MHZ	3 V			1	
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4 (see Note 2)				$1/f_{MCLK}$ + $t_{Clock,LPM3/4}$		

NOTES: 1. The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g. port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
2. Parameter applicable only if DCOCLK is used for MCLK.

typical characteristics – DCO clock wake-up time from LPM3/4

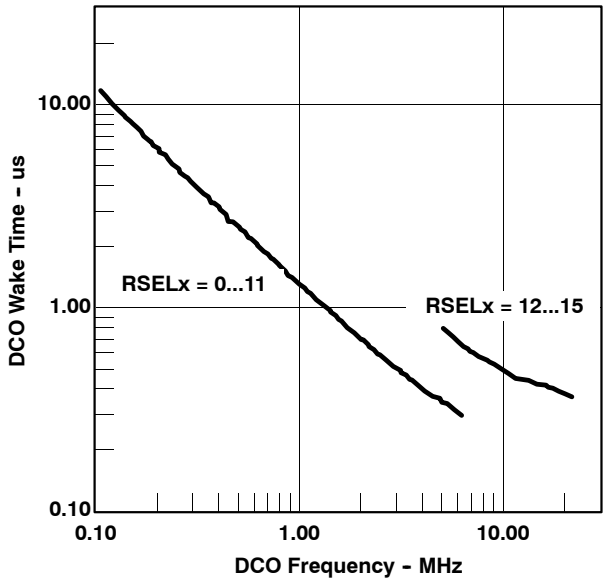


Figure 13. DCO wake-up time from LPM3 vs DCO frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1, low frequency modes (see Note 4)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V – 3.6 V		32,768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, LFXT1Sx = 3	1.8 V – 3.6 V	10,000	32,768	50,000	Hz
OA_{LF}	Oscillation Allowance for LF crystals	XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 12 pF			200		kΩ
$C_{L,eff}$	Integrated effective Load Capacitance, LF mode (see Note 1)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		pF
		XTS = 0, XCAPx = 2			8.5		pF
		XTS = 0, XCAPx = 3			11		pF
Duty Cycle	LF mode	XTS = 0, Measured at P1.4/ACLK, $f_{LFXT1,LF}$ = 32,768 Hz	2.2 V/3 V	30	50	70	%
$f_{Fault,LF}$	Osc. fault frequency threshold, LF mode (see Note 3)	XTS = 0, LFXT1Sx = 3 (see Note 2)	2.2 V/3 V	10		10,000	Hz

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Measured with logic level input frequency but also applies to operation with crystals.
3. Frequencies below the MIN specification will set the fault flag, frequencies above the MAX specification will not set the fault flag. Frequencies in between might set the flag.
4. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
   - Keep as short of a trace as possible between the device and the crystal.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

internal very low power, low frequency oscillator (VLO)

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency		-40–85°C	2.2 V/3 V	4	12	20	kHz
			105°C	2.2 V/3 V			22	
df_{VLO}/dT	VLO frequency temperature drift	(see Note 1)	I: -40–85°C T: -40–105°C	2.2 V/3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	(see Note 2)	25°C	1.8V – 3.6V		4		%/V

NOTES: 1. Calculated using the box method:
I Version: (MAX(–40...85°C) – MIN(–40...85°C))/MIN(–40...85°C)/(85°C – (–40°C))
T Version: (MAX(–40...105°C) – MIN(–40...105°C))/MIN(–40...105°C)/(105°C – (–40°C))
2. Calculated using the box method: (MAX(1.8...3.6V) – MIN(1.8...3.6V))/MIN(1.8...3.6V)/(3.6V – 1.8V)

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Timer_A

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK; External: TACLK, INCLK; Duty Cycle = 50% ±10%	2.2 V			10	MHz
			3 V			16	
$t_{TA,cap}$	Timer_A, capture timing	TA0, TA1	2.2 V/3 V	20			ns

USI, Universal Serial Interface (MSP430x20x2, MSP430x20x3 only)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
f_{USI}	USI clock frequency	External: SCLK; Duty Cycle = 50% ±10%; SPI Slave Mode	2.2 V			10	MHz
			3 V			16	
$V_{OL,I2C}$	Low-level output voltage on SDA and SCL	USI module in I2C mode $I_{(OLmax)}$ = 1.5 mA	2.2 V/3 V	V_{SS}		V_{SS}+0.4	V

typical characteristics – USI low-level output voltage on SDA and SCL (MSP430x20x2, MSP430x20x3 only)

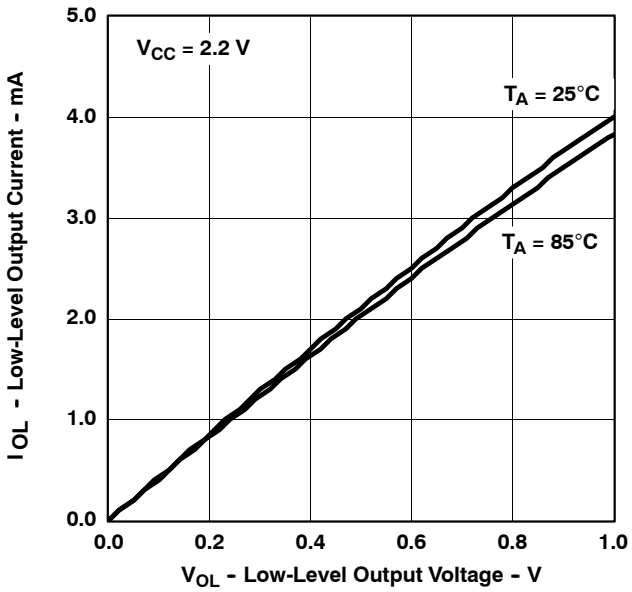


Figure 14. USI Low-Level Output Voltage vs. Output Current

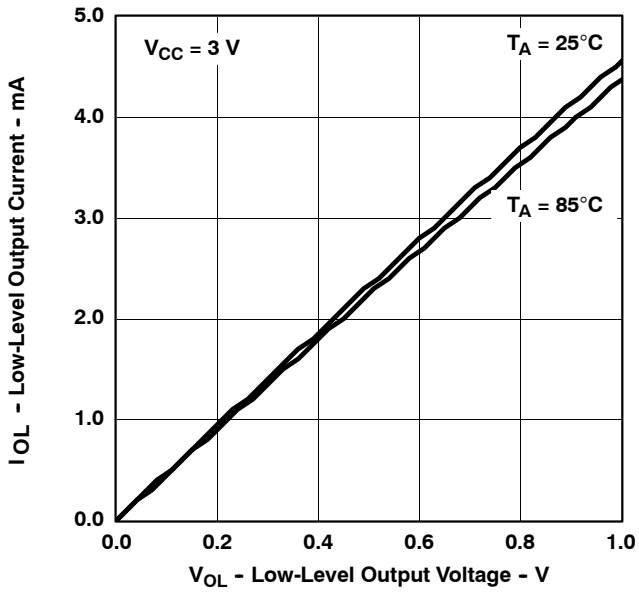


Figure 15. USI Low-Level Output Voltage vs. Output Current

MSP430x20x1 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Comparator_A+ (see Note 1, MSP430x20x1 only)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON=1, CARSEL=0, CAREF=0	2.2 V		25	40	µA
			3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, no load at P1.0/CA0 and P1.1/CA1	2.2 V		30	50	µA
			3 V		45	71	
$V_{(IC)}$	Common-mode input voltage	CAON=1	2.2 V/3 V	0		V_{CC}–1	V
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, no load at P1.0/CA0 and P1.1/CA1	2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5}V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, no load at P1.0/CA0 and P1.1/CA1	2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	(see Figure 19 and Figure 20)	PCA0=1, CARSEL=1, CAREF=3, no load at P1.0/CA0 and P1.1/CA1, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
$V_{(offset)}$	Offset voltage	See Note 2	2.2 V/3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON=1	2.2 V/3 V	0	0.7	1.4	mV
$t_{(response)}$	Response time (low–high and high–low)	T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0 (see Note 3, Figure 16 and Figure 17)	2.2 V	80	165	300	ns
			3 V	70	120	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1 (see Note 3, Figure 16 and Figure 17)	2.2 V	1.4	1.9	2.8	µs
			3 V	0.9	1.5	2.2	

NOTES: 1. The leakage current for the Comparator_A+ terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.
3. Response time measured at P1.3/CAOUT.

MSP430x20x1 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

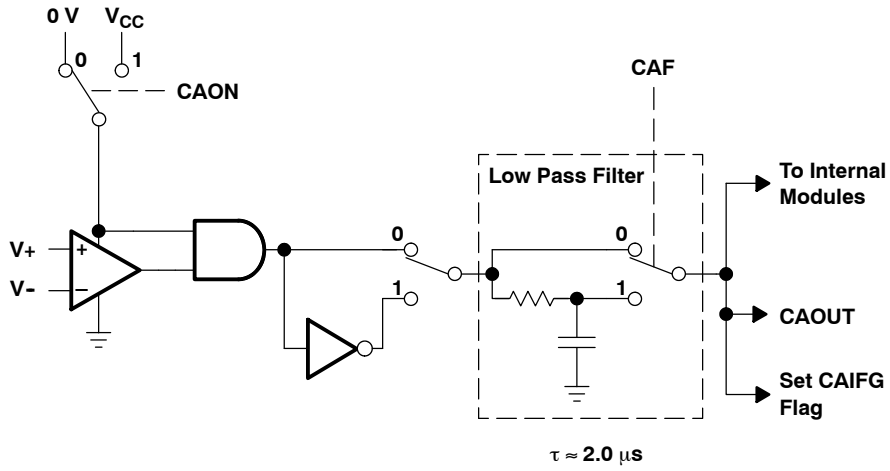


Figure 16. Block Diagram of Comparator_A+ Module

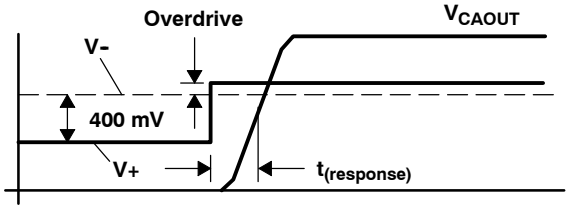


Figure 17. Overdrive Definition

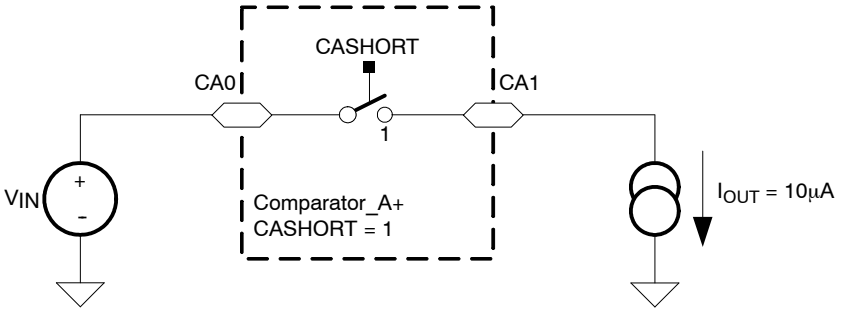


Figure 18. Comparator_A+ Short Resistance Test Condition

MSP430x20x1 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – Comparator_A+ (MSP430x20x1 only)

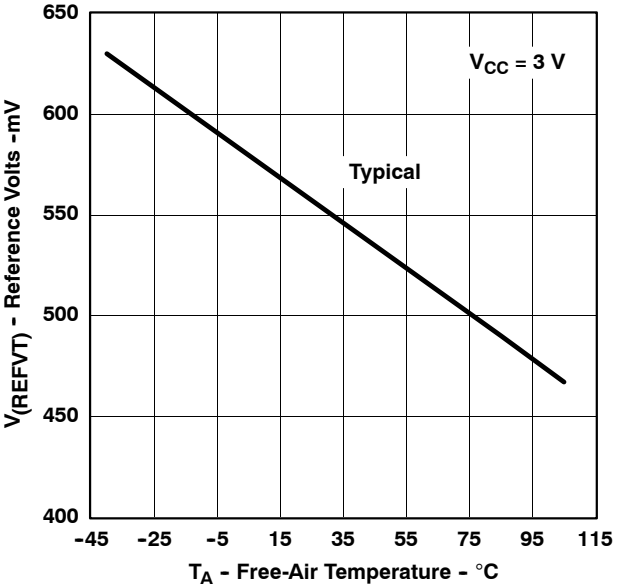


Figure 19. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

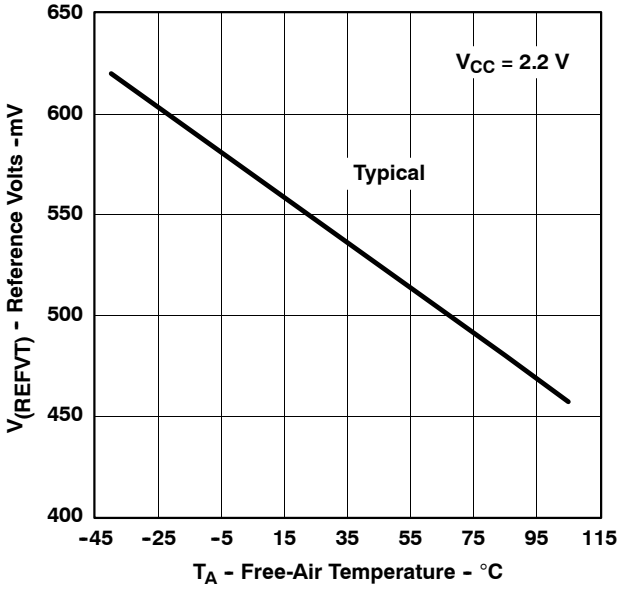


Figure 20. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

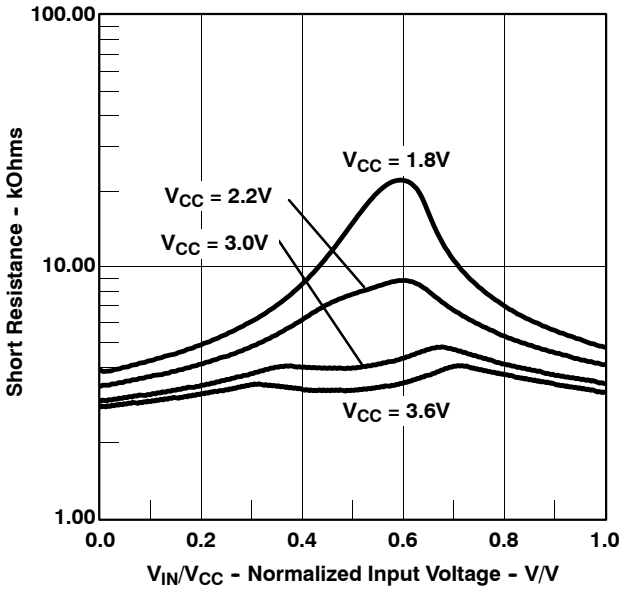


Figure 21. Short Resistance vs V_{IN}/V_{CC}

MSP430x20x2 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, power supply and input range conditions (see Note 1, MSP430x20x2 only)

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
V_{CC}	Analog supply voltage range	V_{SS} = 0 V			2.2		3.6	V
V_{Ax}	Analog input voltage range (see Note 2)	All Ax terminals. Analog inputs selected in ADC10AE register.			0		V_{CC}	V
I_{ADC10}	ADC10 supply current (see Note 3)	$f_{ADC10CLK}$ = 5.0 MHz ADC10ON = 1, REFON = 0 ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	I: -40–85°C T: -40–105°C	2.2 V		0.52	1.05	mA
				3 V		0.6	1.2	
I_{REF+}	Reference supply current, reference buffer disabled (see Note 4)	$f_{ADC10CLK}$ = 5.0 MHz ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	I: -40–85°C T: -40–105°C	2.2 V/3 V		0.25	0.4	mA
		$f_{ADC10CLK}$ = 5.0 MHz ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0	I: -40–85°C T: -40–105°C	3 V				mA
$I_{REFB,0}$	Reference buffer supply current with ADC10SR=0 (see Note 4)	$f_{ADC10CLK}$ = 5.0 MHz ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR=0	-40–85°C	2.2 V/3 V		1.1	1.4	mA
			105°C	2.2 V/3 V			1.8	mA
$I_{REFB,1}$	Reference buffer supply current with ADC10SR=1 (see Note 4)	$f_{ADC10CLK}$ = 5.0 MHz ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR=1	-40–85°C	2.2 V/3 V		0.5	0.7	mA
			105°C	2.2 V/3 V			0.8	mA
C_I	Input capacitance	Only one terminal Ax selected at a time	I: -40–85°C T: -40–105°C				27	pF
R_I	Input MUX ON resistance	$0V \le V_{Ax} \le V_{CC}$	I: -40–85°C T: -40–105°C	2.2 V/3 V			2000	Ω

NOTES:
1. The leakage current is defined in the leakage current table with Px.x/Ax parameter.
2. The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
3. The internal reference supply current is not included in current consumption parameter I_{ADC10}.
4. The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

MSP430x20x2 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, built-in voltage reference (MSP430x20x2 only)

PARAMETER		TEST CONDITIONS		VCC	MIN	TYP	MAX	UNIT
$V_{CC,REF+}$	Positive built-in reference analog supply voltage range	$I_{VREF+} \le$ 1mA, REF2_5V=0			2.2			V
		$I_{VREF+} \le$ 0.5mA, REF2_5V=1			2.8			
		$I_{VREF+} \le$ 1mA, REF2_5V=1			2.9			
V_{REF+}	Positive built-in reference voltage	$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 0		2.2 V/3 V	1.41	1.5	1.59	V
		$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 1		3 V	2.35	2.5	2.65	V
$I_{LD,VREF+}$	Maximum V_{REF+} load current			2.2 V			±0.5	mA
				3 V			±1	
	V_{REF+} load regulation	I_{VREF+} = 500 μA +/– 100 μA Analog input voltage $V_{Ax} \approx$ 0.75 V; REF2_5V = 0		2.2 V/3 V			±2	LSB
		I_{VREF+} = 500 μA ± 100 μA Analog input voltage $V_{Ax} \approx$ 1.25 V; REF2_5V = 1		3 V			±2	LSB
	V_{REF+} load regulation response time	I_{VREF+} = 100μA→900μA, $V_{Ax} \approx 0.5 \times V_{REF+}$ Error of conversion result ≤ 1 LSB	ADC10SR = 0	3 V			400	ns
			ADC10SR = 1	3V			2000	
C_{VREF+}	Max. capacitance at pin V_{REF+} (see Note 1)	$I_{VREF+} \le$ ±1mA, REFON = 1, REFOUT = 1		2.2 V/3 V			100	pF
TC_{REF+}	Temperature coefficient	I_{VREF+} = const. with 0 mA ≤ I_{VREF+} ≤ 1 mA		2.2 V/3 V			±100	ppm/°C
t_{REFON}	Settling time of internal reference voltage (see Note 2)	I_{VREF+} = 0.5 mA, REF2_5V=0 REFON = 0 → 1		3.6 V			30	μs
$t_{REFBURST}$	Settling time of reference buffer (see Note 2)	I_{VREF+} = 0.5 mA, REF2_5V=0, REFON = 1, REFBURST = 1	ADC10SR = 0	2.2 V			1	
			ADC10SR = 1	2.2 V			2.5	
		I_{VREF+} = 0.5 mA, REF2_5V=1, REFON = 1, REFBURST = 1	ADC10SR = 0	3 V			2	μs
			ADC10SR = 1	3 V			4.5	

NOTES: 1. The capacitance applied to the internal buffer operational amplifier, if switched to terminal P2.4/TA2/A4/V_{REF+}/V_{eREF+} (REFOUT=1), must be limited; the reference buffer may become unstable otherwise.

2. The condition is that the error in a conversion started after t_{REFON} or t_{RefBuf} is less than ±0.5 LSB.

MSP430x20x2 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, external reference (see Note 1, MSP430x20x2 only)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference input voltage range (see Note 2)	$V_{eREF+} > V_{eREF-}$ SREF1 = 1, SREF0 = 0		1.4		V_{CC}	V
		$V_{eREF-} \le V_{eREF+} \le V_{CC}$ – 0.15V SREF1 = 1, SREF0 = 1 (see Note 3)		1.4		3.0	V
V_{eREF-}	Negative external reference input voltage range (see Note 4)	$V_{eREF+} > V_{eREF-}$		0		1.2	V
ΔV_{eREF}	Differential external reference input voltage range $\Delta V_{eREF} = V_{eREF+} - V_{eREF-}$	$V_{eREF+} > V_{eREF-}$ (see Note 5)		1.4		V_{CC}	V
I_{VeREF+}	Static input current into V_{eREF+}	$0V \le V_{eREF+} \le V_{CC}$, SREF1 = 1, SREF0 = 0	2.2 V/3 V			±1	μA
		$0V \le V_{eREF+} \le V_{CC}$ – 0.15V ≤ 3V SREF1 = 1, SREF0 = 1 (see Note 3)	2.2 V/3 V			0	μA
I_{VeREF-}	Static input current into V_{eREF-}	$0V \le V_{eREF-} \le V_{CC}$	2.2 V/3 V			±1	μA

NOTES:
1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
4. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
5. The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

MSP430x20x2 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, timing parameters (MSP430x20x2 only)

PARAMETER		TEST CONDITIONS		VCC	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$	ADC10 input clock frequency	For specified performance of ADC10 linearity parameters	ADC10SR = 0	2.2 V/3 V	0.45		6.3	MHz
			ADC10SR = 1	2.2 V/3 V	0.45		1.5	
$f_{ADC10OSC}$	ADC10 built-in oscillator frequency	ADC10DIVx=0, ADC10SSELx = 0 $f_{ADC10CLK} = f_{ADC10OSC}$		2.2 V/3 V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0 $f_{ADC10CLK} = f_{ADC10OSC}$		2.2 V/3 V	2.06		3.51	µs
		$f_{ADC10CLK}$ from ACLK, MCLK or SMCLK: ADC10SSELx ≠ 0			13× ADC10DIV× $1/f_{ADC10CLK}$			µs
$t_{ADC10ON}$	Turn on settling time of the ADC	(see Note 1)					100	ns

NOTES: 1. The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

10-bit ADC, linearity parameters (MSP430x20x2 only)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
E_I	Integral linearity error		2.2 V/3 V			±1	LSB
E_D	Differential linearity error		2.2 V/3 V			±1	LSB
E_O	Offset error	Source impedance R_S < 100 Ω,	2.2 V/3 V			±1	LSB
E_G	Gain error		2.2 V/3 V		±1.1	±2	LSB
E_T	Total unadjusted error		2.2 V/3 V		±2	±5	LSB

MSP430x20x2 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, temperature sensor and built-in V_{MID} (MSP430x20x2 only)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
I_{SENSOR}	Temperature sensor supply current (see Note 1)	REFON = 0, INCHx = 0Ah, T_A = 25°C	2.2 V		40	120	µA
			3 V		60	160	
TC_{SENSOR}		ADC10ON = 1, INCHx = 0Ah (see Note 2)	2.2 V/3 V	3.44	3.55	3.66	mV/°C
$V_{Offset,Sensor}$	Sensor offset voltage	ADC10ON = 1, INCHx = 0Ah (see Note 2)		–100		100	mV
V_{Sensor}	Sensor output voltage (see Note 3)	Temperature sensor voltage at T_A = 105°C (T Version only)	2.2 V/3 V	1265	1365	1465	mV
		Temperature sensor voltage at T_A = 85°C	2.2 V/3 V	1195	1295	1395	mV
		Temperature sensor voltage at T_A = 25°C	2.2 V/3 V	985	1085	1185	
		Temperature sensor voltage at T_A = 0°C	2.2 V/3 V	895	995	1095	
$t_{Sensor(sample)}$	Sample time required if channel 10 is selected (see Note 4)	ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V/3 V	30			µs
I_{VMID}	Current into divider at channel 11 (see Note 5)	ADC10ON = 1, INCHx = 0Bh,	2.2 V			NA	µA
			3 V			NA	
V_{MID}	V_{CC} divider at channel 11	ADC10ON = 1, INCHx = 0Bh, V_{MID} is ≈0.5 x V_{CC}	2.2 V	1.06	1.1	1.14	V
			3 V	1.46	1.5	1.54	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (see Note 6)	ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

NOTES:
1. The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1), or (ADC10ON=1 and INCH=0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
2. The following formula can be used to calculate the temperature sensor output voltage:
   $V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV] or
   $V_{Sensor,typ} = TC_{Sensor}$ T [°C] + $V_{Sensor}(T_A = 0°C)$ [mV]
3. Values are not based on calculations using TC_{Sensor} or $V_{Offset,sensor}$ but on measurements.
4. The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
5. No additional current is needed. The V_{MID} is used during sampling.
6. The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

MSP430x20x3 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

SD16_A, power supply and recommended operating conditions (MSP430x20x3 only)

PARAMETER		TEST CONDITIONS		T_A	VCC	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage range	$AV_{CC} = DV_{CC} = V_{CC}$ $AV_{SS} = DV_{SS} = V_{SS} = 0V$				2.5		3.6	V
I_{SD16}	Analog supply current including internal reference	SD16LP = 0, f_{SD16} = 1 MHz, SD16OSR = 256	GAIN: 1,2	-40–85°C	3 V		730	1050	μA
				105°C				1170	
			GAIN: 4,8,16	-40–85°C			810	1150	
				105°C				1300	
			GAIN: 32	-40–85°C			1160	1700	
				105°C				1850	
		SD16LP = 1, f_{SD16} = 0.5 MHz, SD16OSR = 256	GAIN: 1	-40–85°C	3 V		720	1030	μA
				105°C				1160	
			GAIN: 32	-40–85°C			810	1150	
				105°C				1300	
f_{SD16}	SD16 input clock frequency	SD16LP = 0 (Low power mode disabled)			3 V	0.03	1	1.1	MHz
f_{SD16}	SD16 input clock frequency	SD16LP = 1 (Low power mode enabled)			3 V	0.03	0.5		MHz

SD16_A, input range (MSP430x20x3 only)

PARAMETER		TEST CONDITIONS		VCC	MIN	TYP	MAX	UNIT
$V_{ID,FSR}$	Differential full scale input voltage range (see Note 1)	Bipolar Mode, SD16UNI = 0			$-(V_{REF}/2)/GAIN$		$+(V_{REF}/2)/GAIN$	mV
		Unipolar Mode, SD16UNI = 1			0		$+(V_{REF}/2)/GAIN$	mV
V_{ID}	Differential input voltage range for specified performance (see Note 1)	SD16REFON=1	SD16GAINx=1			±500		mV
			SD16GAINx=2			±250		
			SD16GAINx=4			±125		
			SD16GAINx=8			±62		
			SD16GAINx=16			±31		
			SD16GAINx=32			±15		
Z_I	Input impedance (one input pin to AV_{SS})	f_{SD16} = 1MHz	SD16GAINx=1	3 V		200		kΩ
			SD16GAINx=32	3 V		75		
Z_{ID}	Differential Input impedance (IN+ to IN–)	f_{SD16} = 1MHz	SD16GAINx=1	3 V	300	400		kΩ
			SD16GAINx=32	3 V	100	150		
V_I	Absolute input voltage range				AV_{SS} -0.1V		AV_{CC}	V
V_{IC}	Common-mode input voltage range				AV_{SS} -0.1V		AV_{CC}	V

NOTES: 1. The analog input range depends on the reference voltage applied to V_{REF}. If V_{REF} is sourced externally, the full-scale range is defined by $V_{FSR+} = +(V_{REF}/2)/GAIN$ and $V_{FSR-} = -(V_{REF}/2)/GAIN$. The analog input range should not exceed 80% of V_{FSR+} or V_{FSR-}.

MSP430x20x3 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

SD16_A, SINAD performance (f_{SD16} = 1MHz, SD16OSRx = 1024, SD16REFON = 1, MSP430x20x3 only)

PARAMETER		TEST CONDITIONS	VCC	PW, or N		RSA		UNIT
				MIN	TYP	MIN	TYP	
$SINAD_{1024}$	Signal-to-Noise + Distortion Ratio (OSR = 1024)	SD16GAINx = 1, Signal Amplitude: V_{IN} = 500mV, Signal Frequency: f_{IN} = 100Hz	3 V	84	85	86	87	dB
		SD16GAINx = 2, Signal Amplitude: V_{IN} = 250mV, Signal Frequency: f_{IN} = 100Hz	3 V	82	83	82	83	
		SD16GAINx = 4, Signal Amplitude: V_{IN} = 125mV, Signal Frequency: f_{IN} = 100Hz	3 V	78	79	78	79	
		SD16GAINx = 8, Signal Amplitude: V_{IN} = 62mV, Signal Frequency: f_{IN} = 100Hz	3 V	73	74	73	74	
		SD16GAINx = 16, Signal Amplitude: V_{IN} = 31mV, Signal Frequency: f_{IN} = 100Hz	3 V	68	69	68	69	
		SD16GAINx = 32, Signal Amplitude: V_{IN} = 15mV, Signal Frequency: f_{IN} = 100Hz	3 V	62	63	62	63	

SD16_A, SINAD performance (f_{SD16} = 1MHz, SD16OSRx = 256, SD16REFON = 1, MSP430x20x3 only)

PARAMETER		TEST CONDITIONS	VCC	PW, or N		RSA		UNIT
				MIN	TYP	MIN	TYP	
$SINAD_{256}$	Signal-to-Noise + Distortion Ratio (OSR = 256)	SD16GAINx = 1, Signal Amplitude: V_{IN} = 500mV, Signal Frequency: f_{IN} = 100Hz	3 V	80	81	82	83	dB
		SD16GAINx = 2, Signal Amplitude: V_{IN} = 250mV, Signal Frequency: f_{IN} = 100Hz	3 V	74	75	76	77	
		SD16GAINx = 4, Signal Amplitude: V_{IN} = 125mV, Signal Frequency: f_{IN} = 100Hz	3 V	69	70	71	72	
		SD16GAINx = 8, Signal Amplitude: V_{IN} = 62mV, Signal Frequency: f_{IN} = 100Hz	3 V	63	64	67	68	
		SD16GAINx = 16, Signal Amplitude: V_{IN} = 31mV, Signal Frequency: f_{IN} = 100Hz	3 V	58	59	63	64	
		SD16GAINx = 32, Signal Amplitude: V_{IN} = 15mV, Signal Frequency: f_{IN} = 100Hz	3 V	52	53	57	58	

MSP430x20x3 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – SD16_A SINAD performance over OSR (MSP430x20x3 only)

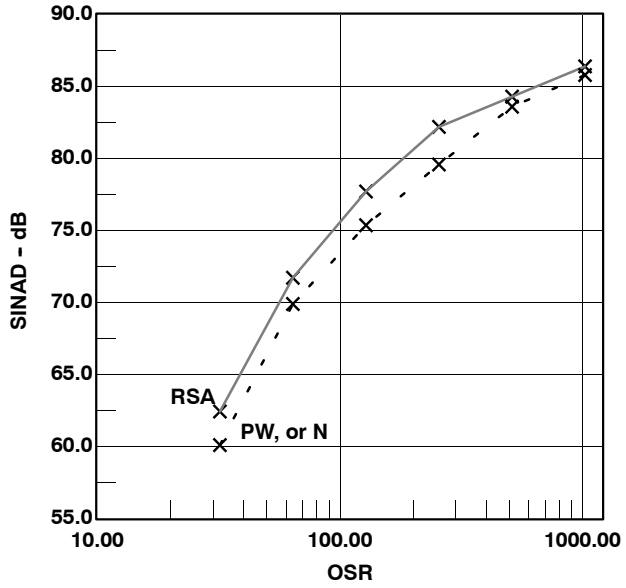


Figure 22. SINAD performance over OSR, f_{SD16} = 1MHz, SD16REFON = 1, SD16GAINx = 1

SD16_A, performance (f_{SD16} = 1MHz, SD16OSRx = 256, SD16REFON = 1, MSP430x20x3 only)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
G	Nominal Gain	SD16GAINx = 1	3 V	0.97	1.00	1.02	
		SD16GAINx = 2	3 V	1.90	1.96	2.02	
		SD16GAINx = 4	3 V	3.76	3.86	3.96	
		SD16GAINx = 8	3 V	7.36	7.62	7.84	
		SD16GAINx = 16	3 V	14.56	15.04	15.52	
		SD16GAINx = 32	3 V	27.20	28.35	29.76	
dG/dT	Gain Temperature Drift	SD16GAINx = 1 (see Note 1)	3 V		15		ppm/°C
E_{OS}	Offset Error	SD16GAINx = 1	3 V			±0.2	%FSR
		SD16GAINx = 32	3 V			±1.5	
dE_{OS}/dT	Offset Error Temperature Coefficient	SD16GAINx = 1	3 V		±4	±20	ppm FSR/°C
		SD16GAINx = 32	3 V		±20	±100	
CMRR	Common-Mode Rejection Ratio	SD16GAINx = 1, Common-mode input signal: V_{ID} = 500 mV, f_{IN} = 50 Hz, 100 Hz	3 V		>90		dB
		SD16GAINx = 32, Common-mode input signal: V_{ID} = 16 mV, f_{IN} = 50 Hz, 100 Hz	3 V		>75		
DC PSR	DC Power Supply Rejection	SD16GAINx = 1; V_{IN} = 500mV V_{CC} = 2.5V - 3.6V (see Note 2)	2.5V–3.6V		0.35		%/V
AC PSRR	AC Power Supply Rejection Ratio	SD16GAINx = 1 V_{CC} = 3.0V±100mV, f_{IN} = 50 Hz	3 V		>80		dB

NOTES: 1. Calculated using the box method: (MAX(–40...85°C) – MIN(–40...85°C)) / MIN(–40...85°C) / (85°C – (–40°C))
2. Calculated using the ADC output code and the box method:
(MAX-code(2.5...3.6V) – MIN-code(2.5...3.6V)) / MIN-code(2.5...3.6V) / (3.6V – 2.5V)

MSP430x20x3 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

SD16_A, built-in voltage reference (MSP430x20x3 only)

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference voltage	SD16REFON = 1, SD16VMIDON = 0		3 V	1.14	1.20	1.26	V
I_{REF}	Reference supply current	SD16REFON = 1, SD16VMIDON = 0	-40–85°C	3 V		190	280	μA
			105°C	3 V			295	
TC	Temperature coefficient	SD16REFON = 1, SD16VMIDON = 0		3 V		18	50	ppm/K
C_{REF}	V_{REF} load capacitance	SD16REFON = 1, SD16VMIDON = 0 (see Note 1)				100		nF
I_{LOAD}	$V_{REF(I)}$ maximum load current	SD16REFON = 1; SD16VMIDON = 0		3 V			±200	nA
t_{ON}	Turn on time	SD16REFON = 0 → 1; SD16VMIDON = 0; C_{REF} = 100nF		3 V		5		ms
DC PSR	DC Power Supply Rejection $\Delta V_{REF}/\Delta V_{CC}$	SD16REFON = 1; SD16VMIDON = 0; V_{CC} = 2.5V - 3.6V		2.5V–3.6V		100		uV/V

NOTES: 1. There is no capacitance required on V_{REF}. However, a capacitance of at least 100nF is recommended to reduce any reference voltage noise.

SD16_A, reference output buffer (MSP430x20x3 only)

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
$V_{REF,BUF}$	Reference buffer output voltage	SD16REFON = 1, SD16VMIDON = 1		3 V		1.2		V
$I_{REF,BUF}$	Reference Supply + Reference output buffer quiescent current	SD16REFON = 1, SD16VMIDON = 1	-40–85°C	3 V		385	600	μA
			105°C	3 V			660	
$C_{REF(O)}$	Required load capacitance on V_{REF}	SD16REFON = 1, SD16VMIDON = 1			470			nF
$I_{LOAD,Max}$	Maximum load current on V_{REF}	SD16REFON = 1, SD16VMIDON = 1		3 V			±1	mA
Maximum voltage variation vs. load current		$\|I_{LOAD}\|$ = 0 to 1mA		3 V	-15		+15	mV
t_{ON}	Turn on time	SD16REFON = 0 → 1; SD16VMIDON = 1; C_{REF} = 470nF		3 V		100		μs

SD16_A, external reference input (MSP430x20x3 only)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage range	SD16REFON = 0	3 V	1.0	1.25	1.5	V
$I_{REF(I)}$	Input current	SD16REFON = 0	3 V			50	nA

MSP430x20x3 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

SD16_A, temperature sensor (MSP430x20x3 only)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
TC_{Sensor}	Sensor temperature coefficient			1.18	1.32	1.46	mV/K
$V_{Offset,Sensor}$	Sensor offset voltage			–100		100	mV
V_{Sensor}	Sensor output voltage (see Note 2)	Temperature sensor voltage at T_A = 85°C	3 V	435	475	515	mV
		Temperature sensor voltage at T_A = 25°C	3 V	355	395	435	
		Temperature sensor voltage at T_A = 0°C	3 V	320	360	400	

NOTES: 1. The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV] or
$V_{Sensor,typ} = TC_{Sensor}$ T [°C] + $V_{Sensor}(T_A = 0°C)$ [mV]
2. Values are not based on calculations using TC_{Sensor} or $V_{Offset,sensor}$ but on measurements.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Flash Memory

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.2		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V/3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V/3.6 V		1	7	mA
t_{CPT}	Cumulative program time (see Note 1)		2.2 V/3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V/3.6 V	20			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 2			30		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				25		
$t_{Block, 1-63}$	Block program time for each additional byte or word				18		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				10593		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (see Note 1)	CPU halted	1.6			V

NOTE 1: This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

JTAG and Spy-Bi-Wire Interface

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency		2.2 V / 3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse length		2.2 V / 3 V	0.025		15	us
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge, see Note 1)		2.2 V/ 3 V			1	us
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time		2.2 V/ 3 V	15		100	us
f_{TCK}	TCK input frequency – 4-wire JTAG (see Note 2)		2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-down resistance on TEST		2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
2. f_{TCK} may be restricted to meet the timing requirements of the module selected.

JTAG Fuse (see Note 1)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TEST for fuse-blow			6		7	V
I_{FB}	Supply current into TEST during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTES: 1. Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible and JTAG is switched to bypass mode.

APPLICATION INFORMATION, MSP430x20x1

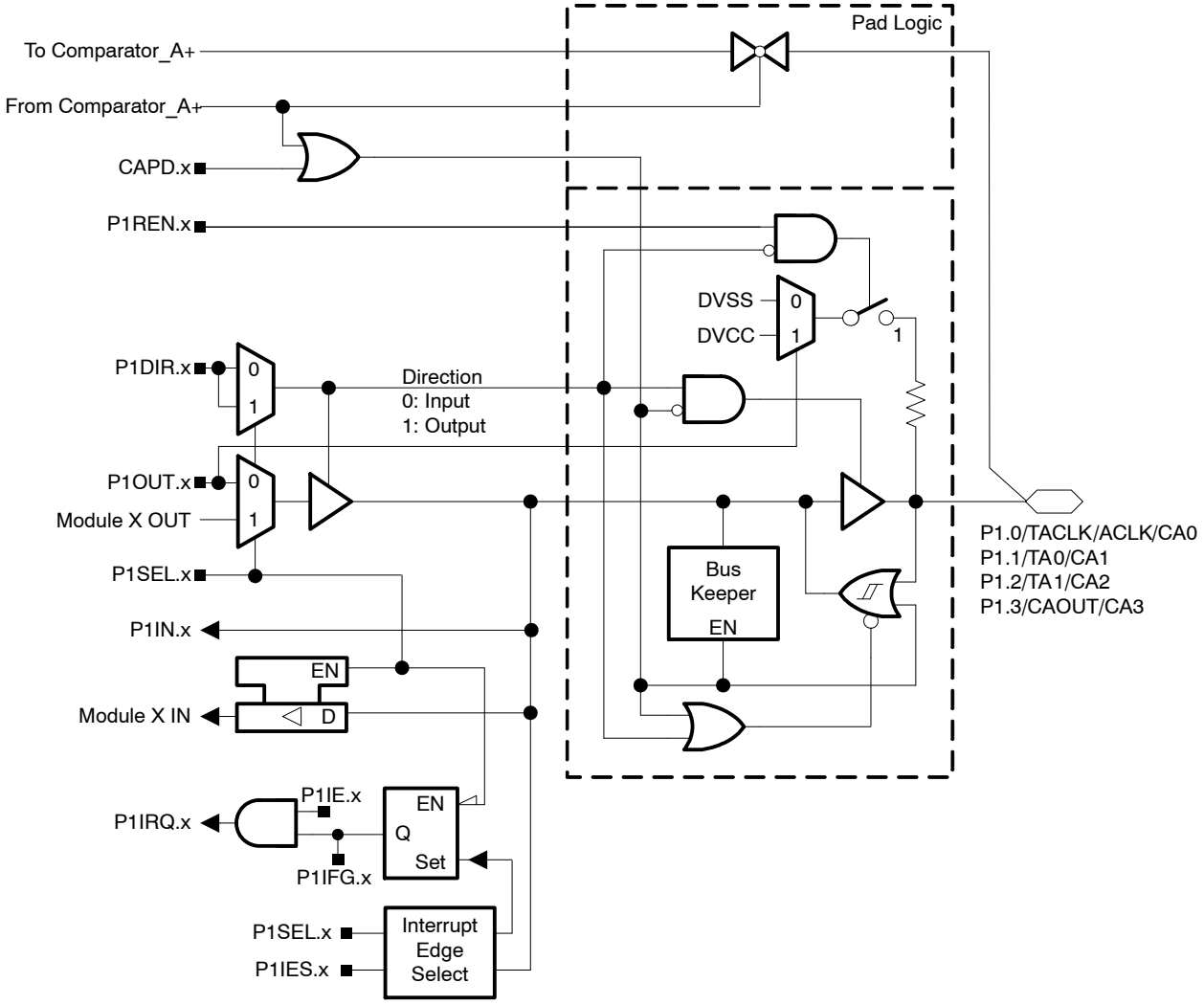
Port P1 (P1.0 to P1.3) pin functions, MSP430x20x1

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	CAPD.x
P1.0/TACLK/ACLK/ CA0	0	P1.0† Input/Output	0/1	0	0
		Timer_A2.TACLK/INCLK	0	1	0
		ACLK	1	1	0
		CA0 (see Note 3)	X	X	1
P1.1/TA0/CA1	1	P1.1† Input/Output	0/1	0	0
		Timer_A2.CCI0A	0	1	0
		Timer_A2.TA0	1	1	0
		CA1 (see Note 3)	X	X	1
P1.2/TA1/CA2	2	P1.2† Input/Output	0/1	0	0
		Timer_A2.CCI1A	0	1	0
		Timer_A2.TA1	1	1	0
		CA2 (see Note 3)	X	X	1
P1.3/CAOUT/CA3	3	P1.3† Input/Output	0/1	0	0
		N/A	0	1	0
		CAOUT	1	1	0
		CA3 (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the CAPD.x bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CAx input pin to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

Port P1 (P1.0 to P1.3) pin schematics, MSP430x20x1



Control signal "From Comparator_A+"

PIN NAME	FUNCTION	SIGNAL "FROM COMPARATOR_A+" = 1					
		P2CA4	P2CA0		P2CA3	P2CA2	P2CA1
P1.0/TACLK/ACLK/CA0	CA0	0	1		N/A	N/A	N/A
P1.1/TA0/CA1	CA1	1	0	OR	0	0	1
P1.2/TA1/CA2	CA2	1	1		0	1	0
P1.3/CAOUT/CA3	CA3	N/A	N/A		0	1	1

NOTES: 1. N/A: Not available or not applicable.

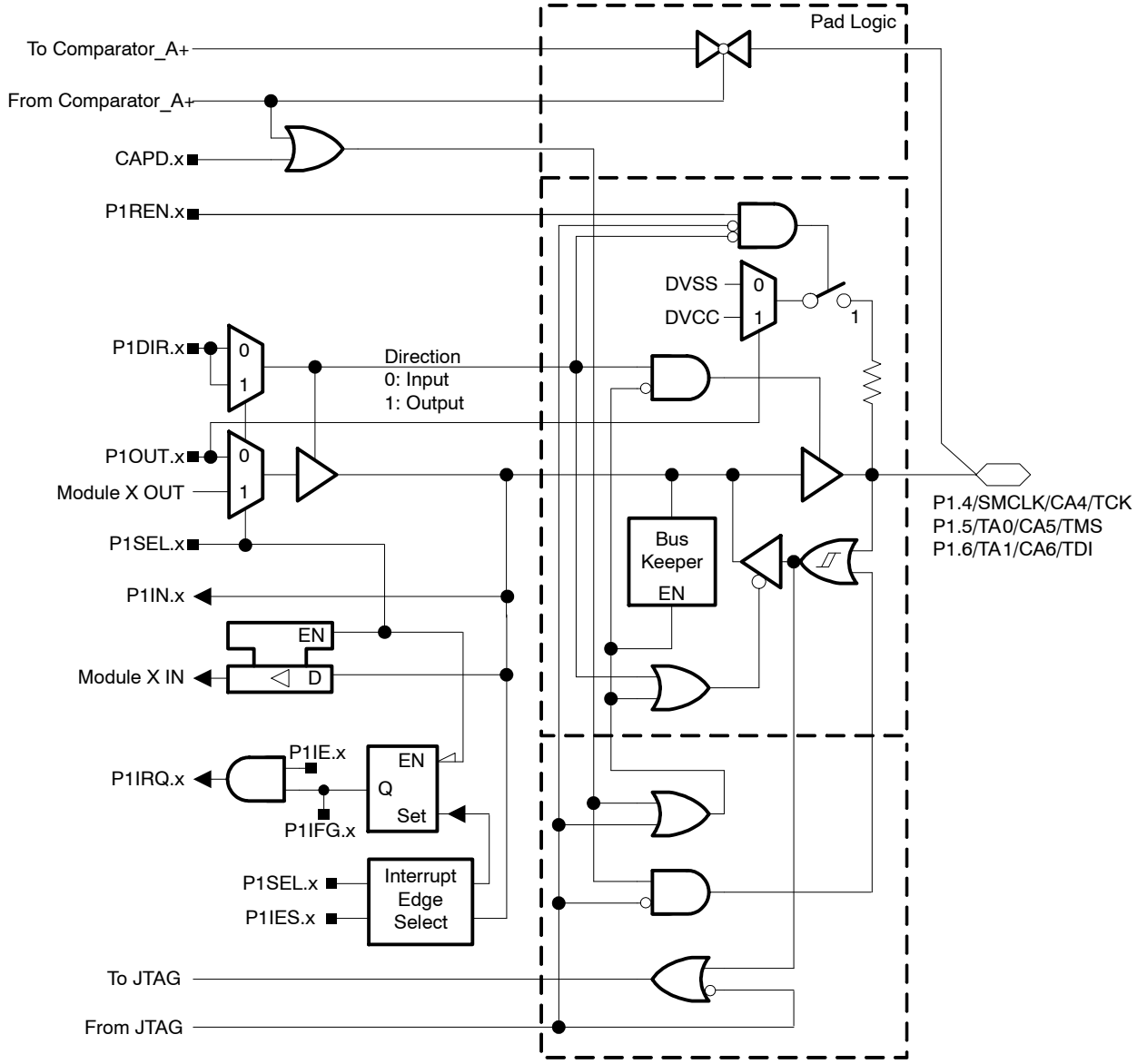
Port P1 (P1.4 to P1.7) pin functions, MSP430x20x1

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P1DIR.x	P1SEL.x	CAPD.x	JTAG Mode
P1.4/SMCLK/CA4/ TCK	4	P1.4† Input/Output	0/1	0	0	0
		N/A	0	1	0	0
		SMCLK	1	1	0	0
		CA4 (see Note 3)	X	X	1	0
		TCK (see Note 4)	X	X	X	1
P1.5/TA0/CA5/ TMS	5	P1.5† Input/Output	0/1	0	0	0
		N/A	0	1	0	0
		Timer_A2.TA0	1	1	0	0
		CA5 (see Note 3)	X	X	1	0
		TMS (see Note 4)	X	X	X	1
P1.6/TA1/CA6/ TDI	6	P1.6† Input/Output	0/1	0	0	0
		N/A	0	1	0	0
		Timer_A2.TA1	1	1	0	0
		CA6 (see Note 3)	X	X	1	0
		TDI (see Note 4)	X	X	X	1
P1.7/CAOUT/CA7/ TDO/TDI	7	P1.7† Input/Output	0/1	0	0	0
		N/A	0	1	0	0
		CAOUT	1	1	0	0
		CA7 (see Note 3)	X	X	1	0
		TDO/TDI (see Notes 4, 5)	X	X	X	1

† Default after reset (PUC/POR)

NOTES:
1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the CAPD.x bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CAx input pin to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.
4. In JTAG mode the internal pull-up/down resistors are disabled.
5. Function controlled by JTAG

Port P1 (P1.4 to P1.6) pin schematics, MSP430x20x1

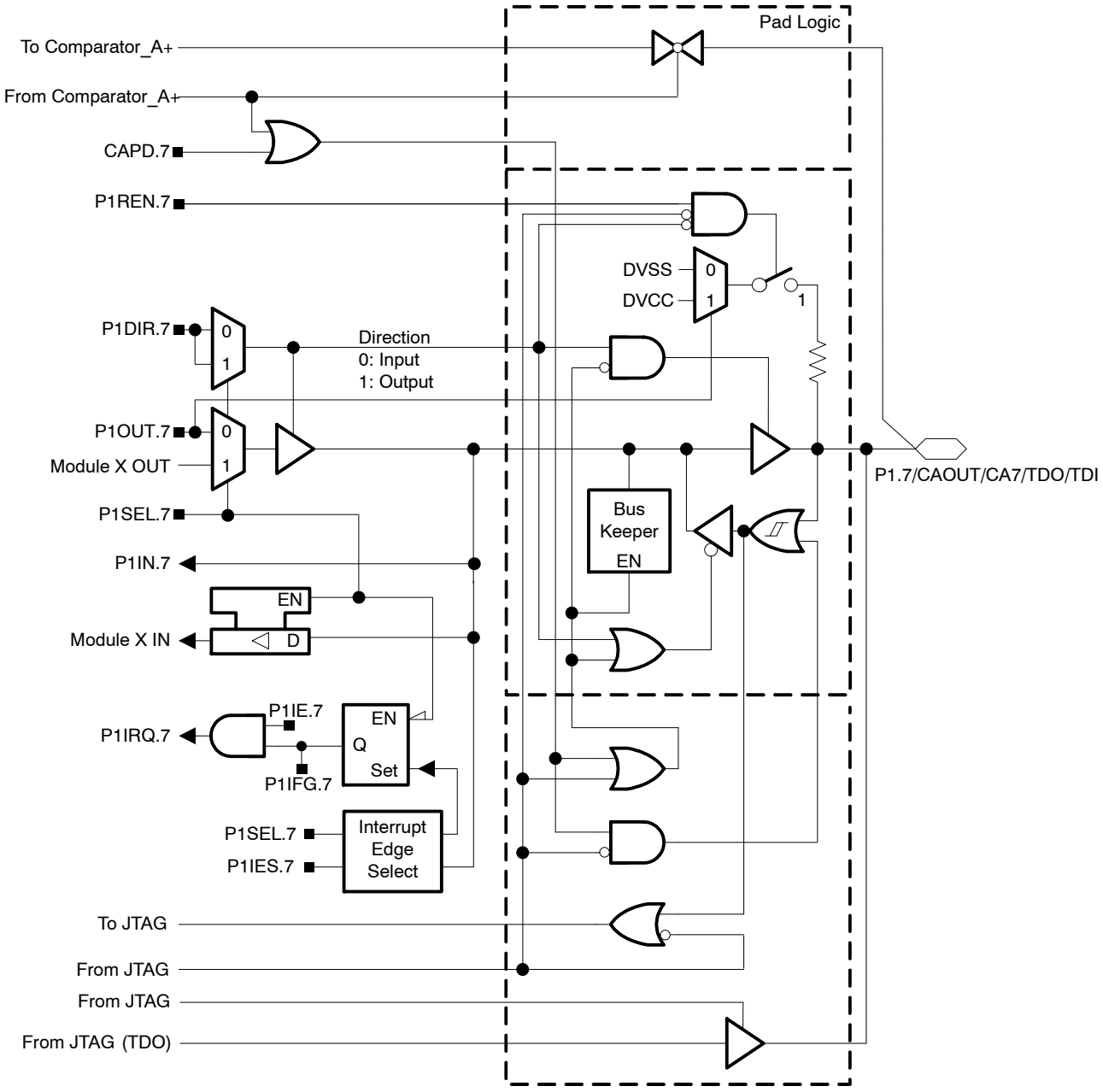


Control signal “From Comparator_A+”

PIN NAME	FUNCTION	SIGNAL “FROM COMPARATOR_A+” = 1		
		P2CA3	P2CA2	P2CA1
P1.4/SMCLK/CA4/TCK	CA4	1	0	0
P1.5/TA0/CA5/TMS	CA5	1	0	1
P1.6/TA1/CA6/TDI	CA6	1	1	0

NOTES: 1. N/A: Not available or not applicable.

Port P1 (P1.7) pin schematics, MSP430x20x1

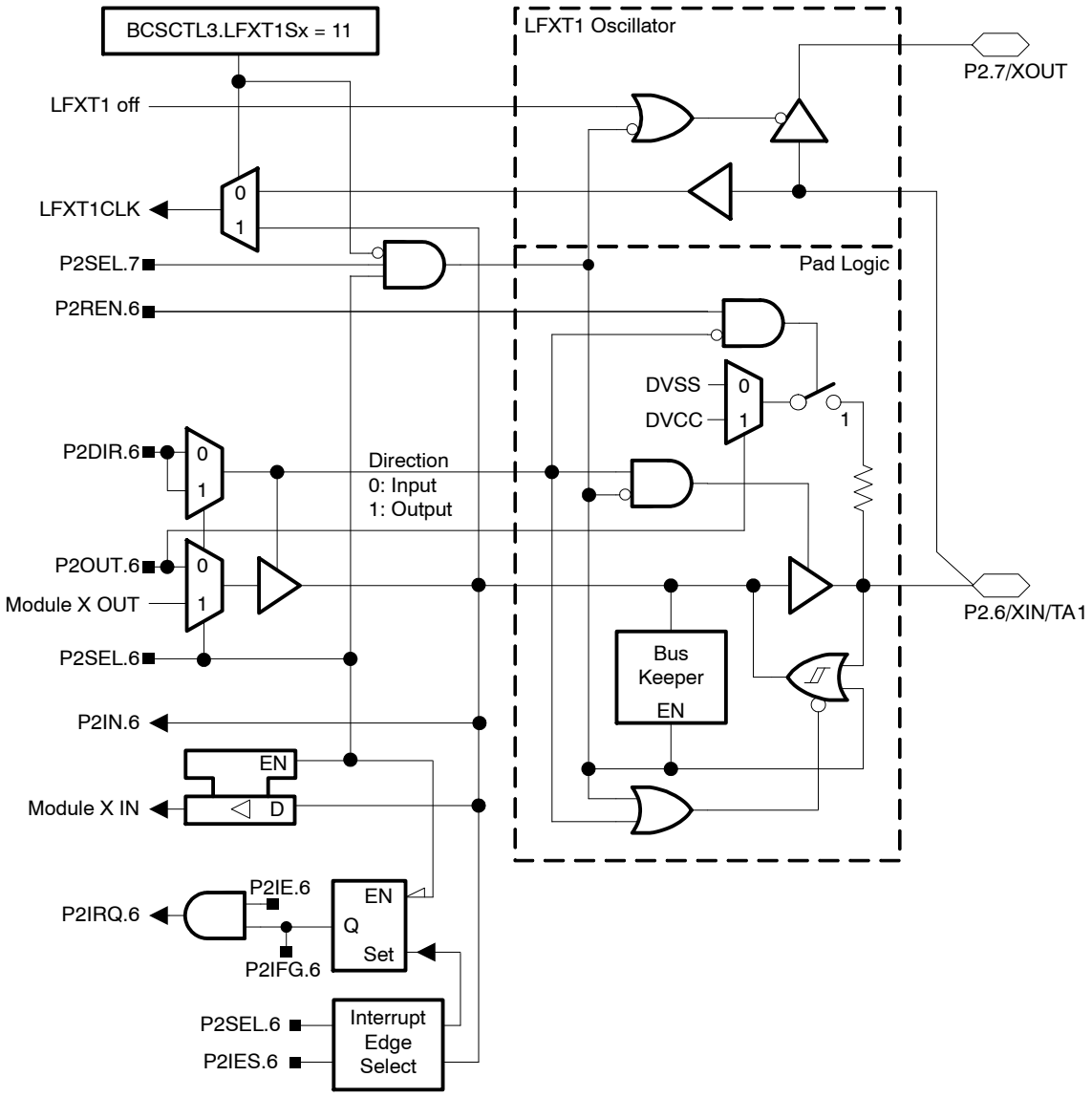


Control signal “From Comparator_A+”

PIN NAME	FUNCTION	SIGNAL “FROM COMPARATOR_A+” = 1		
		P2CA3	P2CA2	P2CA1
P1.7/CAOUT/CA7/TDO/TDI	CA7	1	1	1

NOTES: 1. N/A: Not available or not applicable.

Port P2 (P2.6) pin schematics, MSP430x20x1



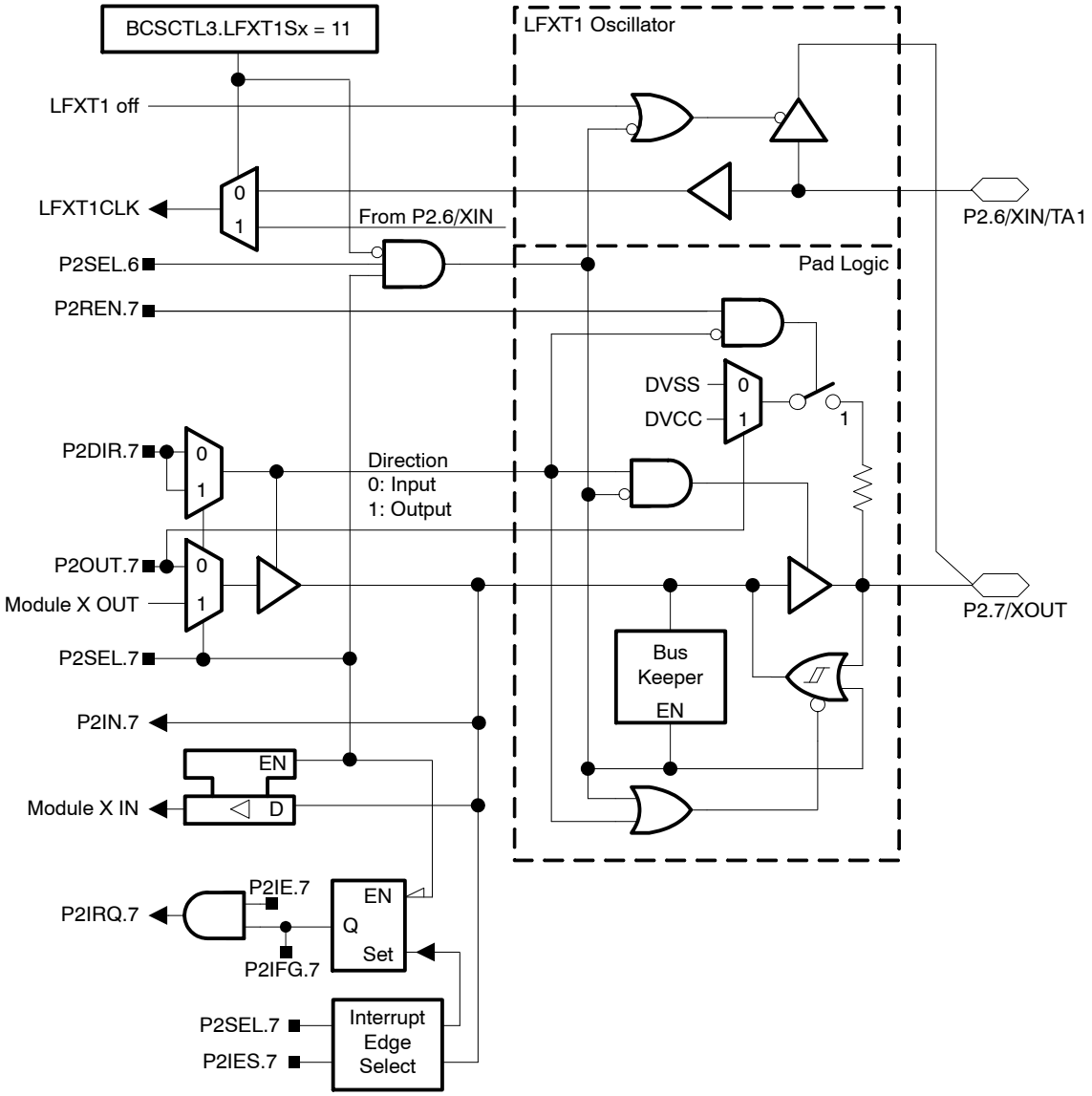
Port P2 (P2.6) pin functions, MSP430x20x1

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.6/XIN/TA1	6	P2.6 Input/Output	0/1	0
		XIN† (see Note 3)	0	1
		Timer_A2.TA1	1	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. XIN is used as digital clock input if the bits LFXT1Sx in register BCSCTL3 are set to 11.

Port P2 (P2.7) pin schematics, MSP430x20x1



Port P2 (P2.7) pin functions, MSP430x20x1

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.7/XOUT	7	P2.7 Input/Output	0/1	0
		DVSS	0	1
		XOUT† (see Note 3)	1	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. If the pin P2.7/XOUT is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

APPLICATION INFORMATION, MSP430x20x2

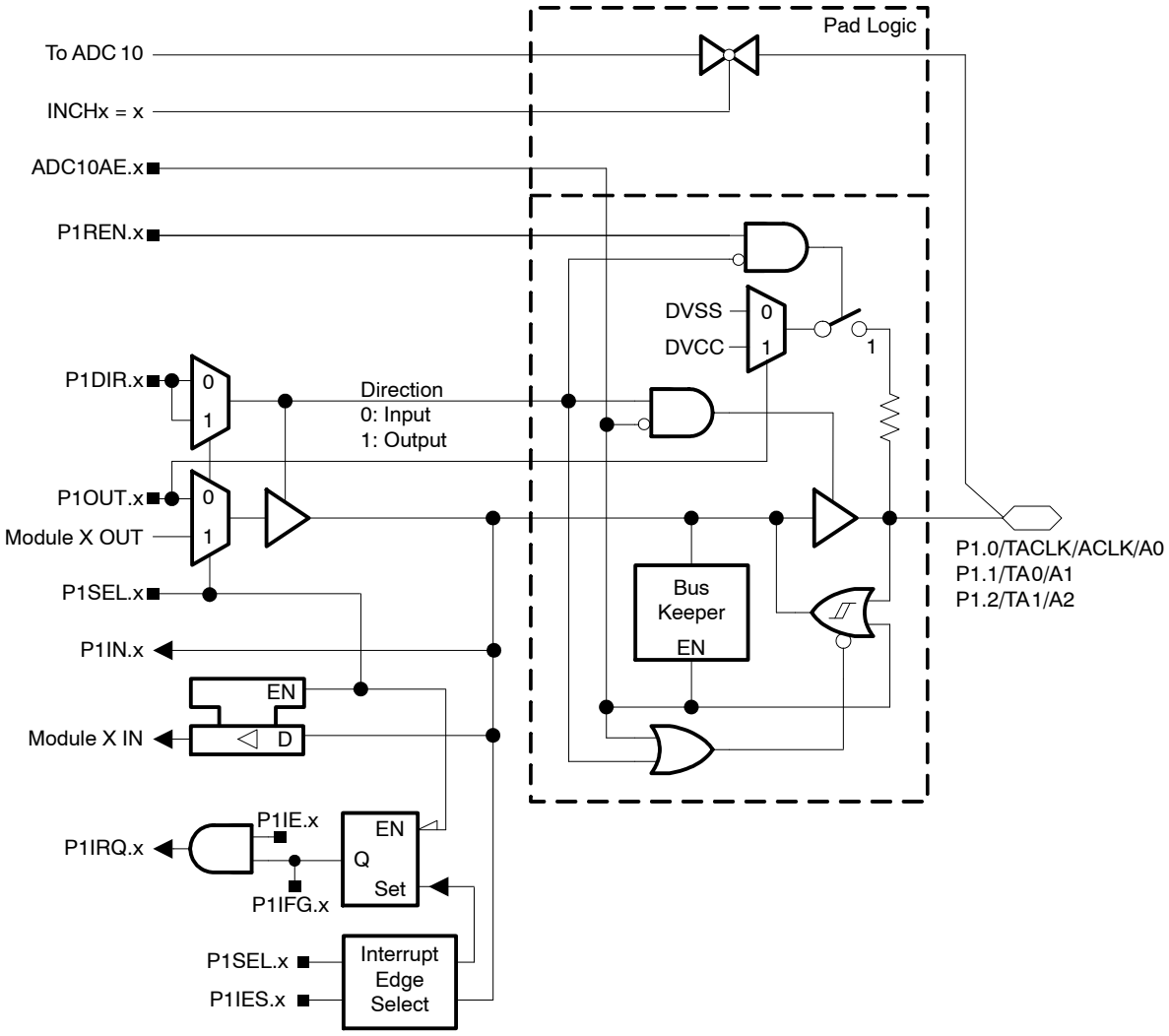
Port P1 (P1.0 to P1.2) pin functions, MSP430x20x2

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P1DIR.x	P1SEL.x	ADC10AE.x	INCHx
P1.0/TACLK/ACLK/A0	0	P1.0† Input/Output	0/1	0	0	N/A
		Timer_A2.TACLK/INCLK	0	1	0	N/A
		ACLK	1	1	0	N/A
		A0 (see Note 3)	X	X	1	0
P1.1/TA0/A1	1	P1.1† Input/Output	0/1	0	0	N/A
		Timer_A2.CCI0A	0	1	0	N/A
		Timer_A2.TA0	1	1	0	N/A
		A1 (see Note 3)	X	X	1	1
P1.2/TA1/A2	2	P1.2† Input/Output	0/1	0	0	N/A
		Timer_A2.CCI1A	0	1	0	N/A
		Timer_A2.TA1	1	1	0	N/A
		A2 (see Note 3)	X	X	1	2

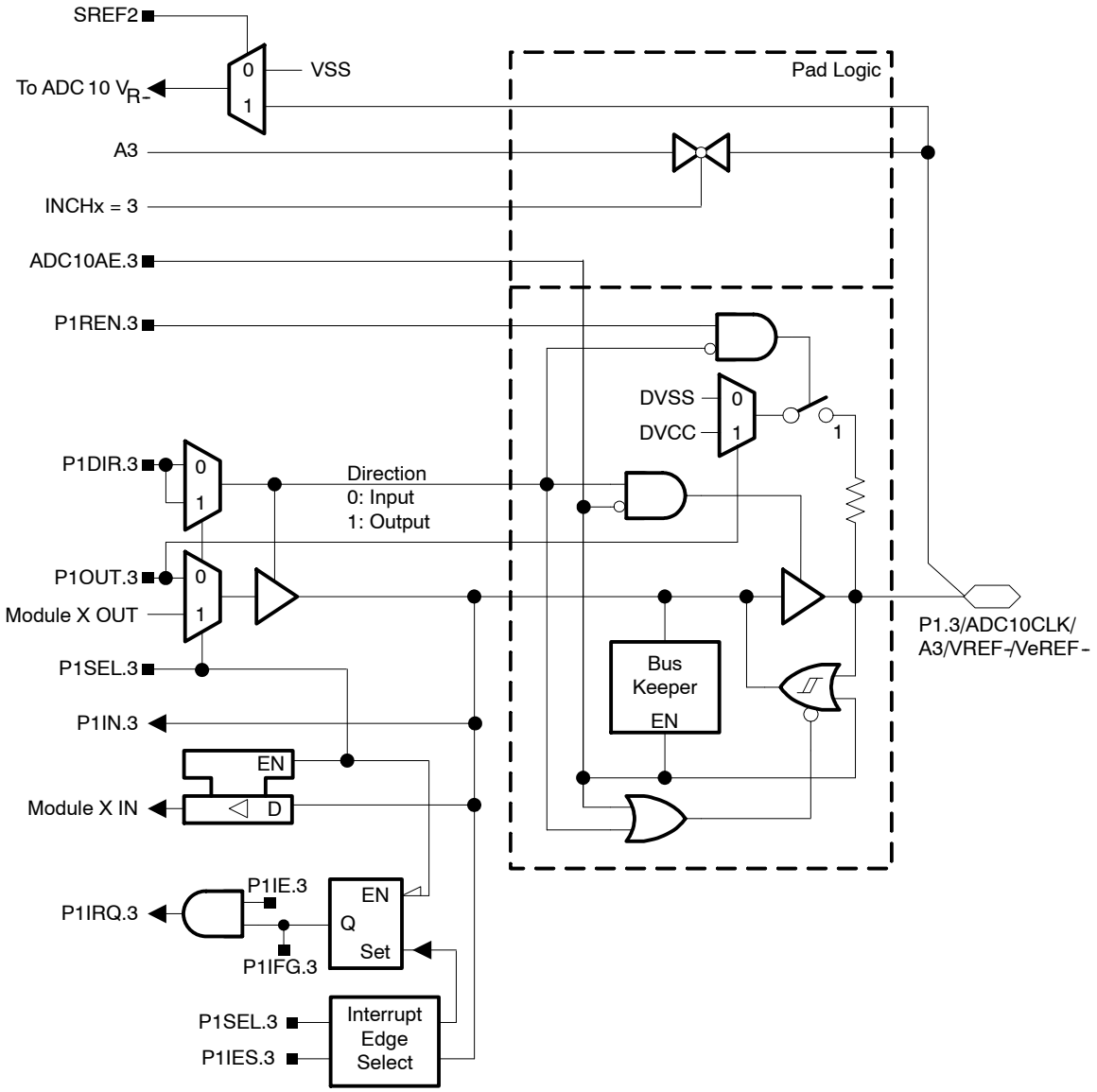
† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the ADC10AE.x bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P1 (P1.0 to P1.2) pin schematics, MSP430x20x2



Port P1 (P1.3) pin schematics, MSP430x20x2



Port P1 (P1.0 to P1.3) pin functions, MSP430x20x2

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P1DIR.x	P1SEL.x	ADC10AE.x	INCHx
P1.3/ADC10CLK/ A3/VREF-/VeREF-	3	P1.3† Input/Output	0/1	0	0	N/A
		N/A	0	1	0	N/A
		ADC10CLK	1	1	0	N/A
		A3 (see Note 3)	X	X	1	3
		VREF-/VeREF- (see Notes 3, 4)	X	X	1	N/A

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the ADC10AE.x bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. An applied voltage is used as negative reference if bit SREF3 in register ADC10CTL0 is set.

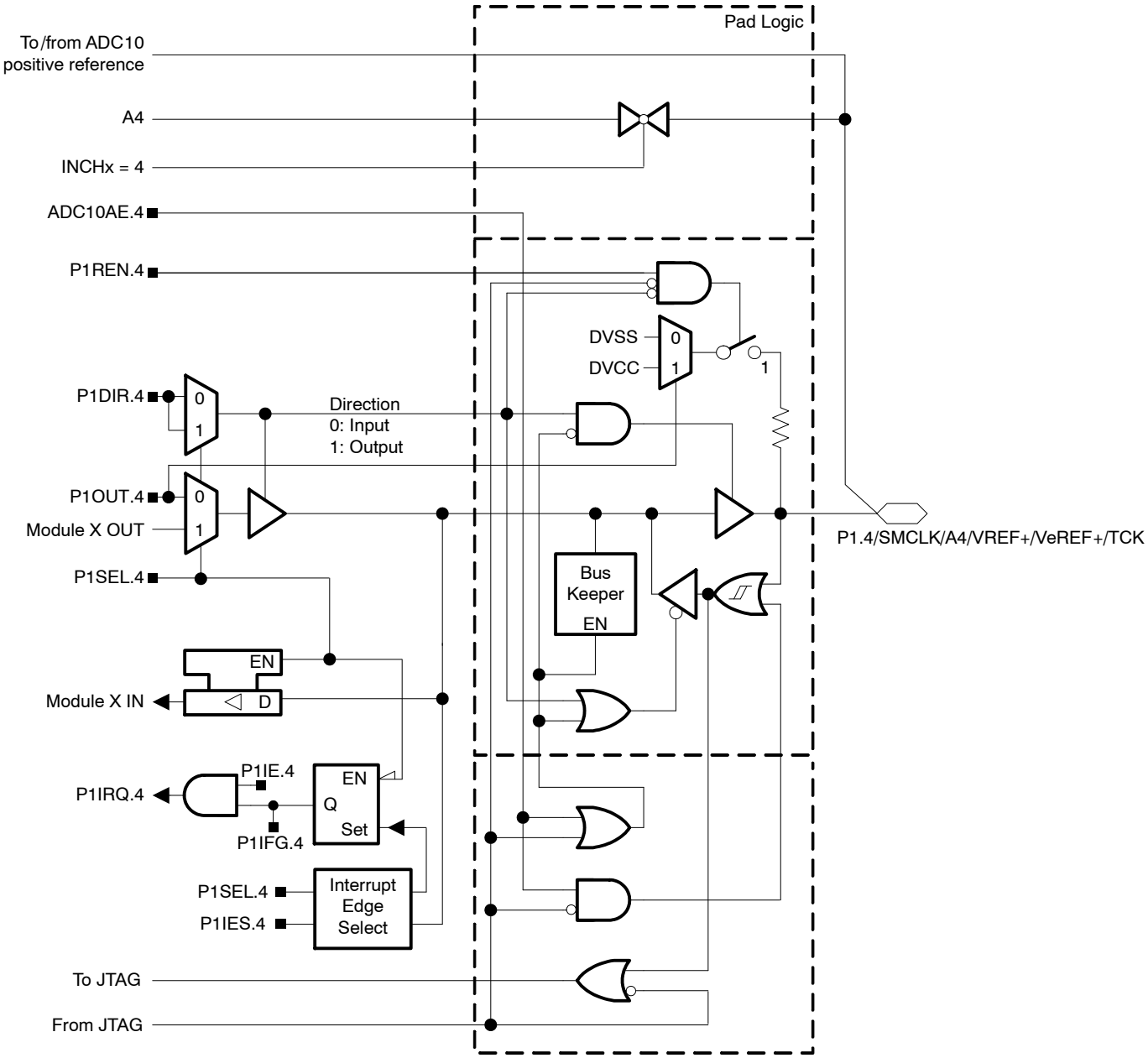
Port P1 (P1.4 to P1.7) pin functions, MSP430x20x2

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS					
			P1DIR.x	P1SEL.x	USIP.x	ADC10AE.x	INCHx	JTAG Mode
P1.4/SMCLK/A4/ VREF+/VeREF+/ TCK	4	P1.4† Input/Output	0/1	0	N/A	0	N/A	0
		N/A	0	1		0	N/A	0
		SMCLK	1	1		0	N/A	0
		A4 (see Note 3)	X	X		1	4	0
		VREF+/VeREF+ (see Notes 3, 4)	X	X		1	N/A	0
		TCK (see Note 5)	X	X		X	X	1
P1.5/TA0/SCLK/A5/ TMS	5	P1.5† Input/Output	0/1	0	X	0	N/A	0
		N/A	0	1	X	0	N/A	0
		Timer_A2.TA0	1	1	X	0	N/A	0
		SCLK	X	X	1	0	N/A	0
		A5 (see Note 3)	X	X	X	1	5	0
		TMS (see Note 5)	X	X	X	X	X	1
P1.6/TA1/SDO/SCL/A6/ TDI	6	P1.6† Input/Output	0/1	0	X	0	N/A	0
		Timer_A2.CCI1B	0	1	X	0	N/A	0
		Timer_A2.TA1	1	1	X	0	N/A	0
		SDO (SPI) / SCL (I2C)	X	X	1	0	N/A	0
		A6 (see Note 3)	X	X	X	1	6	0
		TDI (see Note 5)	X	X	X	X	X	1
P1.7/SDI/SDA/A7/ TDO/TDI	7	P1.7† Input/Output	0/1	0	X	0	N/A	0
		N/A	0	1	X	0	N/A	0
		DVSS	1	1	X	0	N/A	0
		SDI (SPI) / SDA (I2C)	X	X	1	0	N/A	0
		A7 (see Note 3)	X	X	X	1	7	0
		TDO/TDI (see Notes 5, 6)	X	X	X	X	X	1

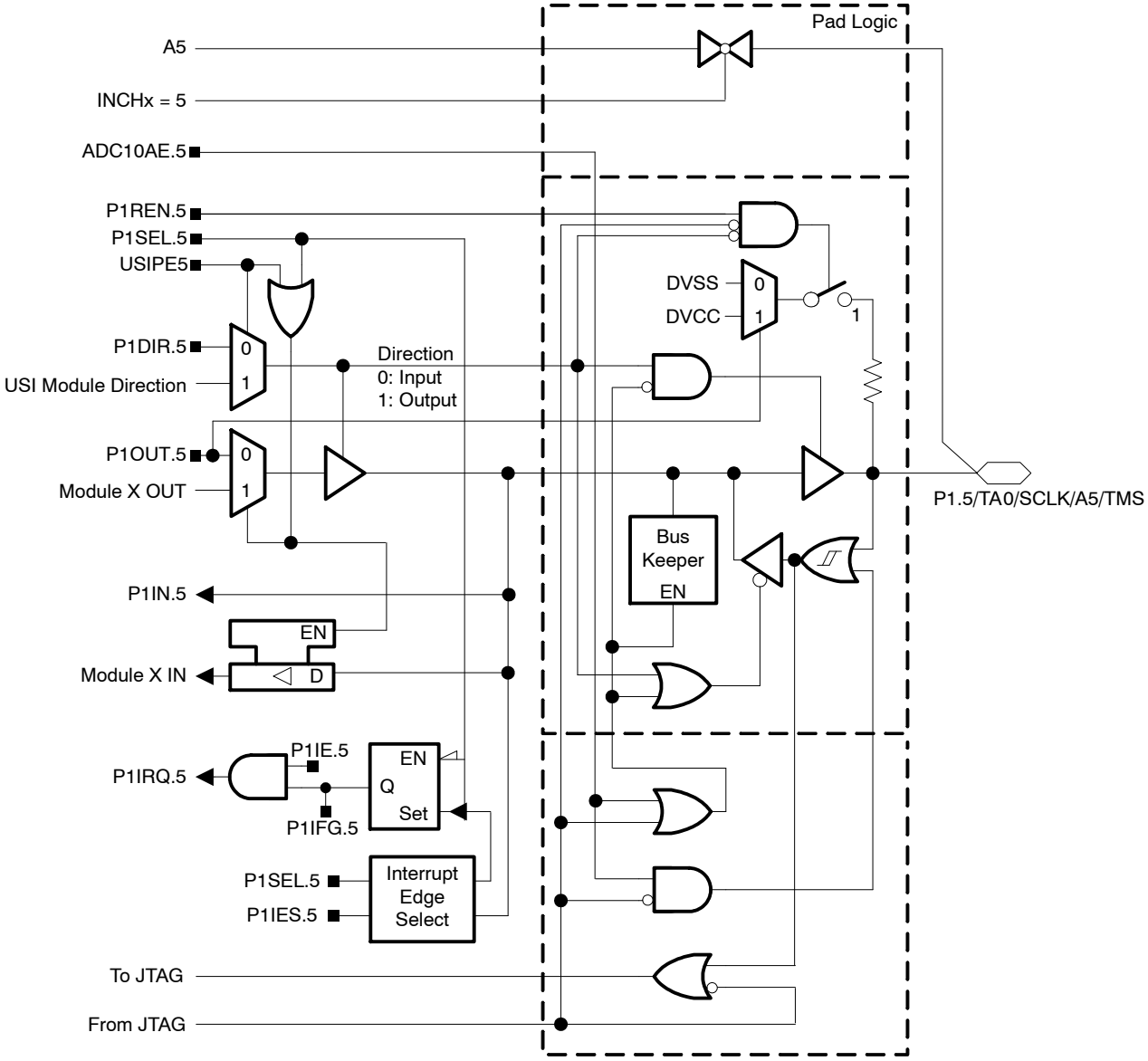
† Default after reset (PUC/POR)

NOTES:
1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the ADC10AE.x bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. The reference voltage is output if bit REFOUT in register ADC10CTL0 is set. An applied voltage is used as positive reference if bits SREF0/1 in register ADC10CTL0 are set to 10 or 11.
5. In JTAG mode the internal pull-up/down resistors are disabled.
6. Function controlled by JTAG

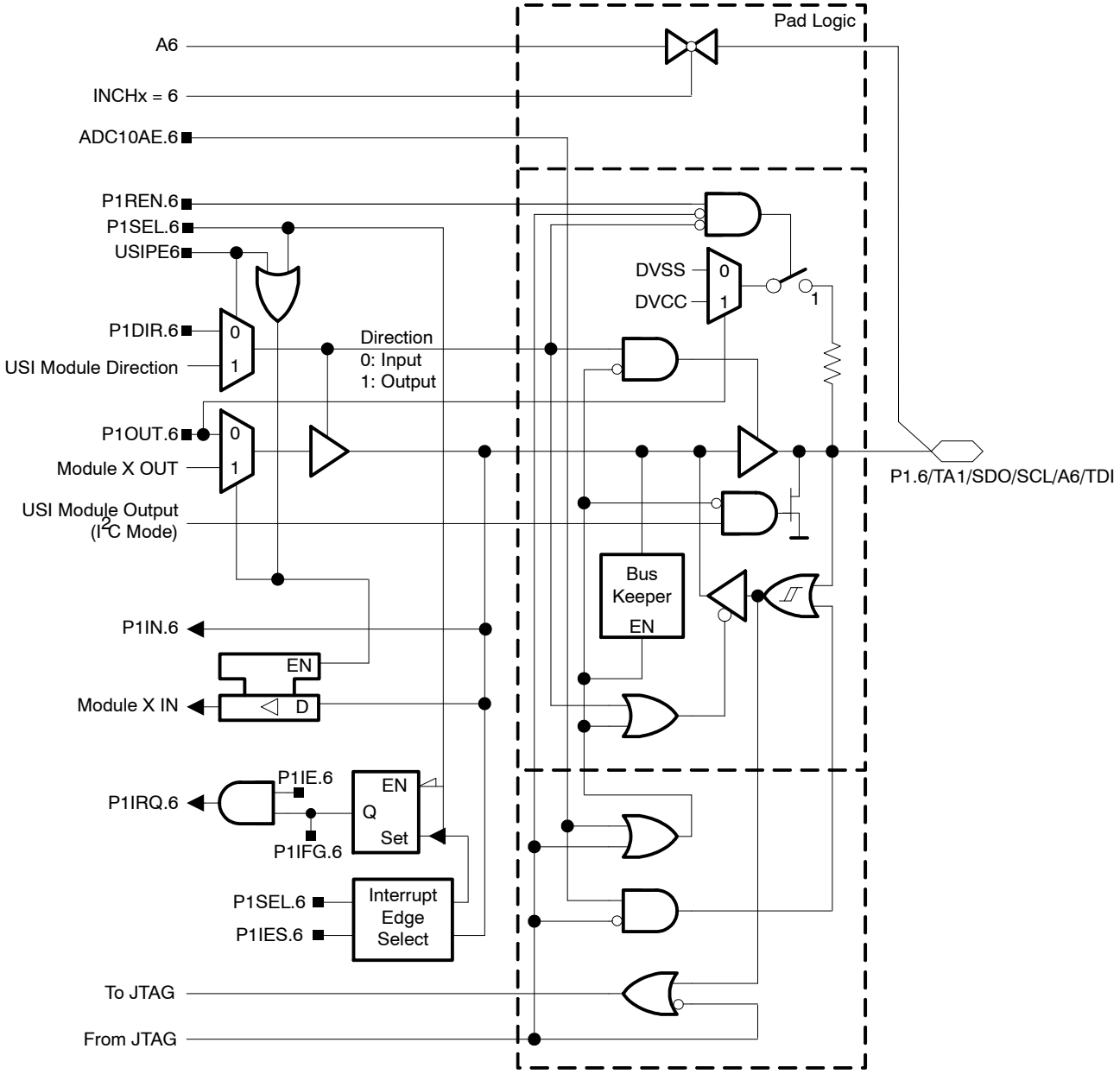
Port P1 (P1.4) pin schematics, MSP430x20x2



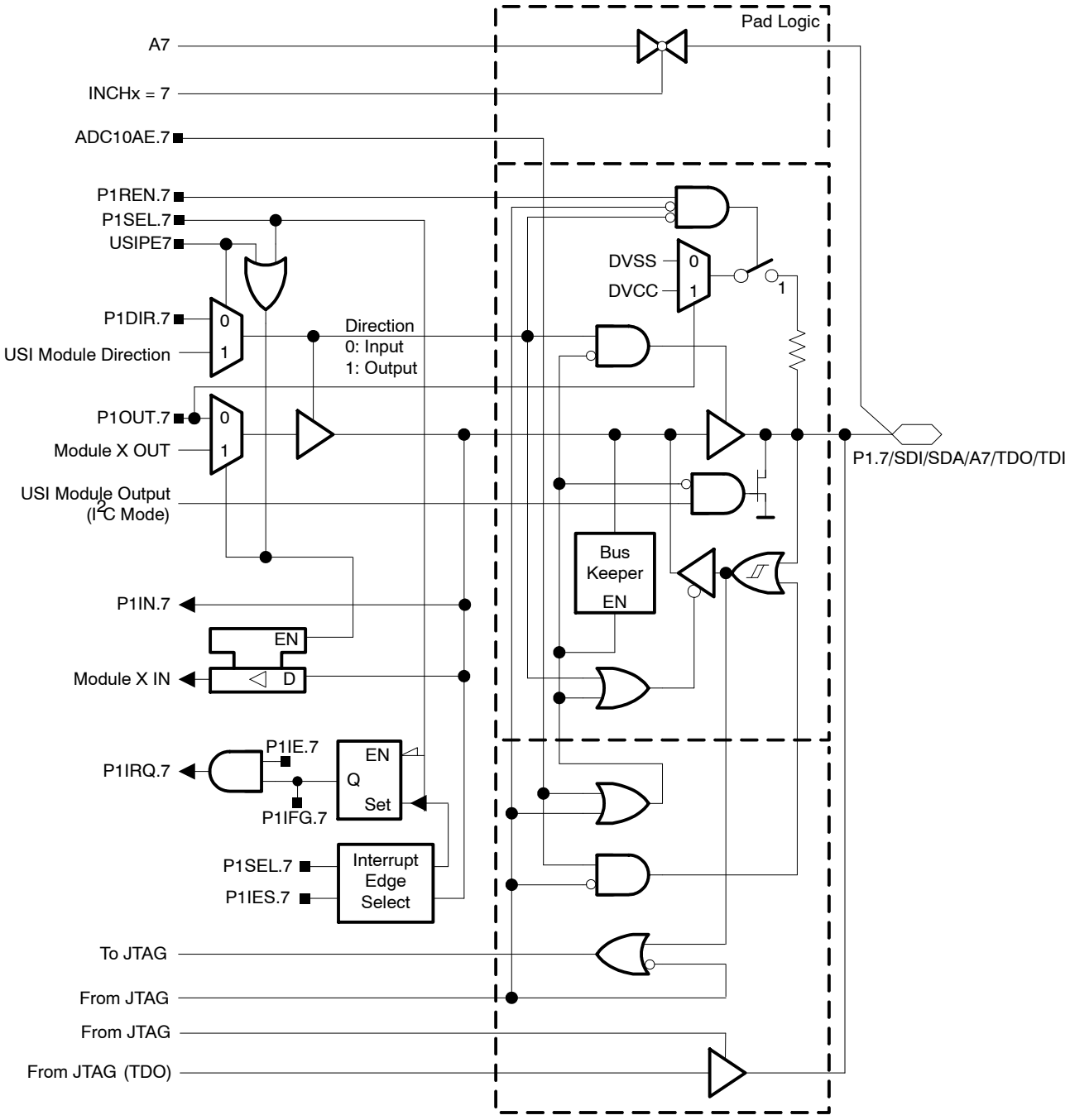
Port P1 (P1.5) pin schematics, MSP430x20x2



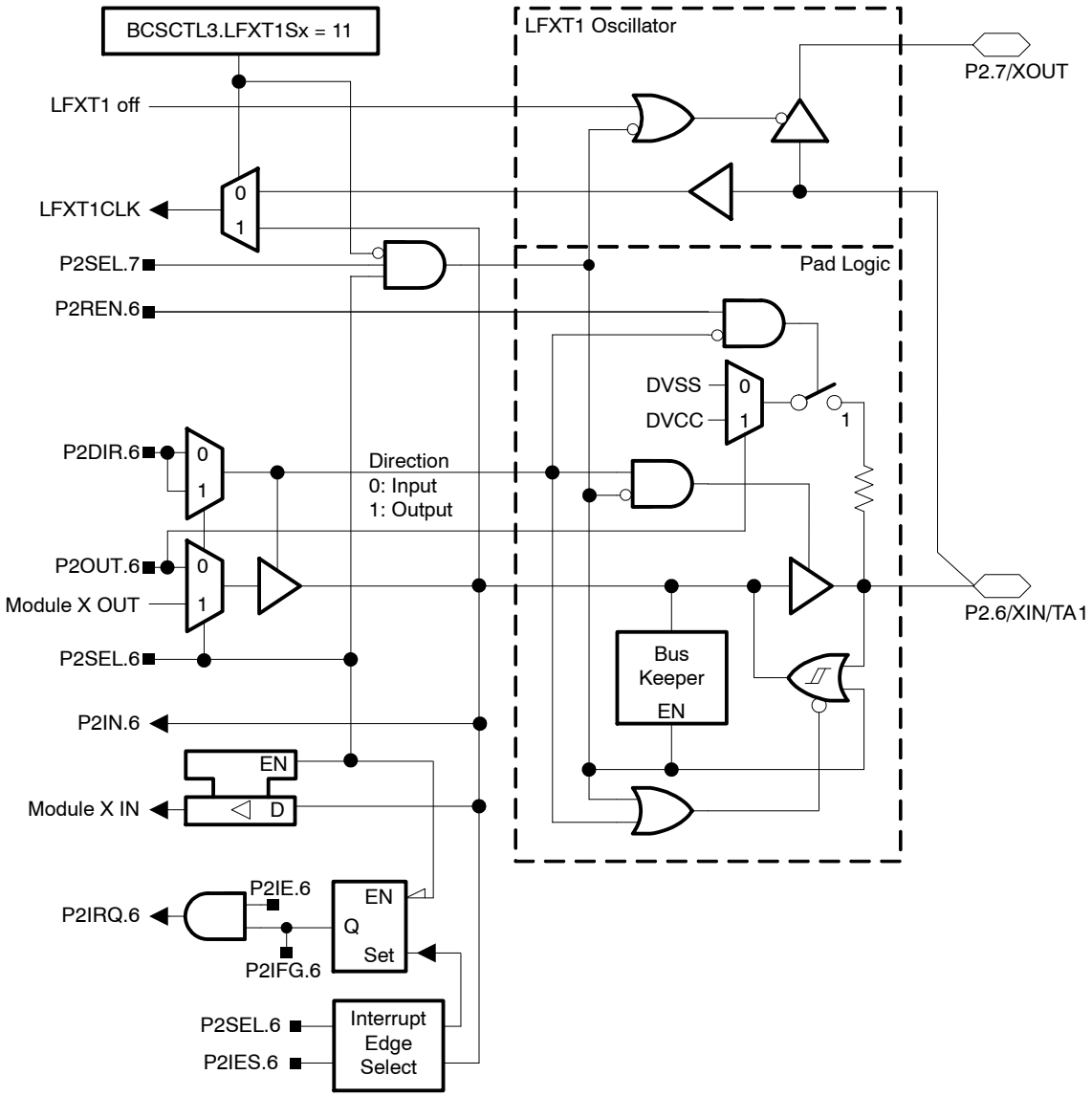
Port P1 (P1.6) pin schematics, MSP430x20x2



Port P1 (P1.7) pin schematics, MSP430x20x2



Port P2 (P2.6) pin schematics, MSP430x20x2



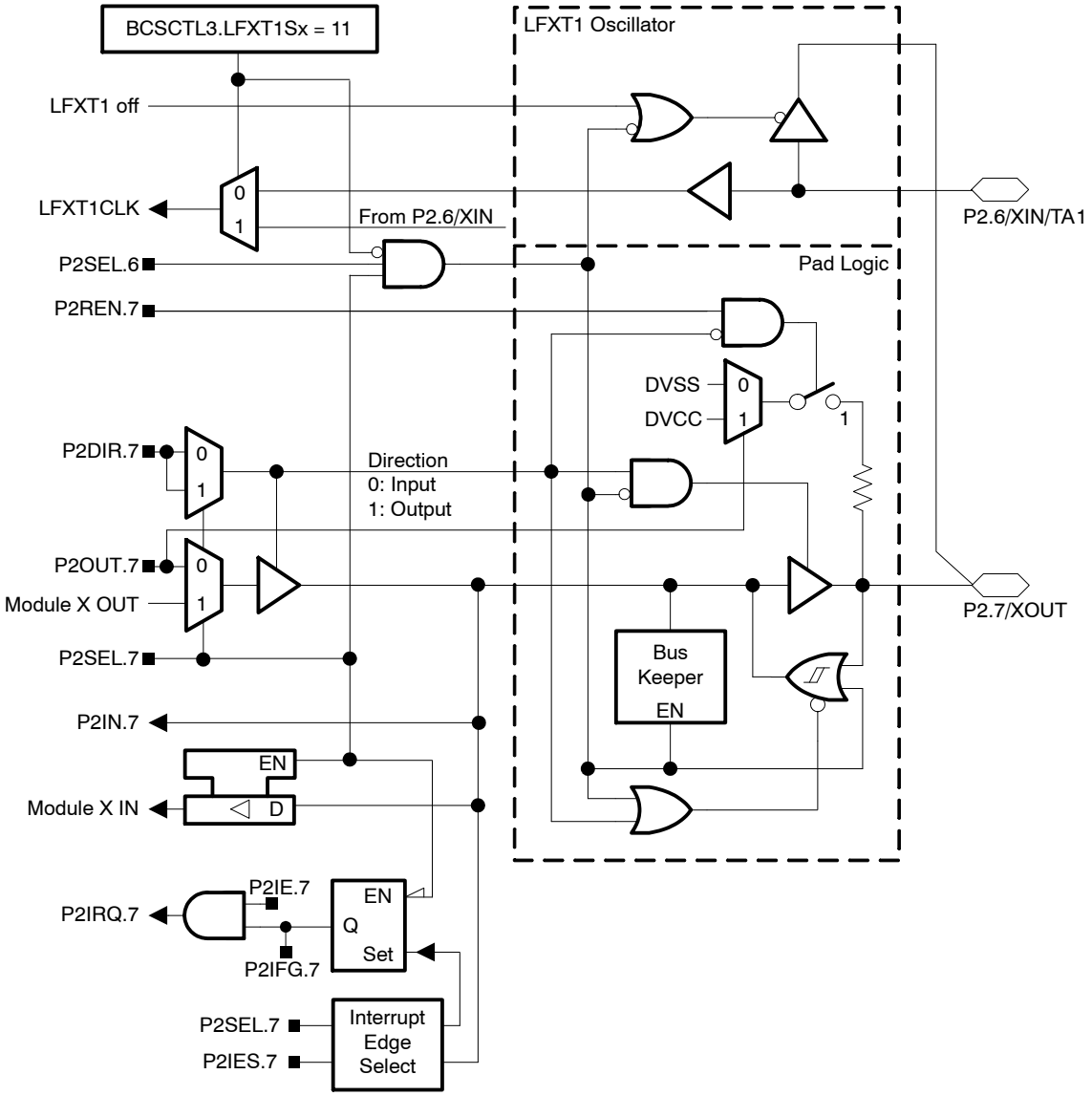
Port P2 (P2.6) pin functions, MSP430x20x2

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.6/XIN/TA1	6	P2.6 Input/Output	0/1	0
		XIN† (see Note 3)	0	1
		Timer_A2.TA1	1	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. XIN is used as digital clock input if the bits LFXT1Sx in register BCSCTL3 are set to 11.

Port P2 (P2.7) pin schematics, MSP430x20x2



Port P2 (P2.7) pin functions, MSP430x20x2

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.7/XOUT	7	P2.7 Input/Output	0/1	0
		DVSS	0	1
		XOUT† (see Note 3)	1	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. If the pin P2.7/XOUT is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

APPLICATION INFORMATION, MSP430x20x3

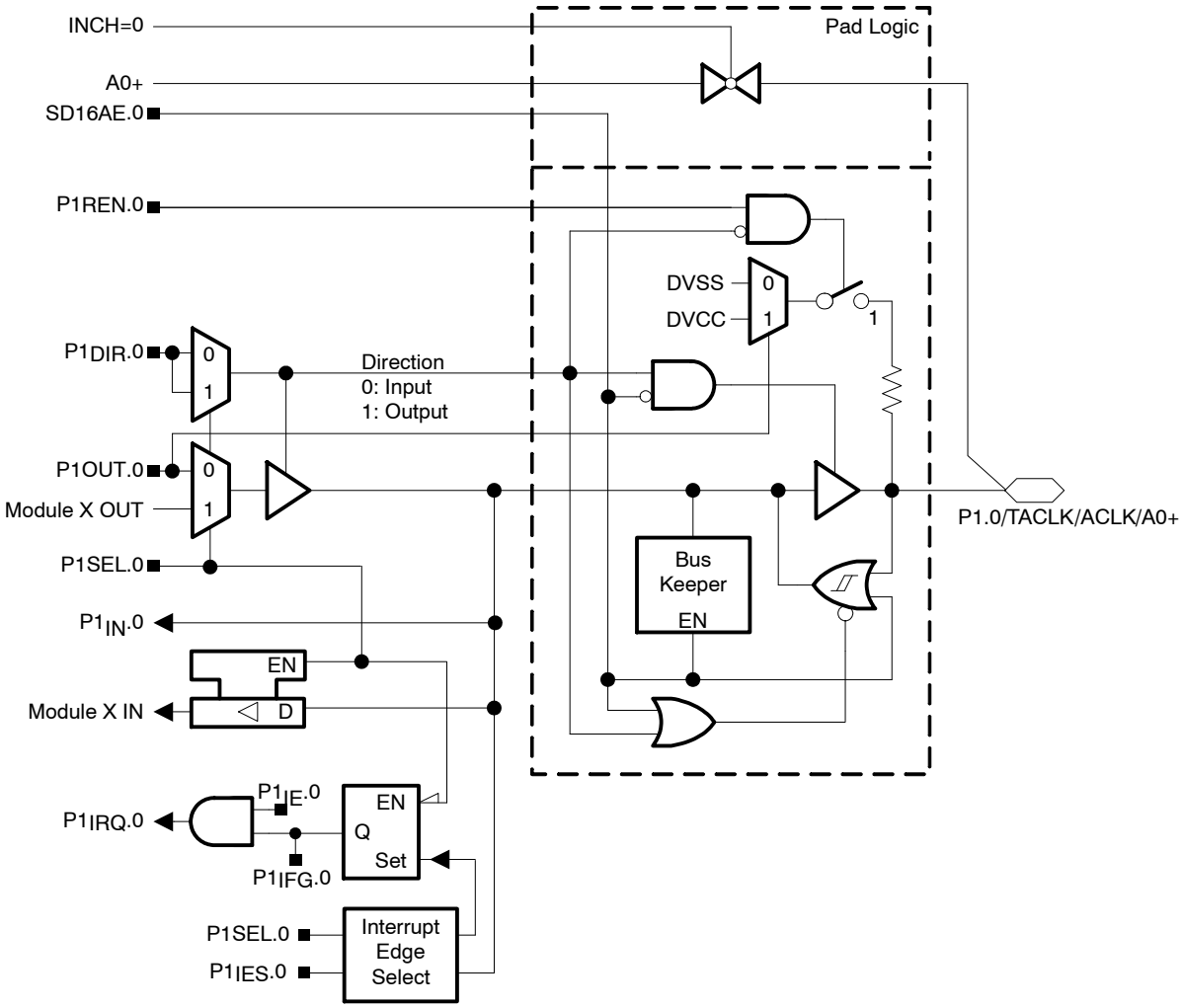
Port P1 (P1.0 to P1.3) pin functions, MSP430x20x3

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P1DIR.x	P1SEL.x	SD16AE.x	INCHx
P1.0/TACLK/ACLK/A0+	0	P1.0† Input/Output	0/1	0	0	N/A
		Timer_A2.TACLK/INCLK	0	1	0	N/A
		ACLK	1	1	0	N/A
		A0+ (see Note 3)	X	X	1	0
P1.1/TA0/A0–/A4+	1	P1.1† Input/Output	0/1	0	0	N/A
		Timer_A2.CCI0A	0	1	0	N/A
		Timer_A2.TA0	1	1	0	N/A
		A0– (see Notes 3, 4)	X	X	1	0
		A4+ (see Note 3)	X	X	1	4
P1.2/TA1/A1+/A4–	2	P1.2† Input/Output	0/1	0	0	N/A
		Timer_A2.CCI1A	0	1	0	N/A
		Timer_A2.TA1	1	1	0	N/A
		A1+ (see Note 3)	X	X	1	1
		A4– (see Notes 3, 4)	X	X	1	4
P1.3/VREF/A1–	3	P1.3† Input/Output	0/1	0	0	N/A
		VREF	X	1	0	N/A
		A1– (see Notes 3, 4)	X	X	1	1

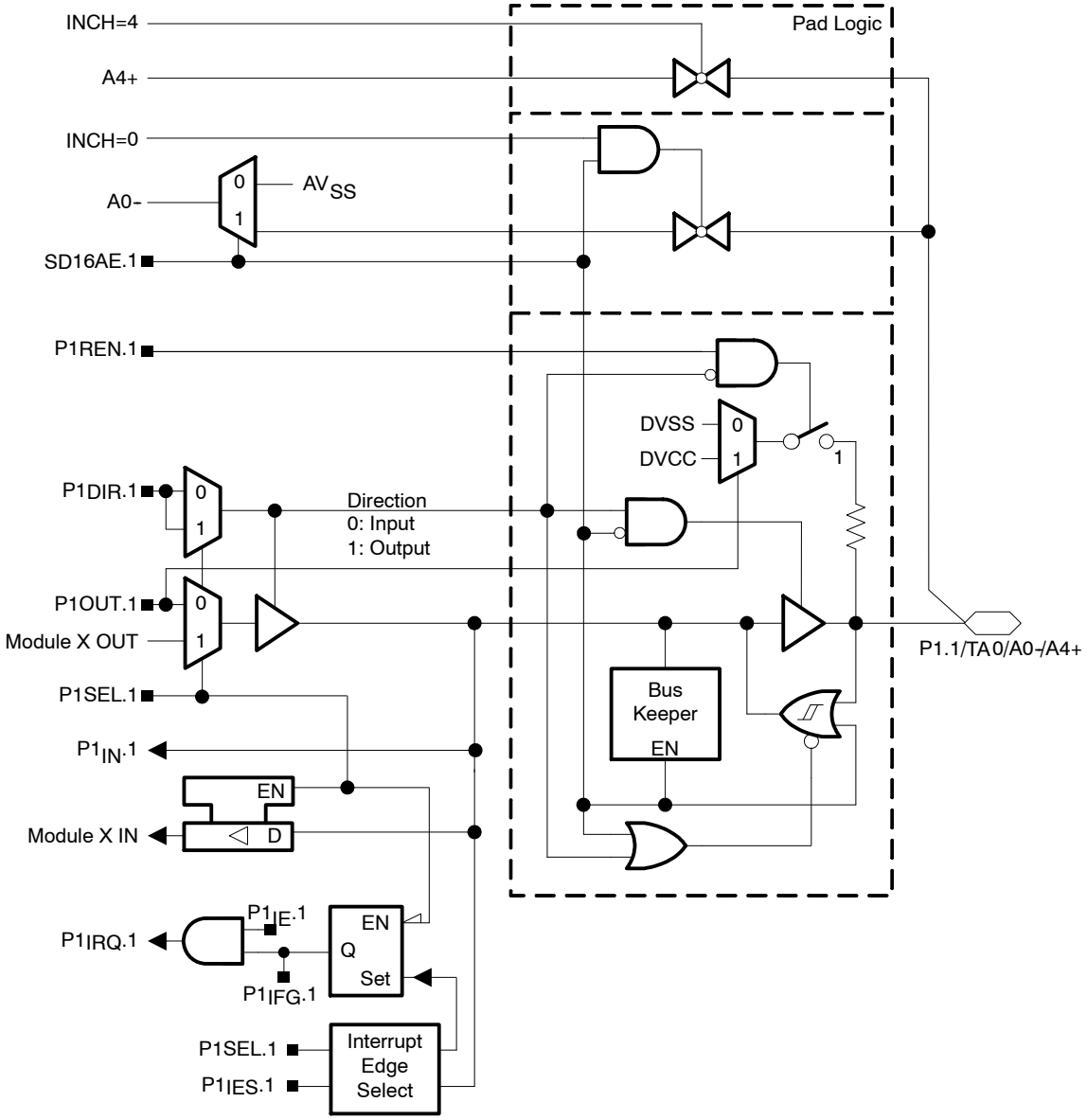
† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the SD16AE.x bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. With SD16AE.x = 0 the negative inputs are connected to VSS if the corresponding input is selected.

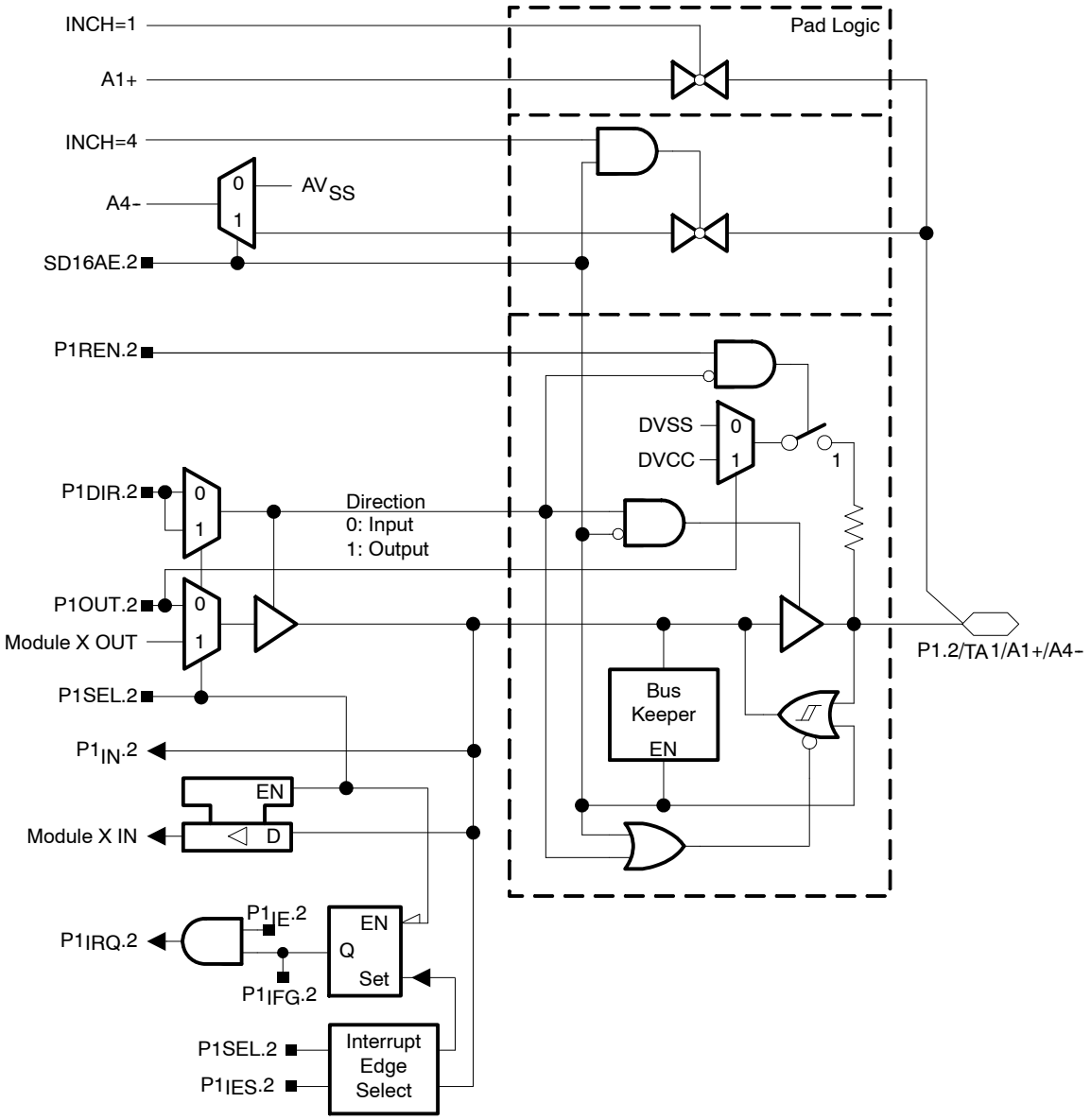
Port P1 (P1.0) pin schematics, MSP430x20x3



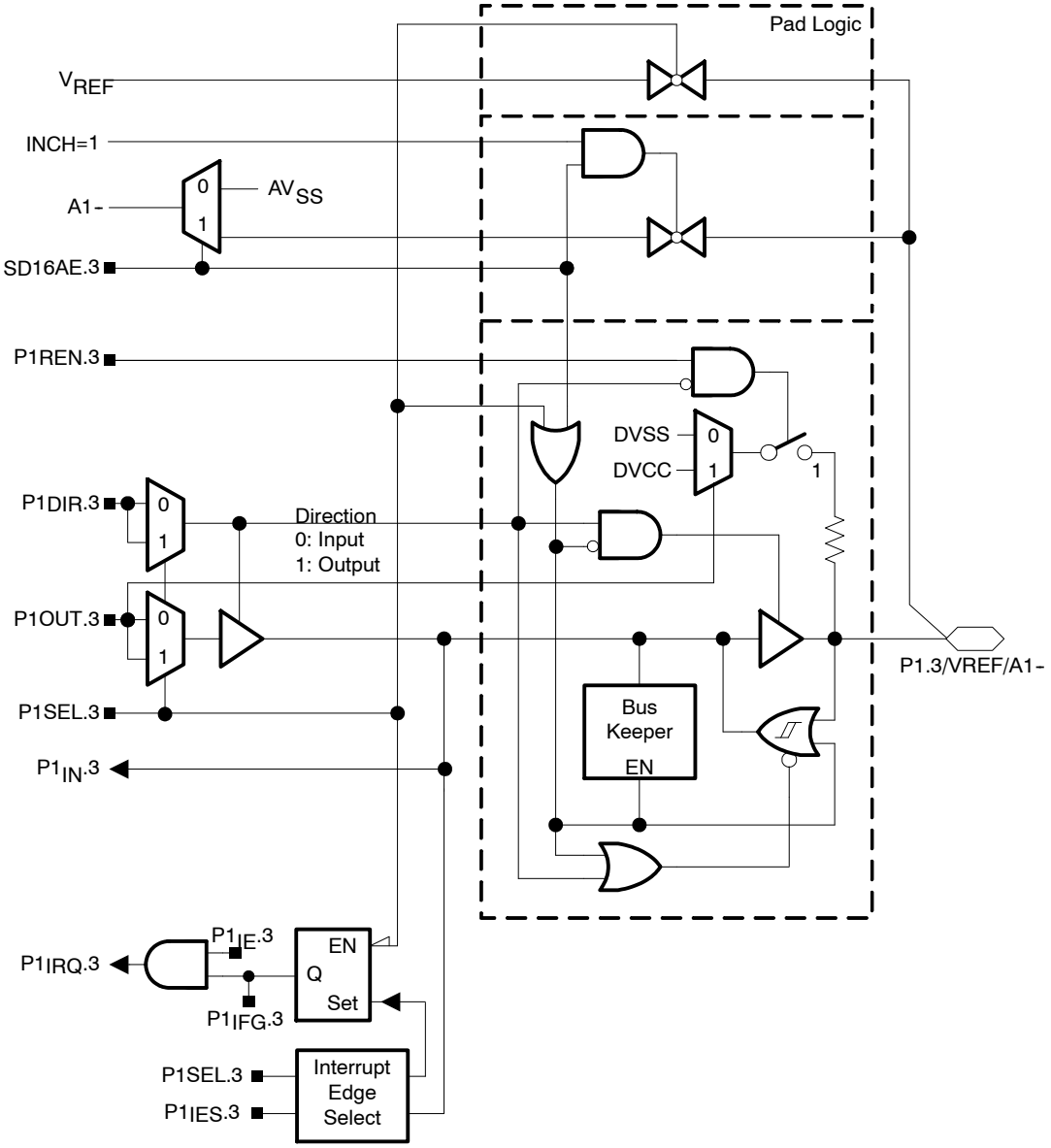
Port P1 (P1.1) pin schematics, MSP430x20x3



Port P1 (P1.2) pin schematics, MSP430x20x3



Port P1 (P1.3) pin schematics, MSP430x20x3



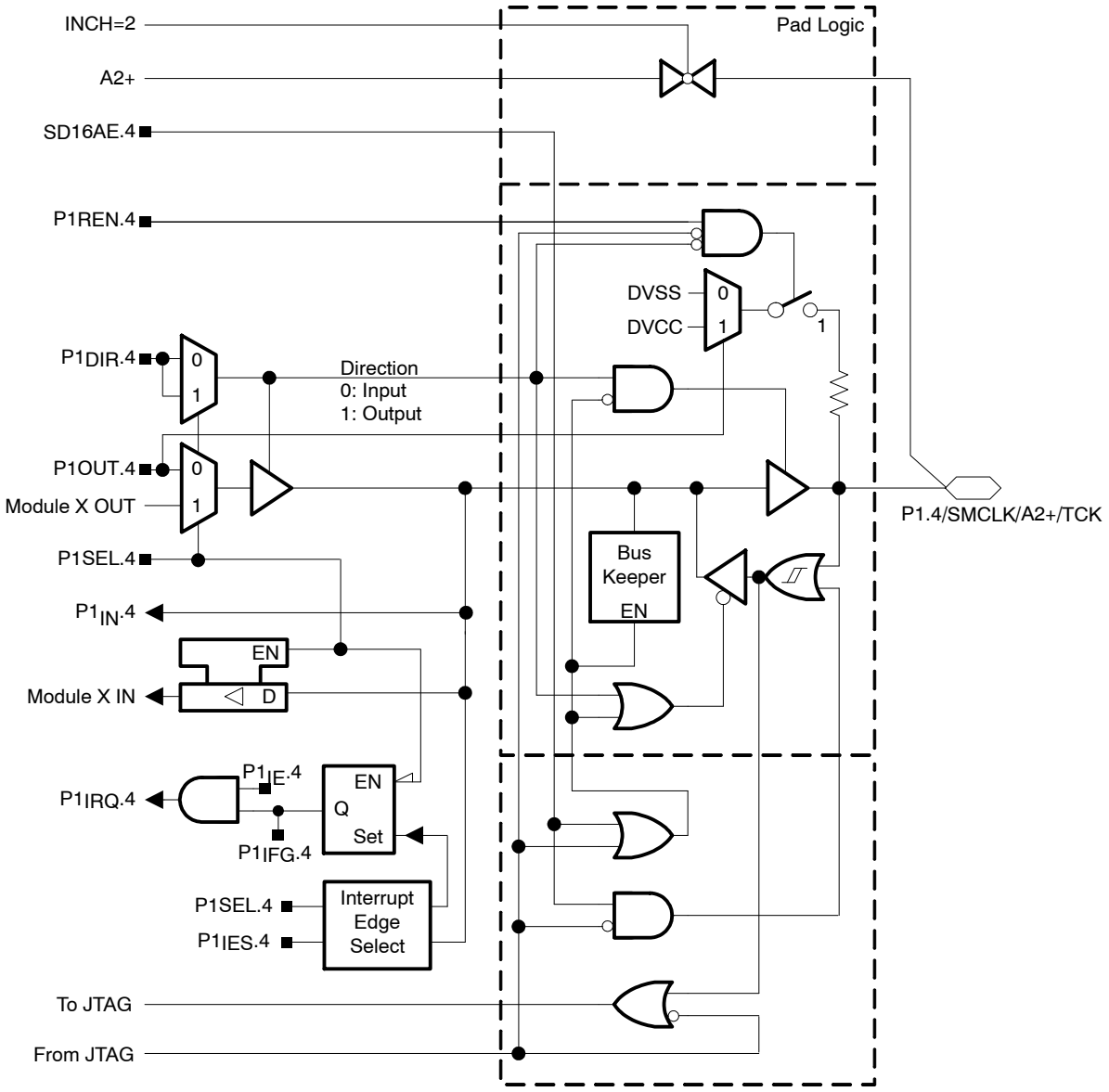
Port P1 (P1.4 to P1.7) pin functions, MSP430x20x3

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS					
			P1DIR.x	P1SEL.x	USIP.x	SD16AE.x	INCHx	JTAG Mode
P1.4/SMCLK/A2+/ TCK	4	P1.4† Input/Output	0/1	0	N/A	0	N/A	0
		N/A	0	1	N/A	0	N/A	0
		SMCLK	1	1	N/A	0	N/A	0
		A2+ (see Note 3)	X	X	N/A	1	2	0
		TCK (see Note 5)	X	X	N/A	X	X	1
P1.5/TA0/SCLK/A2–/ TMS	5	P1.5† Input/Output	0/1	0	X	0	N/A	0
		N/A	0	1	X	0	N/A	0
		Timer_A2.TA0	1	1	X	0	N/A	0
		SCLK	X	X	1	0	N/A	0
		A2– (see Notes 3, 4)	X	X	X	1	2	0
		TMS (see Note 5)	X	X	X	X	X	1
P1.6/TA1/SDO/SCL/A3+/ TDI	6	P1.6† Input/Output	0/1	0	X	0	N/A	0
		Timer_A2.CCI1B	0	1	X	0	N/A	0
		Timer_A2.TA1	1	1	X	0	N/A	0
		SDO (SPI) / SCL (I2C)	X	X	1	0	N/A	0
		A3+ (see Note 3)	X	X	X	1	3	0
		TDI (see Note 5)	X	X	X	X	X	1
P1.7/SDI/SDA/A3–/ TDO/TDI	7	P1.7† Input/Output	0/1	0	X	0	N/A	0
		N/A	0	1	X	0	N/A	0
		DVSS	1	1	X	0	N/A	0
		SDI (SPI) / SDA (I2C)	X	X	1	0	N/A	0
		A3– (see Notes 3, 4)	X	X	X	1	3	0
		TDO/TDI (see Notes 5, 6)	X	X	X	X	X	1

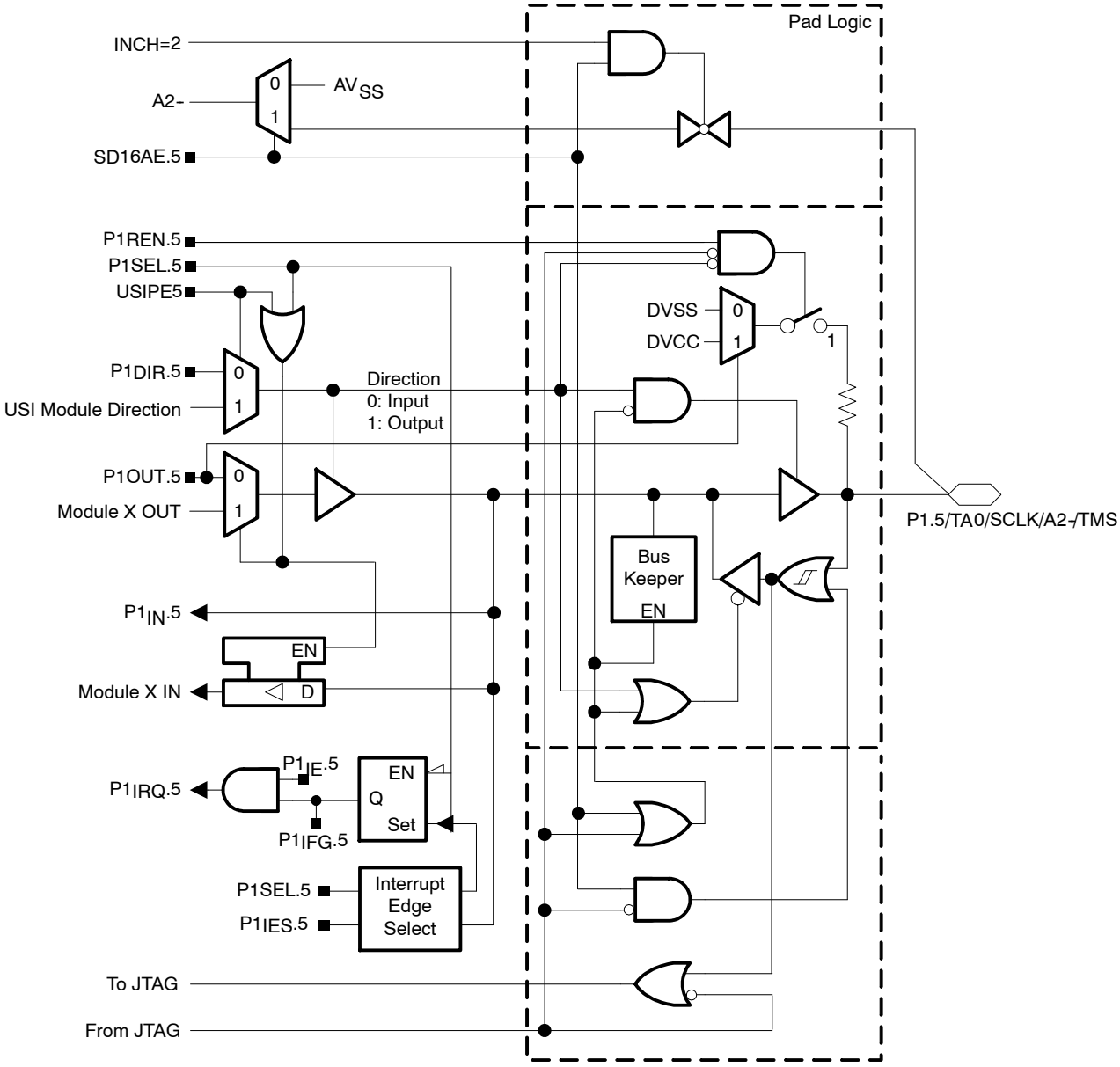
† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the SD16AE.x bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. With SD16AE.x = 0 the negative inputs are connected to VSS if the corresponding input is selected.
5. In JTAG mode the internal pull-up/down resistors are disabled.
6. Function controlled by JTAG

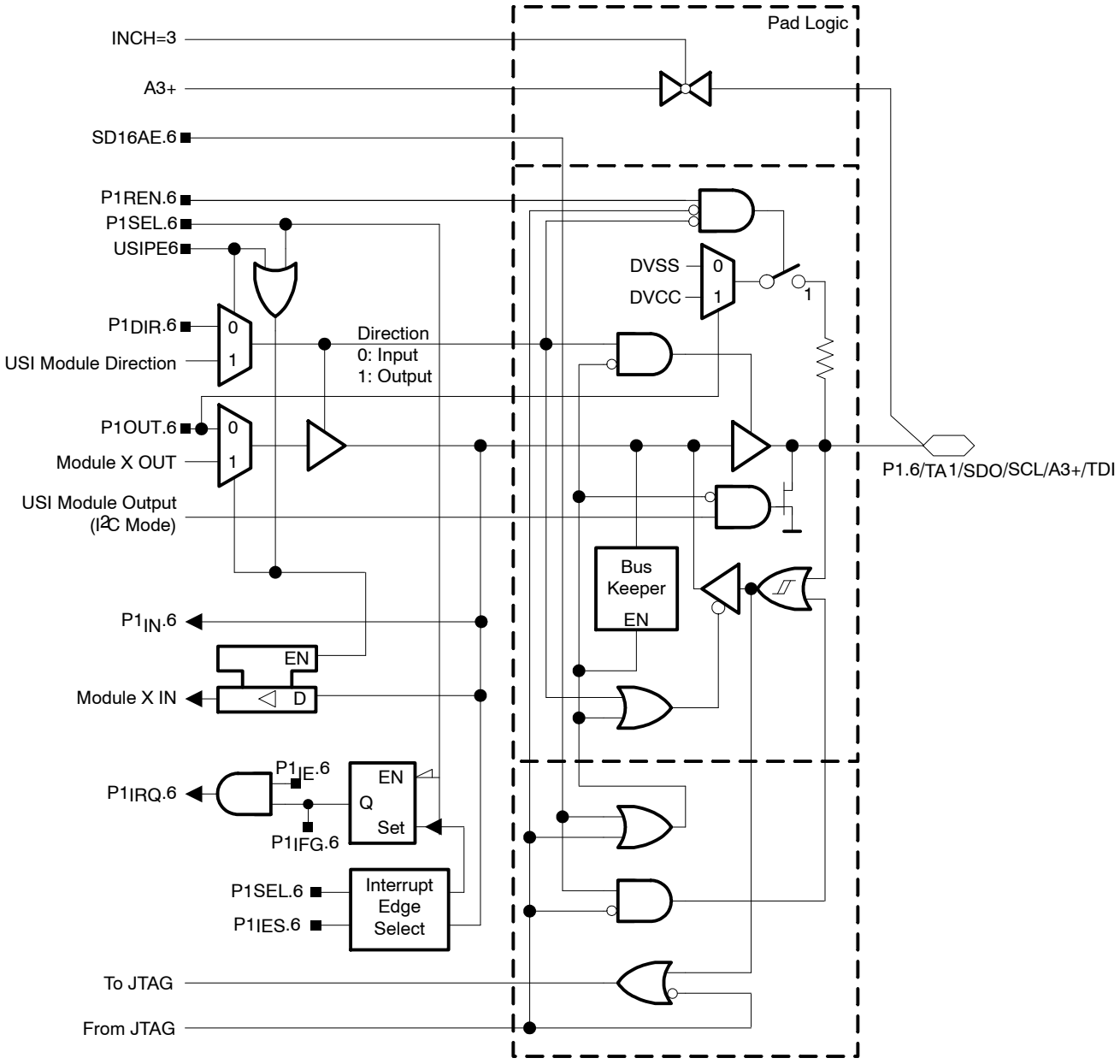
Port P1 (P1.4) pin schematics, MSP430x20x3



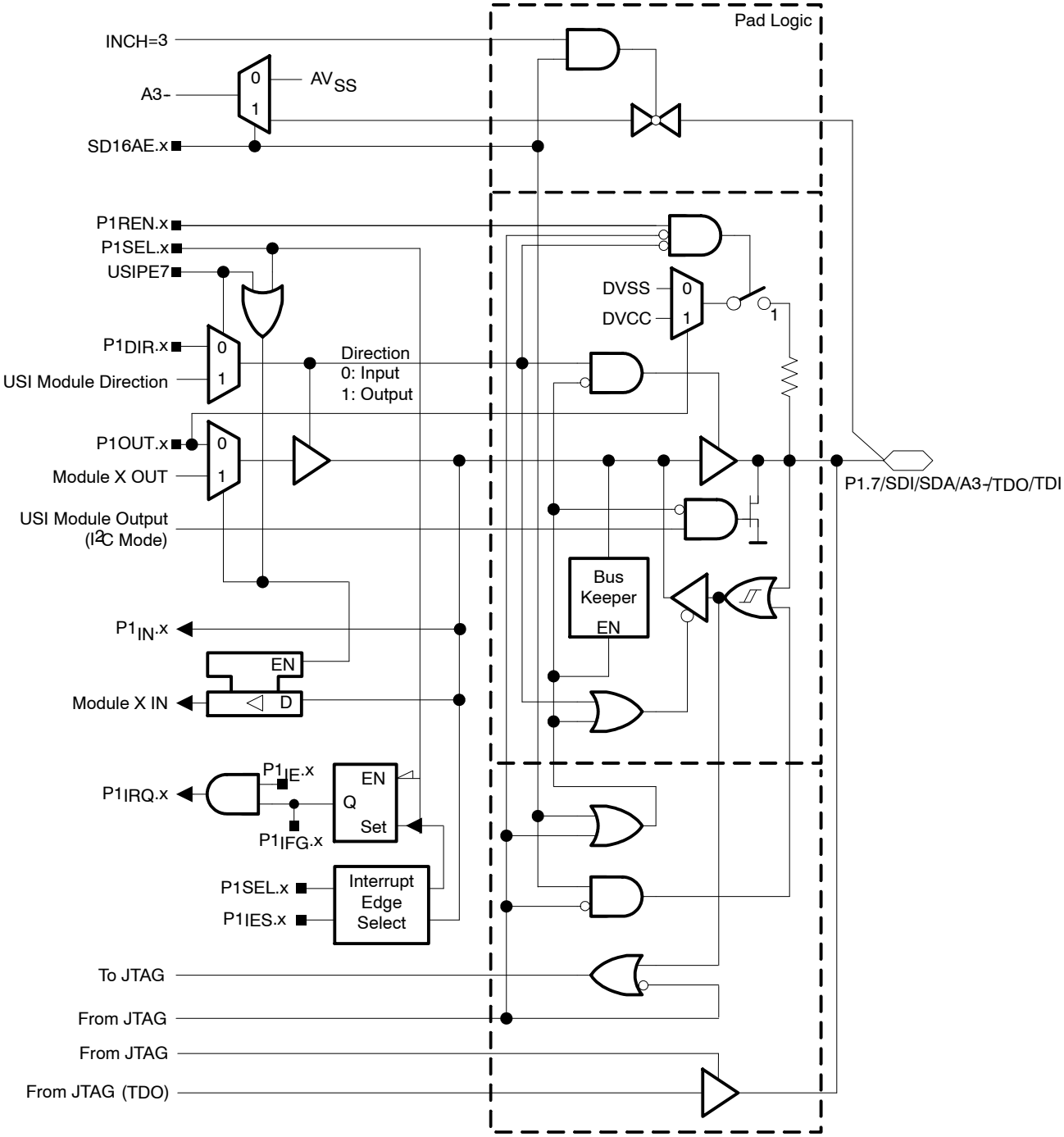
Port P1 (P1.5) pin schematics, MSP430x20x3



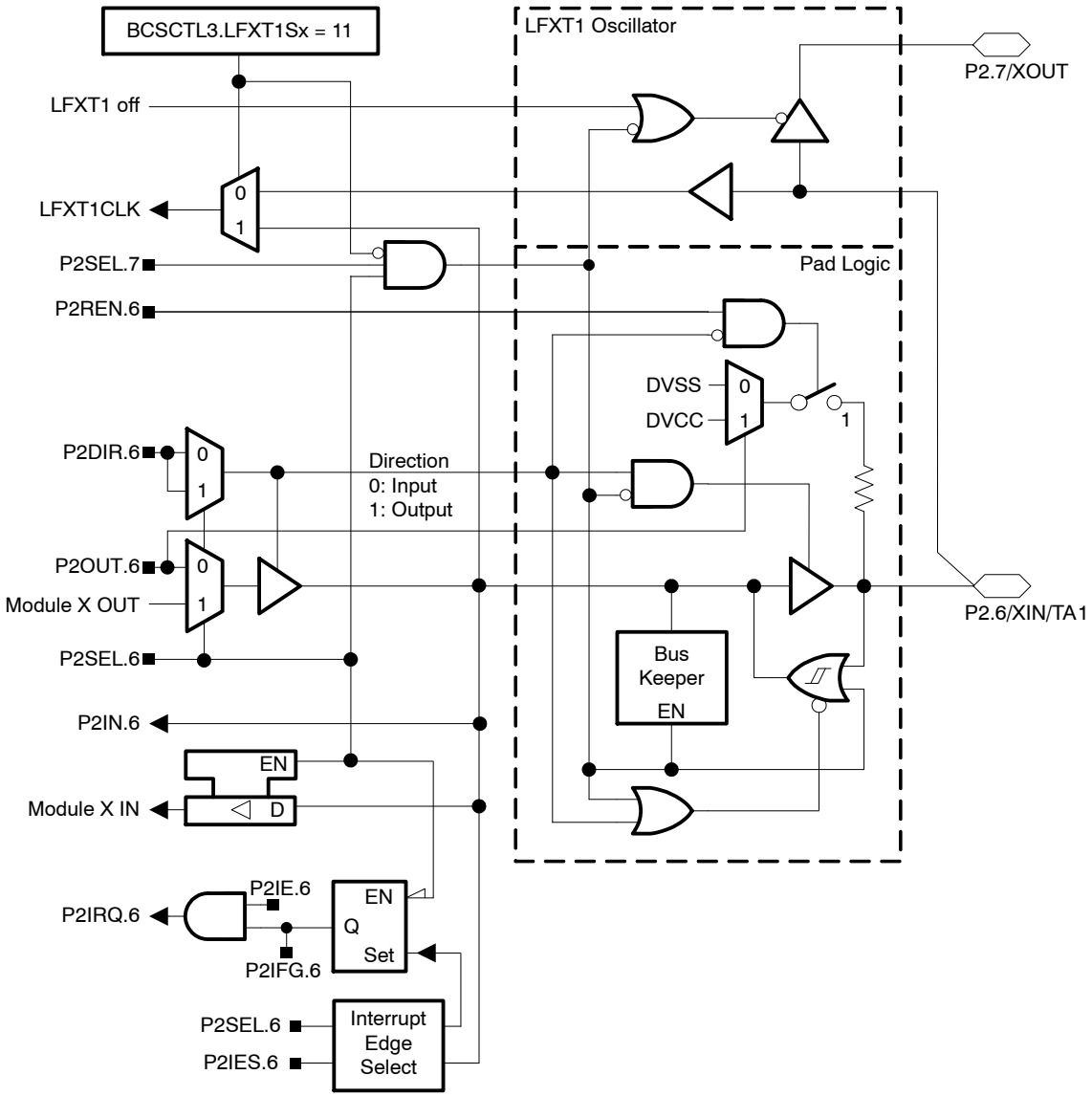
Port P1 (P1.6) pin schematics, MSP430x20x3



Port P1 (P1.7) pin schematics, MSP430x20x3



Port P2 (P2.6) pin schematics, MSP430x20x3



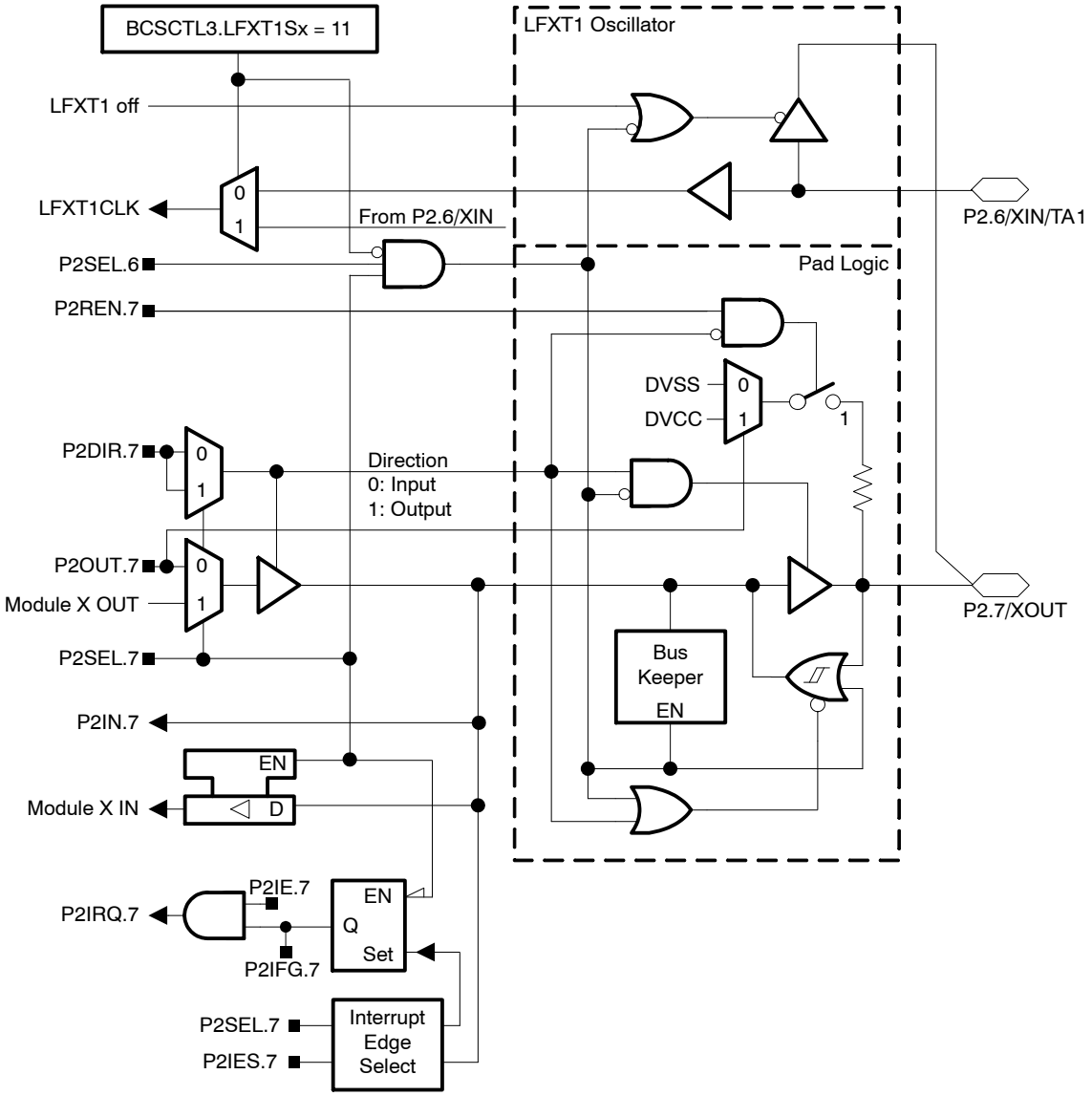
Port P2 (P2.6) pin functions, MSP430x20x3

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.6/XIN/TA1	6	P2.6 Input/Output	0/1	0
		XIN† (see Note 3)	0	1
		Timer_A2.TA1	1	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. XIN is used as digital clock input if the bits LFXT1Sx in register BCSCTL3 are set to 11.

Port P2 (P2.7) pin schematics, MSP430x20x3



Port P2 (P2.7) pin functions, MSP430x20x3

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.7/XOUT	7	P2.7 Input/Output	0/1	0
		DVSS	0	1
		XOUT† (see Note 3)	1	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. If the pin P2.7/XOUT is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

Data Sheet Revision History

Literature Number	Summary
SLAS491	Preliminary PRODUCT PREVIEW data sheet release
SLAS491A	Production data sheet release for MSP430x20x3I. Updated specification and added characterization graphs.
SLAS491B	Production data sheet release for MSP430x20x3T, MSP430x20x1I and MSP430x20x1T. 105°C characterization results added. SD16_A SINAD characterization results for MSP430x20x3RSA package added. Updated SD16_A Power Supply Rejection specification. DCO Calibration Register names: lower case “z” changed to upper case “Z”. $V_{hys(B\_IT-)}$ MAX specification increased from 180mV to 210mV. MIN and MAX percentages for “calibrated DCO frequencies – tolerance over supply voltage VCC” corrected from 2.5% to 3.0% to match the specified frequency ranges.
SLAS491C	Production data sheet release for MSP430x20x2I and MSP430x20x2T.
SLAS491D	Changed f_{ACLK} to 0 Hz in I_{LPM4} test conditions on page 23.
SLAS491E	Changed T_{stg} maximum for programmed devices to 150°C (page 20)
SLAS491F	Added ADC10 data transfer registers to Peripheral File Map (page 18, 19)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
MSP430F2001IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2001IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2001IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2001IRSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2001IRSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2001TN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2001TPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2001TPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2001TRSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2001TRSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2002IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2002IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2002IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2002IRSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2002IRSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2002TN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2002TPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2002TPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
MSP430F2002TRSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2002TRSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2003IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2003IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2003IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2003IRSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2003IRSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2003TN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2003TPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2003TPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2003TRSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2003TRSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2011IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2011IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2011IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2011IRSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2011IRSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2011TN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2011TPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
MSP430F2011TPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2011TRSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2011TRSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2012IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2012IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2012IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2012IRSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2012IRSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2012TN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2012TPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2012TPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2012TRSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2012TRSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2013IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2013IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2013IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2013IRSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2013IRSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2013TN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
MSP430F2013TPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2013TPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430F2013TRSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430F2013TRSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

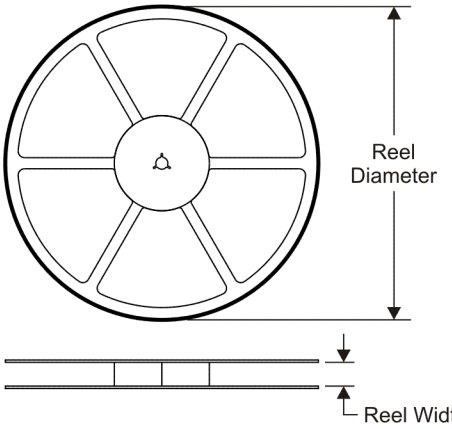
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

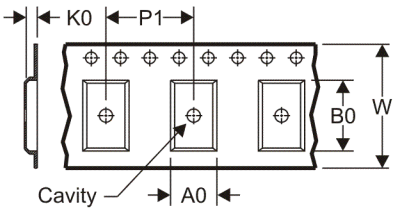
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

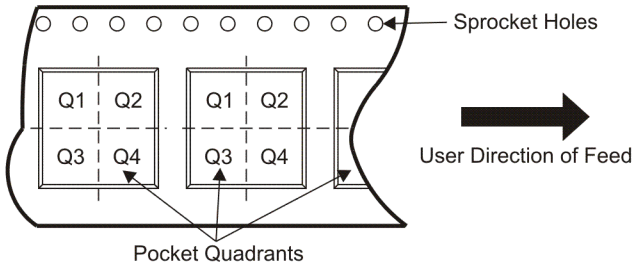


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

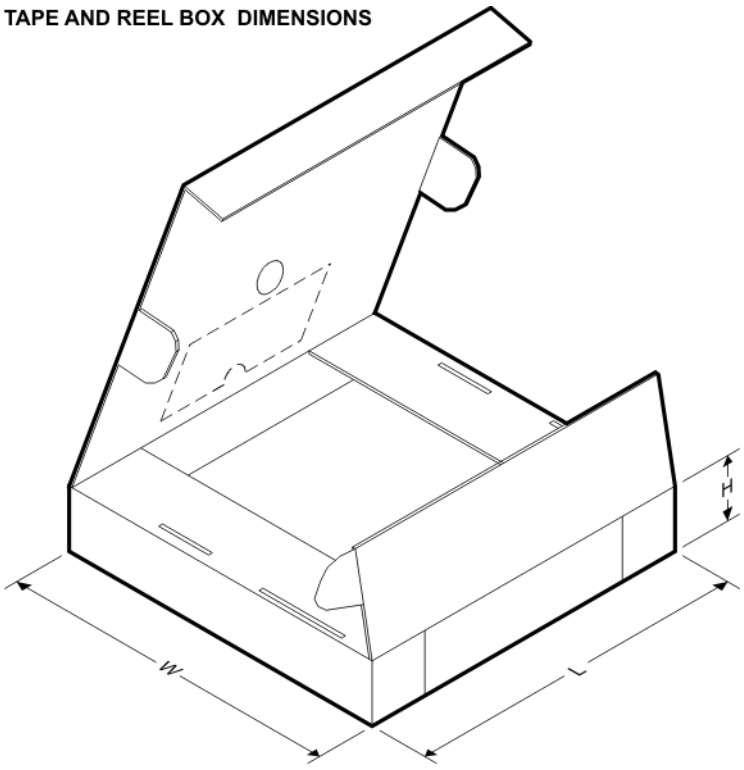


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F2001IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2001IRSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2001IRSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2001TRSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2001TRSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2002IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2002IRSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2002IRSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2002TPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2002TRSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2002TRSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2003IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2003IRSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2003IRSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2003TPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2003TRSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2003TRSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2011IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F2011IRSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2011TPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2011TRSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2011TRSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2012IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2012IRSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2012IRSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2012TPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2012TRSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2012TRSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2013IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2013IRSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2013IRSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2013TPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2013TRSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2013TRSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

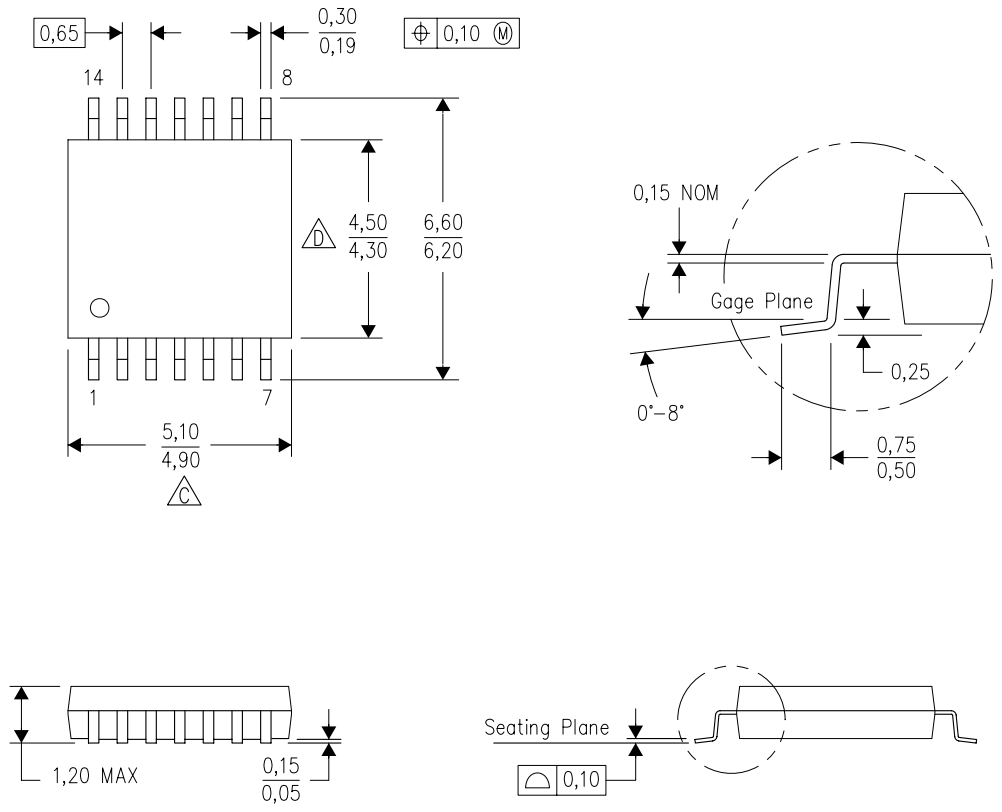


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F2001IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F2001IRSAR	QFN	RSA	16	3000	346.0	346.0	29.0
MSP430F2001IRSAT	QFN	RSA	16	250	190.5	212.7	31.8
MSP430F2001TRSAR	QFN	RSA	16	3000	346.0	346.0	29.0
MSP430F2001TRSAT	QFN	RSA	16	250	190.5	212.7	31.8
MSP430F2002IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
MSP430F2002IRSAR	QFN	RSA	16	3000	346.0	346.0	29.0
MSP430F2002IRSAT	QFN	RSA	16	250	190.5	212.7	31.8
MSP430F2002TPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
MSP430F2002TRSAR	QFN	RSA	16	3000	346.0	346.0	29.0
MSP430F2002TRSAT	QFN	RSA	16	250	190.5	212.7	31.8
MSP430F2003IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
MSP430F2003IRSAR	QFN	RSA	16	3000	346.0	346.0	29.0
MSP430F2003IRSAT	QFN	RSA	16	250	190.5	212.7	31.8
MSP430F2003TPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
MSP430F2003TRSAR	QFN	RSA	16	3000	346.0	346.0	29.0
MSP430F2003TRSAT	QFN	RSA	16	250	190.5	212.7	31.8
MSP430F2011IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
MSP430F2011IRSAR	QFN	RSA	16	3000	346.0	346.0	29.0
MSP430F2011TPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
MSP430F2011TRSAR	QFN	RSA	16	3000	346.0	346.0	29.0
MSP430F2011TRSAT	QFN	RSA	16	250	190.5	212.7	31.8
MSP430F2012IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
MSP430F2012IRSAR	QFN	RSA	16	3000	346.0	346.0	29.0
MSP430F2012IRSAT	QFN	RSA	16	250	190.5	212.7	31.8
MSP430F2012TPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
MSP430F2012TRSAR	QFN	RSA	16	3000	346.0	346.0	29.0
MSP430F2012TRSAT	QFN	RSA	16	250	190.5	212.7	31.8
MSP430F2013IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
MSP430F2013IRSAR	QFN	RSA	16	3000	346.0	346.0	29.0
MSP430F2013IRSAT	QFN	RSA	16	250	190.5	212.7	31.8
MSP430F2013TPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
MSP430F2013TRSAR	QFN	RSA	16	3000	346.0	346.0	29.0
MSP430F2013TRSAT	QFN	RSA	16	250	190.5	212.7	31.8

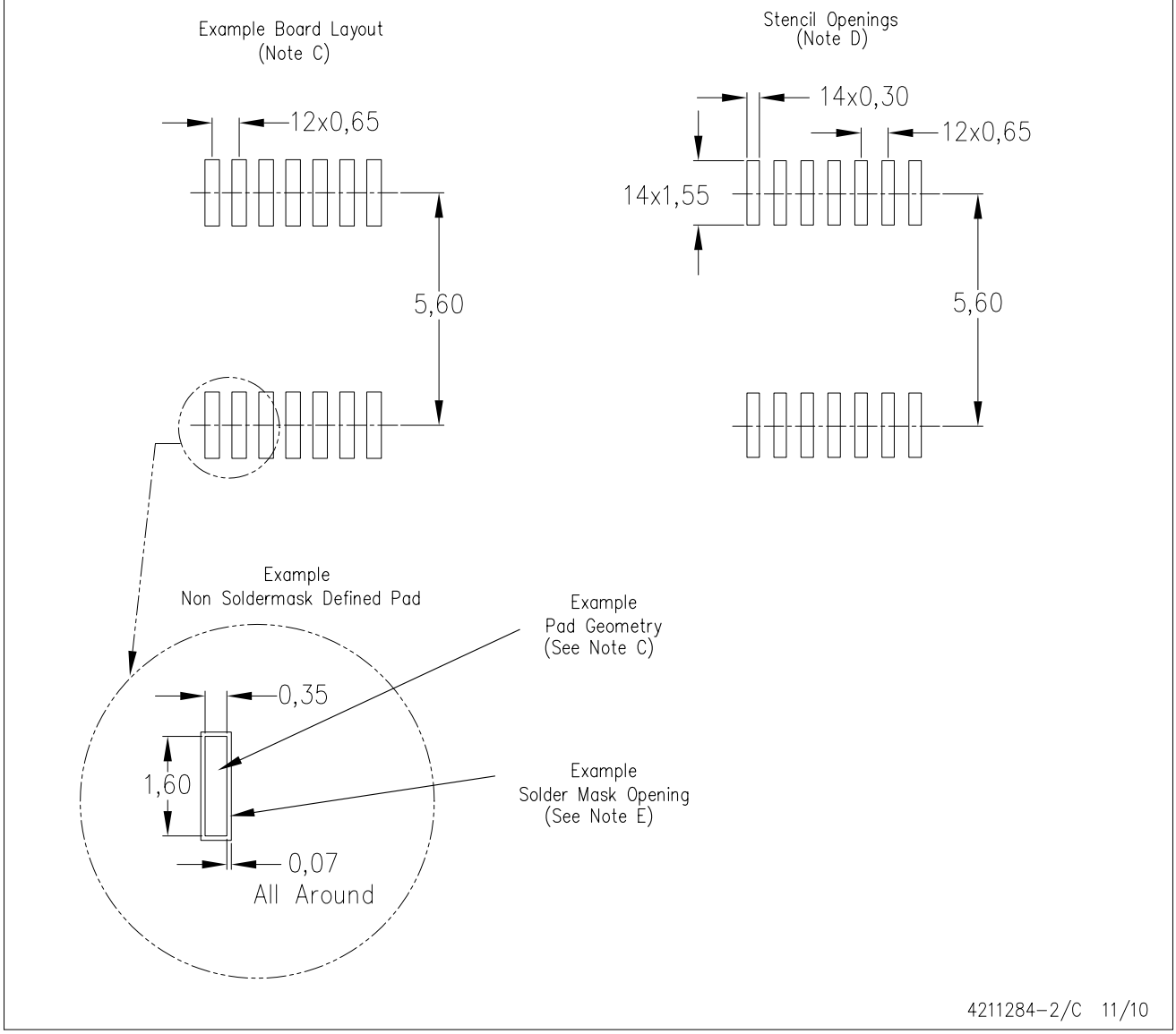
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

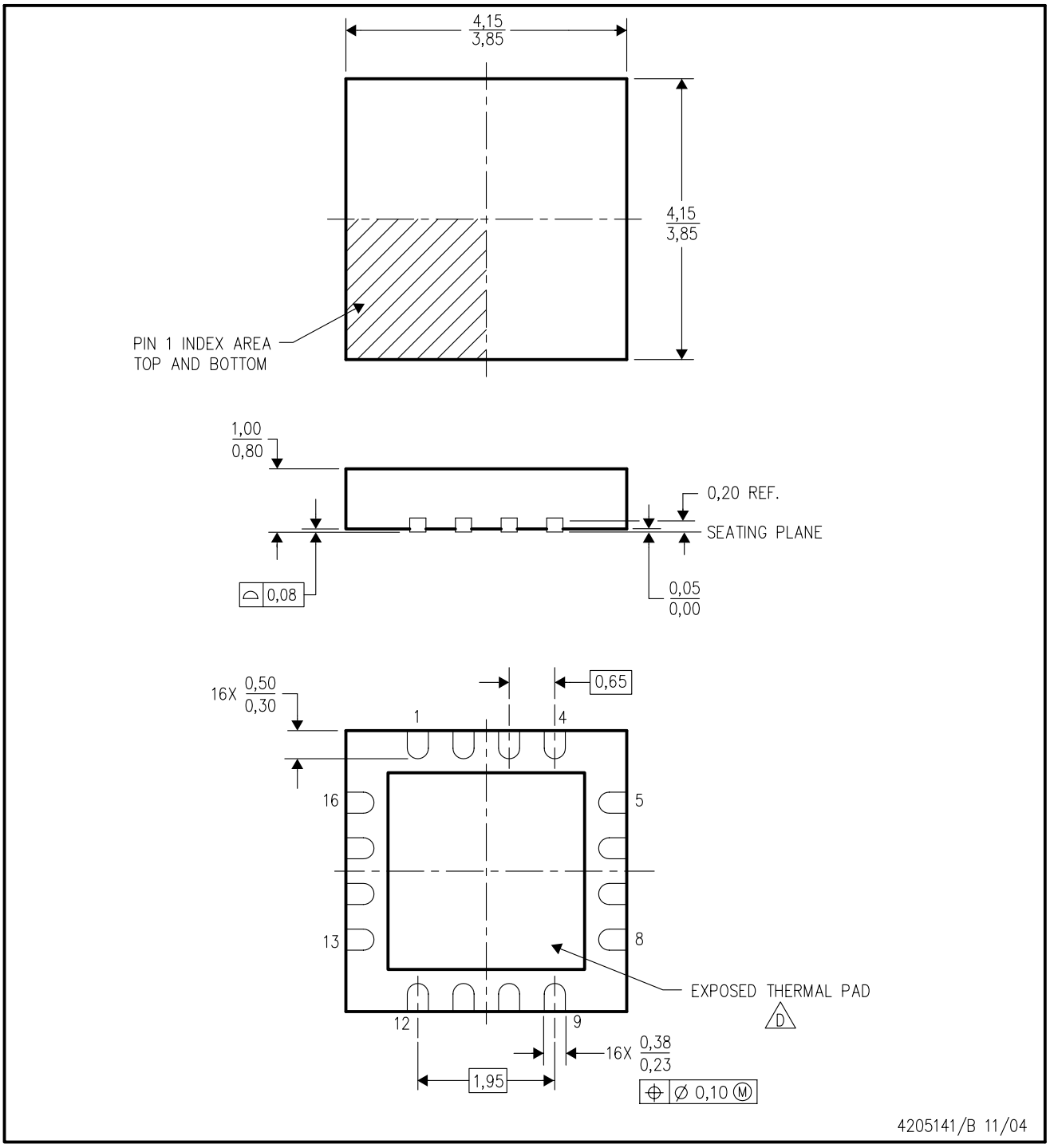
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSA (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

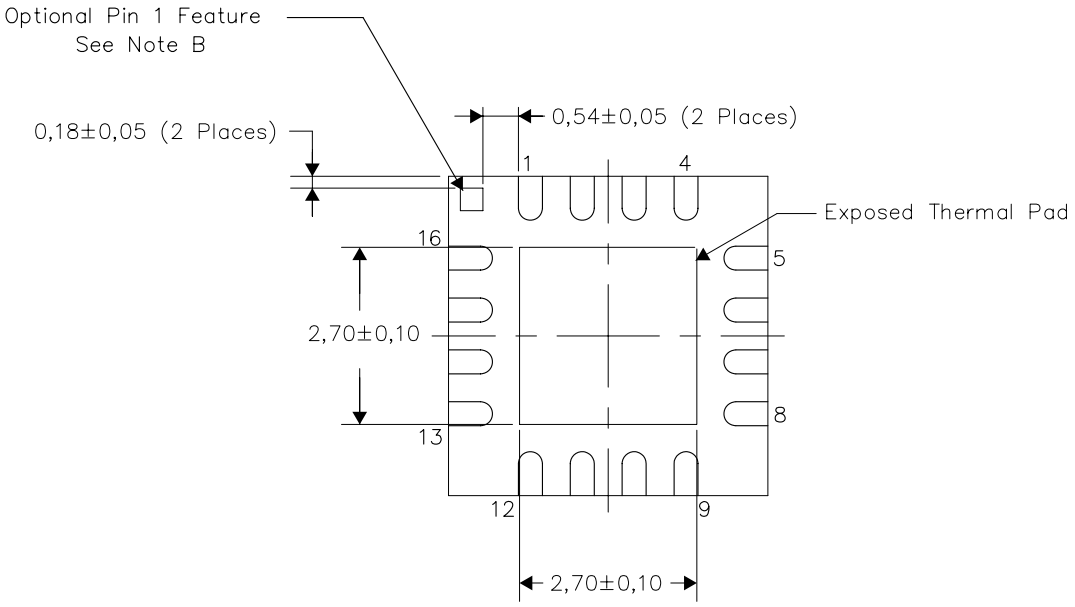
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

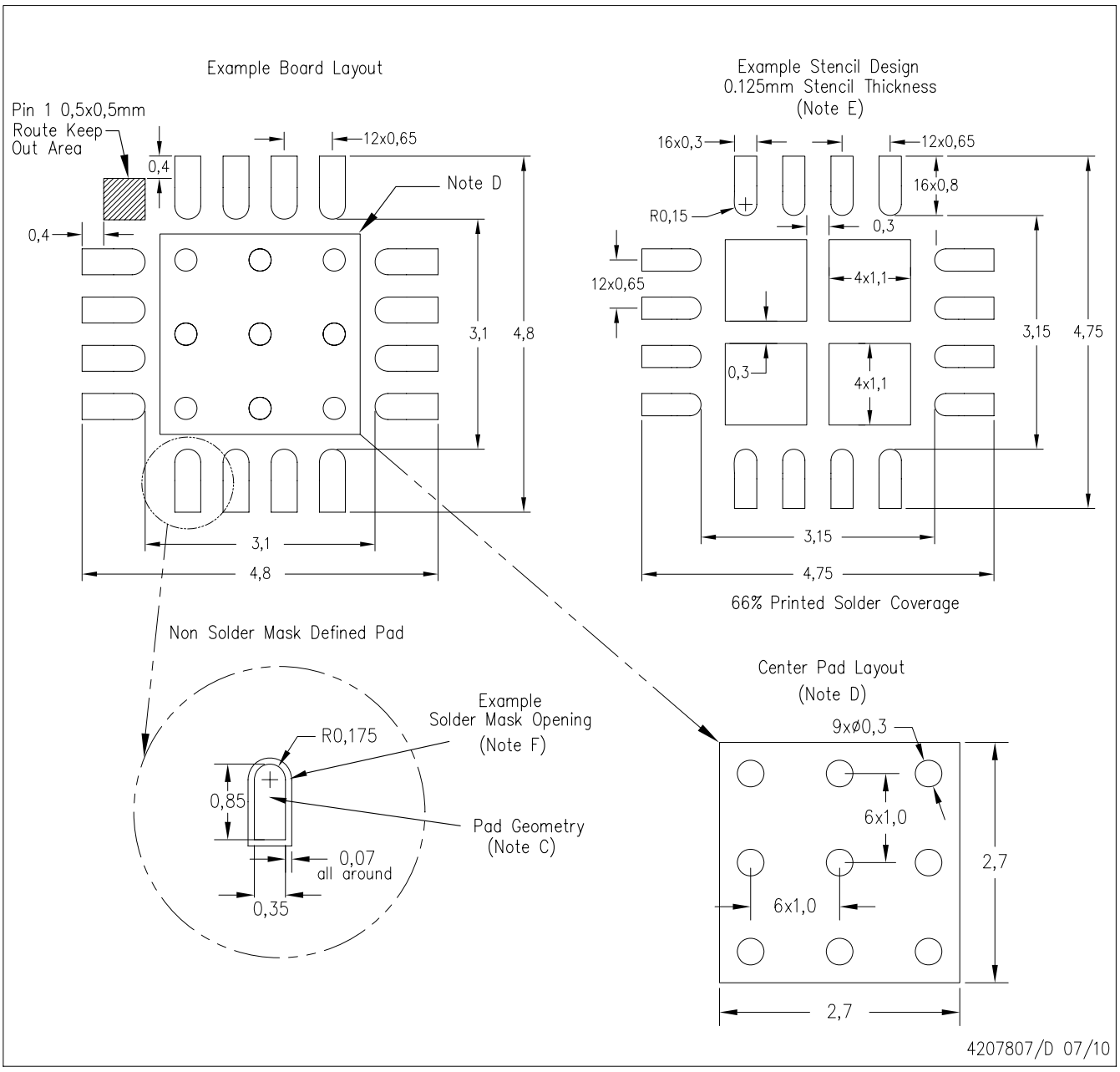
4206364/J 01/11

NOTES:

A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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