Timer 0 -Register ATmega8:

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x39(0x59)	TIMSK							–	TOIE0	72
0x38(0x58)	TIFR							–	TOV0	72
0x33(0x53)	TCCR0	–	–	–	–	–	CS02	CS01	CS00	71
0x32(0x52)	TCNT0	Timer/Counter0 (8 Bits)								72

TIMSK	TOIE0	Timer overflow interrupt enable
TIFR	TOV0	Timer overflow flag
TCCR0	CS02:1	Clock select bits: 0=stop 1=/1 2=/8 3=/64 4=/256 5=/1024 6=T1-Pin falling 7=T1-Pin rising

Timer 0-Register ATmega88

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x6E)	TIMSK0	–	–	–	–	–	OCIE0B	OCIE0A	TOIE0	106
0x28(0x48)	OCR0B	Timer/Counter0 output compare register B								
0x27(0x47)	OCR0A	Timer/Counter0 output compare register A								
0x26(0x46)	TCNT0	Timer/Counter0 (8-bit)								
0x25(0x45)	TCCR0B	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	
0x24(0x44)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	
0x15(0x35)	TIFR0	–	–	–	–	–	OCF0B	OCF0A	TOV0	
0x23(0x43)	GTCCR	TSM	–	–	–	–	–		PSRSYNC	139

TIMSK0	TOIE0	Timer overflow interrupt enable
	OCIE0A/B	Timer output compare A/B match interrupt enable
TCCR0B	CS00:2	Clock select bits: 0=stop 1=/1 2=/8 3=/64 4=/256 5=/1024 6=T1-Pin falling 7=T1-Pin rising
	FOC0A/B	Force output compare A/B
	WGM02	Wave generation mode bit 2
TCCR0A	COM0A/B1:0	Compare match output A/B mode

COM0A/B1:0	non-PWM	fast PWM	phase correct PWM
00	OC0A/B disconnected	OC0A/B disconnected	OC0A/B disconnected
01	Toggle OC0A/B on compare match	WGM02 = 0: OC0A/B disconnected WGM02 = 1: Toggle OC0A/B on compare match	WGM02 = 0: OC0A/B disconnected WGM02 = 1: Toggle OC0A/B on compare match
10	Clear OC0A/B on compare match	Clear OC0A/B on compare match, set OC0A/B at BOTTOM	Clear OC0A/B on compare match when up-counting, Set OC0A/B on compare match when down-counting
11	Set OC0A/B on compare match	Set OC0A/B on compare match, Clear OC0A/B at BOTTOM	Set OC0A/B on compare match when up-counting, Clear OC0A/B on compare match when down-counting

WGM02:0 — Wave generation mode bits 2:0

WGM2:0	Mode	TOP	update of OCRx at	TOV flag set on
000	Normal	0xFF	Immediate	MAX
001	PWM, phase correct	0xFF	TOP	BOTTOM
010	CTC	OCRA	Immediate	MAX
011	Fast PWM	0xFF	BOTTOM	MAX
100	Reserved			
101	PWM, phase correct	OCRA	TOP	BOTTOM
110	Reserved			
111	Fast PWM	OCRA	BOTTOM	TOP

TIFR	TOV0	Timer overflow flag
	OCF0A/B	Timer output compare A/B match flag
GTCCR	TSM	Timer/Counter 1 & 2 synchronization mode
	PSRSYNC	Timer/Counter 1 & 2 Prescaler reset

Timer 1-Register ATmega8:

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x39(0x59)	TIMSK			TICIE1	OCIE1A	OCIE1B	TOIE1	–		100
0x38(0x58)	TIFR			ICF1	OCF1A	OCF1B	TOV1	–		101
0x2F(0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	96
0x2E(0x4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	98
0x2D(0x4D)	TCNT1H	Timer/Counter1 – Counter Register High byte								99
0x2C(0x4C)	TCNT1L	Timer/Counter1 – Counter Register Low byte								99
0x2B(0x4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High byte								99
0x2A(0x4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low byte								99
0x29(0x49)	OCR1BH	Timer/Counter1 – Output Compare Register B High byte								99
0x28(0x48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low byte								99
0x27(0x47)	ICR1H	Timer/Counter1 – Input Capture Register High byte								100
0x26(0x46)	ICR1L	Timer/Counter1 – Input Capture Register Low byte								100

TIMSK	TOIE1	Timer overflow interrupt enable			
	OCIE1A/B	Timer/Counter1 output compare A/B match interrupt enable			
	TICIE1	Timer/Counter1 Input Capture Interrupt enable			
TIFR	TOV1	Timer/Counte1r overflow flag			
	OCF1A/B	Timer/Counter1 output compare A/B match flag			
	ICF1	Timer/Counter1 Input Capture Flag			
TCCR1A	COM1A/B1:0	Compare match output A/B mode			
			non-PWM	**fast PWM**	**phase correct PWM**
		00	OC1A/B disconnected	OC1A/B disconnected	OC1A/B disconnected
		01	Toggle OC1A/B on compare match	WGM13:0 != 15: OC1A/B disconnected WGM13:0 == 15: Toggle OC1A on compare match, OC1B disconnected	WGM13:0 != 9 or 14: OC0A/B disconnected WGM13:0 == 9 or 14: Toggle OC1A on compare match, OC1B disconnected
		10	Clear OC1A/B on compare match	Clear OC1A/B on compare match, set OC1A/B at BOTTOM	Clear OC1A/B on compare match when up-counting, Set OC1A/B on compare match when down-counting
		11	Set OC1A/B on compare match	Set OC1A/B on compare match, Clear OC1A/B at BOTTOM	Set OC1A/B on compare match when up-counting, Clear OC1A/B on compare match when down-counting
	WGM11:0	Wave generation mode bits 1:0			

WGM3:0	**Mode**	**TOP**	**update of OCR1x at**	**TOV flag set on**
0 0000	Normal	0xFFFF	Immediate	MAX
1 0001	PWM, phase correct 8 bit	0x00FF	TOP	BOTTOM
2 0010	PWM, phase correct 9 bit	0x01FF	TOP	BOTTOM
3 0011	PWM, phase correct 10 bit	0x03FF	TOP	BOTTOM
4 0100	CTC	OCRA	Immediate	MAX
5 0101	Fast PWM 8 bit	0x00FF	BOTTOM	TOP
6 0110	Fast PWM 9 bit	0x01FF	BOTTOM	TOP
7 0111	Fast PWM 10 bit	0x03FF	BOTTOM	TOP
8 1000	PWM, Phase an Frequency Correct	ICR1	BOTTOM	BOTTOM
9 1001	PWM, Phase an Frequency Correct	OCR1A	BOTTOM	BOTTOM
10 1010	PWM, phase correct	ICR1	TOP	BOTTOM
11 1011	PWM, phase correct	OCR1A	BOTTOM	BOTTOM
12 1100	CTC	ICR1	Immediate	MAX
13 1101	reserved			
14 1110	Fast PWM	ICR1	BOTTOM	TOP
15 1111	Fast PWM	OCR1A	BOTTOM	TOP

	FOC1A/B	Force output compare A/B
TCCR1B	ICNC1	Input Capture Noise Canceler
	ICES1	Input Capture Edge Select: 0=falling 1=rising
	WGM13:2	Wave generation mode bits 3:2
	CS12:0	Clock select bits: 0=stop 1=/1 2=/8 3=/64 4=/256 5=/1024 6=T1-Pin falling 7=T1-Pin rising

Timer 1-Register ATmega88

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x8B)	OCR1BH	Timer/Counter1 - output compare register B high byte								134
(0x8A)	OCR1BL	Timer/Counter1 - output compare register B low byte								134
(0x89)	OCR1AH	Timer/Counter1 - output compare register A high byte								134
(0x88)	OCR1AL	Timer/Counter1 - output compare register A low byte								134
(0x87)	ICR1H	Timer/Counter1 - input capture register high byte								135
(0x86)	ICR1L	Timer/Counter1 - input capture register low byte								135
(0x85)	TCNT1H	Timer/Counter1 - counter register high byte								134
(0x84)	TCNT1L	Timer/Counter1 - counter register low byte								134
(0x82)	TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–	133
(0x81)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	132
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	–	–	WGM11	WGM10	130
(0x6F)	TIMSK1	–	–	ICIE1	–	–	OCIE1B	OCIE1A	TOIE1	135
0x23(0x43)	GTCCR	TSM	–	–	–	–	–		PSRSYNC	139
0x16(0x36)	TIFR1	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1	136

TCCR1C	FOC1A/B	Force output compare A/B				
TCCR1B	ICNC1	Input Capture Noise Canceler				
	ICES1	Input Capture Edge Select: 0=falling 1=rising				
	WGM13:2	Wave generation mode bits 3:2				
	CS12:0	Clock select bits: 0=stop 1=/1 2=/8 3=/64 4=/256 5=/1024 6=T1-Pin falling 7=T1-Pin rising				
TCCR1A	COM1A/B1:0	Compare match output A/B mode				
			non-PWM	fast PWM	phase correct (and frequency correct) PWM	
		00	OC1A/B disconnected	OC1A/B disconnected	OC1A/B disconnected	
		01	Toggle OC1A/B on compare match	WGM13:0 != 14 or 15: OC1A/B disconnected WGM13:0 == 14 or 15: Toggle OC1A on compare match, OC1B disconnected	WGM13:0 != 9 or 11: OC0A/B disconnected WGM13:0 == 9 or 11: Toggle OC1A on compare match, OC1B disconnected	
		10	Clear OC1A/B on compare match	Clear OC1A/B on compare match, set OC1A/B at BOTTOM	Clear OC1A/B on compare match when up-counting, Set OC0A/B on compare match when down-counting	
		11	Set OC1A/B on compare match	Set OC1A/B on compare match, Clear OC1A/B at BOTTOM	Set OC0A/B on compare match when up-counting, Clear OC0A/B on compare match when down-counting	
	WGM11:0	Wave generation mode bits 1:0				
		WGM3:0	Mode	TOP	update of OCR1x at	TOV flag set on
		0 0000	Normal	0xFFFF	Immediate	MAX
		1 0001	PWM, phase correct 8 bit	0x00FF	TOP	BOTTOM
		2 0010	PWM, phase correct 9 bit	0x01FF	TOP	BOTTOM
		3 0011	PWM, phase correct 10 bit	0x03FF	TOP	BOTTOM
		4 0100	CTC	OCR1A	Immediate	MAX
		5 0101	Fast PWM 8 bit	0x00FF	BOTTOM	TOP
		6 0110	Fast PWM 9 bit	0x01FF	BOTTOM	TOP
		7 0111	Fast PWM 10 bit	0x03FF	BOTTOM	TOP
		8 1000	PWM, Phase an Frequency Correct	ICR1	BOTTOM	BOTTOM
		9 1001	PWM, Phase an Frequency Correct	OCR1A	BOTTOM	BOTTOM
		10 1010	PWM, phase correct	ICR1	TOP	BOTTOM
		11 1011	PWM, phase correct	OCR1A	TOP	BOTTOM
		12 1100	CTC	ICR1	Immediate	MAX
		13 1101	reserved			
		14 1110	Fast PWM	ICR1	BOTTOM	TOP
		15 1111	Fast PWM	OCR1A	BOTTOM	TOP
TIMSK1	TOIE1	Timer/Counter overflow interrupt enable				
	OCIE1A/B	Timer/Counter output compare A/B match interrupt enable				
	ICIE1	Timer/Counter Input Capture Interrupt enable				
GTCCR	TSM	Timer/Counter 1 & 2 synchronization mode				
	PSRSYNC	Timer/Counter 1 & 2 Prescaler reset				
TIFR1	TOV1	Timer overflow flag				
	OCF1A/B	Timer output compare A/B match flag				
	ICF1	Timer/Counter1 Input Capture Flag				

Timer 2-Register ATmega8:

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x39(0x59)	TIMSK	OCIE2	TOIE2					–		72, 102, 122
0x38(0x58)	TIFR	OCF2	TOV2					–		73, 102, 122
0x25(0x45)	TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	117
0x24(0x44)	TCNT2	Timer/Counter2 (8 Bits)								119
0x23(0x43)	OCR2	Timer/Counter2 Output Compare Register								119
0x22(0x42)	ASSR	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	119

TIMSK	TOIE2	Timer/Counter 2 overflow interrupt enable				
	OCIE2	Timer/Counter2 output compare match interrupt enable				
TIFR	TOV2	Timer/Counter2 overflow flag				
	OCF2	Timer/Counter2 output compare match flag				
TCCR2	COM21:0	Compare match output mode				
		COM21:0	**non-PWM**	**fast PWM**	**phase correct PWM**	
		00	OC2A disconnected	OC2A disconnected	OC1A/B disconnected	
		01	Toggle OC2A on compare match	reserved	reserved	
		10	Clear OC2A on compare match	Clear OC2 on compare match, set OC2 at BOTTOM	Clear OC2 on compare match when up-counting, Set OC2 on compare match when down-counting	
		11	Set OC2A on compare match	Set OC2 on compare match, Clear OC2 at BOTTOM	Set OC2 on compare match when up-counting, Clear OC2 on compare match when down-counting	
	WGM21:0	Wave generation mode bits 1:0				
		WGM2	Mode	TOP	update of OCRx at	TOV flag set on
		00	Normal	0xFF	Immediate	MAX
		01	PWM, phase correct	0xFF	TOP	BOTTOM
		10	CTC	OCRA	Immediate	MAX
		11	Fast PWM	0xFF	BOTTOM	MAX
	FOC2	Force output compare				
	CS22:0	Clock select bits: 0=stop 1=/1 2=/8 3=/64 4=/256 5=/1024 6=T1-Pin falling 7=T1-Pin rising				
ASSR	AS2	Asynchronous Timer/Counter 2				
	TCN2UB	Timer/Counter 2 Update Busy				
	OCR2UB	Output Compare Resister 2 Update Busy				
	TCR2UB	Timer/Counter Control Register Update Busy				

Timer 2-Register ATmega88

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xB6)	ASSR	–	EXCLK	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB	159
(0xB4)	OCR2B	Timer/Counter2 output compare register B								158
(0xB3)	OCR2A	Timer/Counter2 output compare register A								157
(0xB2)	TCNT2	Timer/Counter2 (8-bit)								157
(0xB1)	TCCR2B	FOC2A	FOC2B	–	–	WGM22	CS22	CS21	CS20	156
(0xB0)	TCCR2A	COM2A1	COM2A0	COM2B1	COM2B0	–	–	WGM21	WGM20	153
(0x70)	TIMSK2	–	–	–	–	–	OCIE2B	OCIE2A	TOIE2	158
0x23(0x43)	GTCCR	TSM	–	–	–	–	–	PSRASY		160
0x17(0x37)	TIFR2	–	–	–	–	–	OCF2B	OCF2A	TOV2	158

TIMSK2	TOIE2	Timer/Counter 2 overflow interrupt enable				
	OCIE2A/B	Timer/Counter2 output compare match interrupt enable				
TIFR2	TOV2	Timer/Counter2 overflow flag				
	OCF2	Timer/Counter2 output compare match flag				
TCCR2B	FOC2A/B	Force Output Compare A/B				
	WGM22	Wave generation mode bit 2				
	CS22:1	Clock select bits: 0=stop 1=/1 2=/8 3=/64 4=/256 5=/1024 6=T1-Pin falling 7=T1-Pin rising				
TCCR2A	COM2A/B1:0	Compare match output mode				
			non-PWM	fast PWM	phase correct PWM	
		00	OC2A disconnected	OC2A disconnected	OC1A/B disconnected	
		01	Toggle OC2A on compare match	WGM22 == 0: OC2A/B disconnected WGM22 == 1: Toggle OC2A on compare match	WGM22 == 0: OC2A disconnected WGM22 == 1: Toggle OC2A on compare match, OC1B disconnected	
		10	Clear OC2A on compare match	Clear OC2A on compare match, set OC2A at BOTTOM	Clear OC2A on compare match when up-counting, Set OC2A on compare match when down-counting	
		11	Set OC2A on compare match	Set OC2A on compare match, Clear OC2A at BOTTOM	Set OC2A on compare match when up-counting, Clear OC2A on compare match when down-counting	
	WGM21:0	Wave generation mode bits 1:0				
		WGM2:0	Mode	TOP	update of OCRx at	TOV flag set on
		000	Normal	0xFF	Immediate	MAX
		001	PWM, phase correct	0xFF	TOP	BOTTOM
		010	CTC	OCRA	Immediate	MAX
		011	Fast PWM	0xFF	BOTTOM	MAX
		100	Reserved			
		101	PWM, phase correct	OCRA	TOP	BOTTOM
		110	Reserved			
		111	Fast PWM	OCRA	BOTTOM	TOP
ASSR	EXCLK	Enable external clock input				
	AS2	Asynchronous Timer/Counter 2				
	TCN2UB	Timer/Counter 2 Update Busy				
	OCR2A/BUB	Output Compare Resister 2 Update Busy				
	TCR2A/BUB	Timer/Counter Control Register Update Busy				