

Lattice Diamond Tutorial

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Type Conventions Used in This Document

Convention	Meaning or Use
Bold	Items in the user interface that you select or click. Text that you type into the user interface.
<italic></italic>	Variables in commands, code syntax, and path names.
Ctrl+L	Press the two keys at the same time.
Courier	Code examples. Messages, reports, and prompts from the software.
••••	Omitted material in a line of code.
•	Omitted lines in code and report examples.
[]	Optional items in syntax descriptions. In bus specifications, the brackets are required.
()	Grouped items in syntax descriptions.
{ }	Repeatable items in syntax descriptions.
	A choice between items in syntax descriptions.



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Lattice Diamond Tutorial

The next generation design tool for FPGA design, Lattice Diamond, was designed to address the needs of high-density FPGA designers.

This tutorial leads you through all the basic steps of designing and implementing a mixed VHDL, Verilog, and Edif design targeted to the Lattice ECP2 device family. It shows you how to use several processes, tools, and reports from the Lattice Diamond software to import sources, run design analysis, view design hierarchy, and inspect strategy settings. The tutorial then proceeds to step through the processes of adding and editing a strategy, specifying the synthesis requirements, examining the device resources, setting timing and location assignments, and editing preferences to configure the filter to implement the design to the target device.

Learning Objectives

When you have completed this tutorial, you should be able to do the following:

- Set up a mixed VHDL, Verilog, and EDIF project
- View and Analyze the design
- Inspect Strategy Settings
- Examine Design Resources
- Set Timing and Location Assignments
- Place and Route
- Create an Implementation
- Set an Active Implementation
- Compare Multiple Place and Route Runs
- Examine Post Place and Route Results

Time to Complete This Tutorial

The time to complete this tutorial is about 60 minutes.

System Requirements

The following software is required to complete the tutorial:

• Lattice Diamond software

Accessing Online Help

You can find online help information on any tool included in the tutorial at any time by choosing **Help > Lattice Diamond Help**.

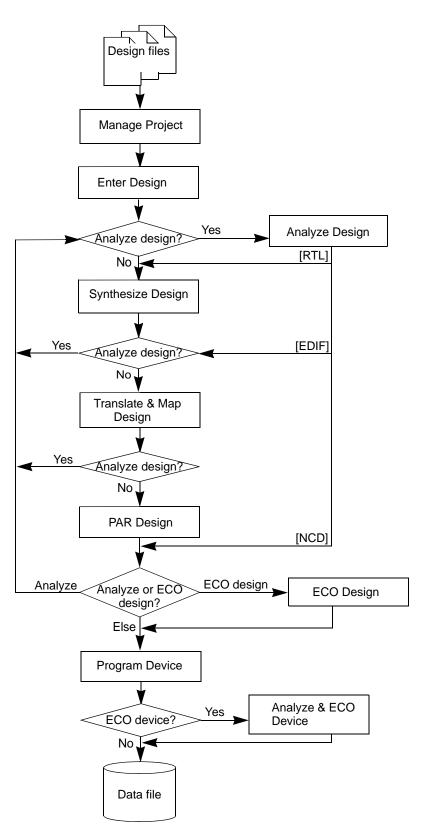
About the Tutorial Design

The design in this tutorial consists of a Verilog HDL module, two VHDL module and one EDIF module. The design that you create is targeted to Lattice ECP2 device families.

About the Tutorial Data Flow

The following figure illustrates the tutorial data flow through the system. You may find it helpful to refer to this diagram as you move through the tutorial tasks.

Tutorial Data Flow

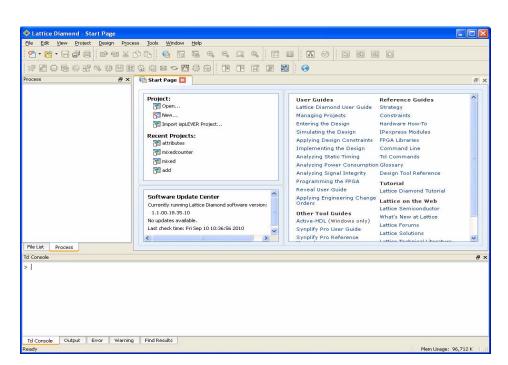


Task 1: Create a New Project

Projects are used to manage input files, preferences, and optimization options related to an FPGA implementation. While there are a number of tasks you can perform independent of a project, most designs start with creating a new project.

To create a new project:

 On Windows, select the Lattice Diamond icon or Start > Programs > Lattice Diamond 1.4 > Lattice Diamond.



The Lattice Diamond Design Environment appears.

The initial layout provides a Start Page which provides a list of common Project actions like **Open...** to open a pre-existing project and **New....** to run the New Project Wizard. Hyperlinks in the right pane of the Start Page provide access to user guides, reference material, and online resources available from www.latticesemi.com.

Note

Several design entry and analysis features of Lattice Diamond are available without a source file as part of the project, for example, you may wish to define and generate an IP core or a microprocessor platform using the Diamond interface and use the result later in one or more projects. Also the power analysis features in Diamond do not require source files to perform estimation.

2. From the Start Page, click **Project > New**, or from the Diamond main window choose **File > New > Project**. You can also click the **New** icon

from the toolbar and then choose Project $\stackrel{\text{Ke}}{=}$.

The New Project overview dialog box appears.

- 3. Click Next. The New Project dialog appears.
- 4. Specify Project name: mixedcounter

Note

File names for Diamond projects and project source files must start with a letter (A-Z, a-z) and must contain only alphanumeric characters (A-Z, a-z, 0-9) and underscores (_).

 Click Browse... to specify a directory on your local PC other than the Diamond installation directory, for example, <drive:\my_diamond_tutorial>.

Note

You will have to store your tutorial files in a directory other than your Lattice Diamond installation directory. You do not have the write permission to the Diamond installation directory.

6. Enter an implementation name. For this tutorial, enter verilog_vhdl_edif.

Implementations are comprised of source and constraint files. You may create or add multiple Implementations per project when you want to compare multiple place and route runs.

By default, when you specify the project name, the implementation name is simultaneously specified the same. For this tutorial, change the implementation name to **verilog_vhdl_edif**. The directory to store the implementation will be automatically displayed in the Location area.

We will talk about creating a new implementation later in this tutorial.

roject:			
i ojecti			
Name: mixed	counter		
Location: F:/my	_diamond_tutorial	~]	B <u>r</u> owse
	_vhdl_edif	vbdl edif	
Locagion. [P./my	_alamona_adonal/veritog_	ma_can	

- 7. Click **Next >**. The Add Source dialog appears.
- 8. Click Add Source... The Import File dialog appears.

- 9. Select the folder where the source files are located
 - <drive:\diamond_install_directory\version#\examples\mixedcounter\sourc e>. Choose count8.edn, topcount.v, typepackge.vhd, and count16.vhd in the directory and click **Open**. The Add Source step of the Wizard appear with all the selected source added.
- 10. Enable **Copy source to implementation directory** and click **Next**. The Select Device dialog appears.
- 11. Select the following device options:

Family: LatticeECP2

Device: LFE2-35E

Performance Grade: 5

Package type: FPBGA672

Click Next >

The **Project Information** dialog appears. The project information including project name, location, implementation name, device, etc. are listed.

12. Click Finish.

The File List view is populated with the Process view and the Reports view.

Note

- If you have run Design > Auto Generate Hierarchy and Design > Auto Run BKM Check in a Lattice Diamond session before starting this tutorial, you will also see the Module Library view, Dictionary view, Hierarchy view displayed beside the Process view. And the Design view of the HDL Diagram will be opened to the right of the Reports view.
- The File List view, Process view, Module Library view, Dictionary view, and Hierarchy view are dockable. You can drag and drop them anywhere in the Diamond main window or even outside the main window.

The File List view displays the components of the project.

Project name:	mixedcounter
Target device:	LFE2-35E-5F672C
Strategies:	Strategy1
Design Implementation:	verilog_vhdl_edif

Note

You can also see Area, I/O Assistant, Quick, Timing listed in the Strategies folder in the File List view. These are predefined strategies supplied by Lattice Semiconductor. They are designed to solve particular types of design. For details of these predefined strategies, refer to the online Help.

🚸 Lattice Diamond - Reports						
Eile Edit View Project Design Proces	s <u>T</u> ools <u>W</u> indow <u>H</u> elp					
9 · 6 · 8 # 6 • 6 • 8	B & B & B & C (3, 0, 9, 12 10 1	. 🛛 i d d i			
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File List 🗗 🗶	👔 Start Page 🔝 🔃 🛄 Rep	orts 🔯			a ×	
	verilogo_vhdl_edif				₽×	
LFE2-35E-5F672C Strategies	Design Summary	N.A.			A	
- Area	Project		mixedcounter project summary			
I/O Assistant	Project Summary Process Reports	Module Name:	mixedcounter	Synthesis:	SynplifyPro	
Timing Strategy1	🛅 Synplify Pro 🛅 Map	Implementation Name:	verilogo_vhdl_edif	Strategy Name:	Strategyl	
Werilogo_vhdl_edif Input Files	D Place & Route	Last Process:		State:		
verilogo_vhdl_edif/source/	Bitstream	Target Device:	LFE2-35E-5F672C	Device Family:	LatticeECP2	
Werilogo_vhdl_edif/sou	🖨 🗾 Analysis Reports	Device Type:	LFE2-35E	Package Type:	FPBGA672	
Werilogo_vhdl_edif/source/i	Place & Route Tra I/O Timing Analysis Tool Reports Generate Hierarchy Run BKM Check PIO DRC	Performance grade:	5	Operating conditions:	COM	
LPF Constraint Files Mixedcounter.lpf Debug Files		Logic preference file:	mixedcounter.lpf			
Cript Files		Physical Preference file:	verilogo_vhdl_edif/mixedcounter_verilogo_vhdl_edif.prf			
- 🗁 Programming Files		Product Version:	1.4.66	Updated:	2011/10/25 16:12:47	
		Implementation Location:	C:/lscc/diamond/l.«	4/examples/tutoria	l/verilogo_vhdl_edif	
File Process Modul Dicti.1		Project File:	C:/lscc/diamond/l.	4/examples/tutoria	l/mixedcounter.ldf	
Output					₽×	
Finished drawing Design View. Starting: "prj_project save"						
Tcl Console Output Error Warning Ready	Find Results				Mem Usage: 256,260 K	

The imported VHDL, Verilog, and EDIF files appear in the Input Files folder in the File List view. The File List organizes project files by categories: Strategies, Implementation including Input Files, Constraint Files, Debug Files, Script Files, and Analysis Files. You may adjust file order by dragging/dropping of the filenames in the list. Properties of each file are accessed by highlighting a file, clicking the right mouse button, and selecting Properties from the pop up menu.

The Process view lists all the processes available, such as synthesize design, translate design, map design, place and route design, and export files.

The Reports view provides a way to examine and print process reports. Reports view displays reports for the major processes. There are two panes in the Reports view. The left pane lists the design summary information including the reports types. The reports in detail are displayed in the right pane. You can navigate the reports quickly by using the Find function.

Section	Description
Project Summary	Lists the summary information of the project including module name, synthesis tool chosen, implementation name, strategy name, target device, device family, device type, package type, performance grade, operating conditions, logic preference file, software product version, project file name, and location, etc.

Section	Description
Process Reports	Lists the synthesis, map, place and route, signal/pad, bitstream reports in HTML format.
	Lists the map trace, place and route trace, I/O timing analysis, IO SSO analysis reports.

Log messages are displayed in the Output frame of the Diamond main window.

Next you will learn how to explore and analyze the HDL design.

Task 2: Running Analysis Tools

Diamond provides an HDL visualization and rule-checks to detect coding style violations that may lead to pre-/post-synthesis simulation mismatches.

To analyze and view the HDL design:

1. Choose **Design > Generate Hierarchy** or click the Generate Hierarchy

icon 🛃.

The file list is scanned and a syntax check is performed. The Module Library, Dictionary, Hierarchy views, as well as the HDL Diagram appear in the Diamond main window and are populated with details about the VHDL modules and other symbols like signals and ports of the HDL design.

The Module Library view is a standard tree-list view that shows all the modules in the loaded design, used and unused. You can open the entries in this view to browse the complete port, signal, behavioral block, and instance hierarchies within each module of the loaded design.

The Dictionary view shows a sorted list of all the elements in the design. Within the list, design elements are grouped by name instead of by type. This view is very useful for finding design elements.

The Hierarchy view is a mirror of the current view of the HDL Diagram and presents Ports, Signals, Instances, and Continuous Assignments for the current level of hierarchy.

Note

By default, only modules and instances are displayed in the Module Library view, Hierarchy view, and the Dictionary view. If you want to have a full display of the hierarchy of the design, turn off the **Simplified Hierarchy Display** option from the Options dialog (**Tools > Options** from the Diamond main window) the HDL Diagram section.

The Design view shows a graphical display of the HDL module hierarchy of the design.

Details about the scan appear in the Output frame.

2. Choose **Design > Run BKM Check**. Best Known Methods (BKM) analysis is run.

Best Known Methods (BKM) are design guidelines that HDL Diagram uses to analyze your design. BKM checks include the following:

Connectivity – Checks the pin connectivity of instances throughout the design.

Synthesis – Checks for violations of the Sunburst Design coding styles, as well as other potential synthesis problems.

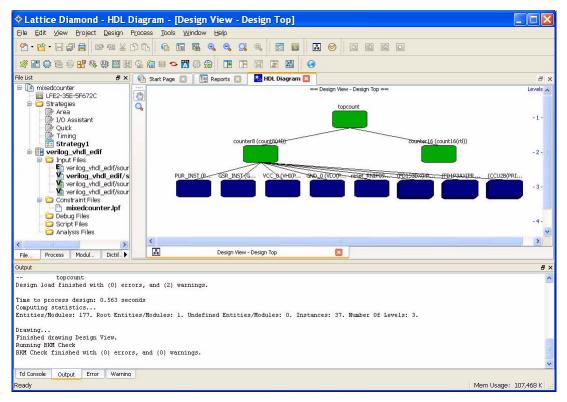
Structural Fan-Out – Checks for maximum structural fan-out violations.

Coding Styles – Colors modules based on their line count, colors pins and ports based on their width, validates module names, and also performs big-endian or little-endian checks on all ports.

Verification – Validates the existence and timestamps of VCD files. A series of Lint-like RTL rule checks are run. Modules that have rule violations are color coded in the HDL Diagram view.

The checks performed during a BKM run can be customized in the **Options** dialog (**Tools > Options** from the Diamond main window) HDL Diagram section.

It is a good practice to run RTL analysis before synthesis to detect coding style that could lead to mismatches between pre-synthesis and post-synthesis simulation results. The analysis views are also excellent documentation output for your design.



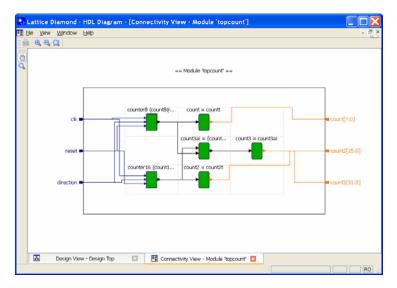
3. After running the BKM check, you might encounter warning and error messages. Error and warning messages are displayed in the Output,

Warning, and Error frames. In the Output, Error, or Warning frames, if you double click the message, the very source indicated in the message will be opened in the associated editor. This cross-probing function can ease your check of the source file.

For this tutorial, there is no error and warning after running the BKM check.

 Double click the topcount block from the HDL Diagram Design view, or right-click the topcount block and choose View Connectivity. The Connectivity view appears as a new tab. You can click the Detach Tool

icon on the upper right corner the HDL Diagram to make it a separate window. The Connectivity view shows signal flow between module ports, internal instances and the behavioral blocks within a particular instance or module. It enables you to explore the signal connectivity—signals and bundles—between instances and behavioral blocks within the current module.



- When you finish checking the signal connectivity, you can choose Window > Attach Window from the separated HDL Diagram to make it back to the Diamond main window.
- 6. After running the design analysis tool, you can see the top-level source **topcount** is bold-faced in the File List view.

Task 3: Inspect Strategy Settings

A **strategy** is a collection of settings for controlling the different stages of the implementation process (synthesis, map, place & route, and so on). Strategies can control whether the design is optimized for area or speed, how long place and route takes, and many other factors. Diamond provides a default strategy, which may be a good collection to start with, and some variations that you can try. You can modify **Strategy1** and create other strategies to experiment with or to use in different circumstances.

To adjust synthesis settings:

 From the File List view, double-click Strategy1. The Strategies -Strategy1 dialog appears. Browse to Synthesis > Synplify Pro. A set of default global synthesis timing constraints and optimization setting appear in the panel. Synplify Pro settings are displayed as the default in the dialog.

For information on SDC file usage in Synplify, see the Synplify and Synplify Pro for Lattice Reference Manual in the Synplify Pro for Lattice installation directory.

2. Specify the following setting for Synplify Pro:

Number of Critical Paths: 10

		Synplify Pro		
		Display catalog: All 💽 Defau	lt	
Precision ranslate Design Name Type	Value	^		
Allow Duplicate Modules	T/F	False		
Area	T/F	False		
Arrange VHDL Files	T/F	True		
Command line Options	Text			
Default Enum Encoding	List	Default		
Disable IO Insertion	T/F	False		
FSM Encoding	T/F	True		
Fanout Limit	Num	100		
Fix Gated Clocks [0-3]	Num	3	5	
Fix Generated Clocks [0-3]	Num	3		
Force GSR	List	False		
Frequency (MHz)	Num	200		
Number of Critical Paths	Num	10 3		
Number of Start/End Points	Num	0	~	
	Allow Duplicate Modules Area Arrange VHDL Files Command line Options Default Enum Encoding Disable IO Insertion FSM Encoding Fanout Limit Fix Gated Clocks [0-3] Fix Generated Clocks [0-3] Force GSR Frequency (MHz) Number of Start/End Points	Allow Duplicate Modules T/F Arrange VHDL Files T/F Command line Options Text Default Enum Encoding List Disable 10 Insertion T/F FSM Encoding T/F Fanout Limit Num Fix Gated Clocks [0-3] Num Force GSR List Frequency (MHz) Num Number of Critical Paths Num	Name Type Value Allow Duplicate Modules T/F False Area T/F False Arrange VHDL Files T/F True Command line Options Text Default Enum Encoding Default Enum Encoding List Default Disable 10 Insertion T/F False FSM Encoding T/F True Fanout Limit Num 100 Fix Gated Clocks [0-3] Num 3 Force GSR List False Frequency (MHz) Num 200 Number of Critical Paths Num 10	

Note

When each strategy is selected, descriptive text appears in the lower panel of the dialog.

3. Choose OK. Global synthesis options are now set for the design.

Task 4: Examine Resources

Diamond provides visualization tools to help you understand and document the physical resources of the target device and the utilization of resources. You can browse and locate device features independent of the project's source files. After synthesis, you can view the calculated resource utilization. To browse device resources:

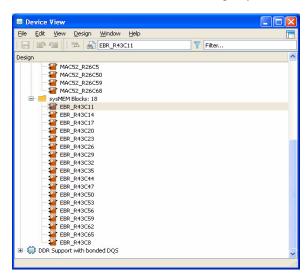
1. Choose Tools > Device View. The Device view appears. Click the Detach

Tool icon an the upper right corner the Device view to make it a separate window. An index of the physical resources of the target device appear.

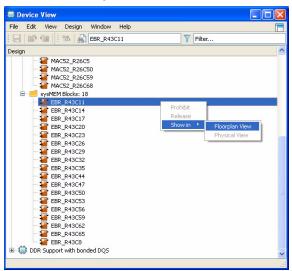
- 2. Click the 🖶 icon to expand the Device folder. Several folders organized by feature type appear.
- 3. Expand the sysDSP Blocks and sysMEM Blocks folders.

Eight sysDSP blocks and 18 sysMEM blocks appear.

4. Type **EBR_R43C11** into the Find entry box at the top of the Device View. The first occurrence of an EBR design symbol is highlighted.



5. Select the EBR_R43C11 in the list. Right-click EBR_R43C11 and choose **Show in > Floorplan View**.



Floorplan View provides a large-component layout of your design. It displays user constraints from the logical preference file (.lpf) and placement and routing information.

6. Close the Floorplan view and the Device view.

After synthesis, you can view the calculated utilization of resources.

To synthesize the design and examine resource utilization:

- 1. From the Process View, double-click Synthesize Design.
- 2. When the synthesis process is complete, select the **Hierarchy Post Synthesis Resources** tab.

Unit	Regist	ers C	arry Cells	Instantiated	
i⊟- topcount ⊕- Ports ⊕- Signals	48(0)		(0)	65(65)	
 Continuous Assignments Count16_uniq_0(rtl)(counter 	16) 48(48)	9((9)	0(0)	
🗄 📑 count8(rtl)(counter8)	0(0)	0((0)	0(0)	
Hierarchy - Post Synthesis Resources	File List	Process	Module library	Dictionary	

The Post-Synthesis Hierarchy View displays the number of logical resources within each level of the design.

Task 5: Set Timing and Location Assignments

Timing and location assignments constrain logic synthesis, as well as back-end map, place, and route programs to help meet your design requirements. A well constrained design helps optimization algorithms work as efficiently as possible. In this section you'll set default timing constraints for the operating frequency and I/O timing then assign package pins to specific I/O signals.

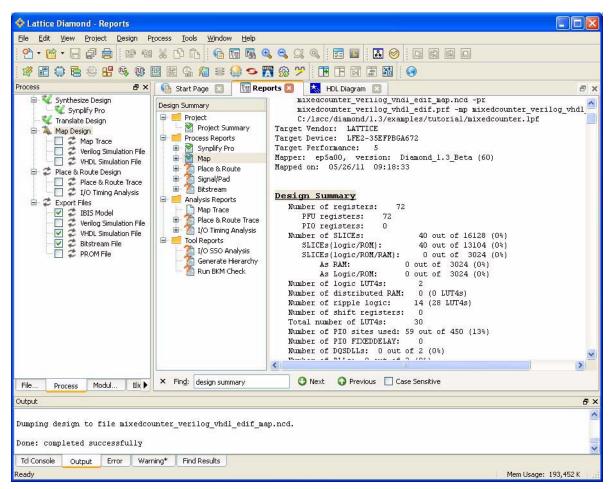
To set timing and location assignments:

 From the Process view, double-click Translate Design and then Map Design. The batch interface to logic synthesis, EDIF translation, and the design mapper run. Report files appears in the Reports view. To view each process report, select the process in the Design Summary pane.

Each major stage of an FPGA implementation is illustrated as a milestone in the Process view: Synthesize Design, Translate Design, Map Design, Place&Route Design, and Export Files. The status of any stage is represented by the following color-coded icons:

 Completed (Green check mark) - The stage completed successfully and produced output.

- Warning (Yellow Exclamation mark) The stage completed with warning messages generated. You can go to the Warning panel to view the warning messages.
- Error (Red cross mark) The stage failed. You can go to the Error panel to view the error messages.
- From the Design Summary pane of the Reports view, select Process Reports > Map. The Map Report appears in the right panel.
- 3. Right click in the right pane of the Reports view, choose **Find in Text...** Type in **Design Summary**. The report highlights the Design Summary section of the report.



- 4. Choose Tools > Spreadsheet View. The Spreadsheet View appears. The Spreadsheet View is one of several preference editors available to you to define timing, I/O and floorplan constraints for the place and route tools. Preferences are organized by type into separate tabs of the Spreadsheet View.
- 5. Click the **Detach Tool** icon at the upper right corner of the Spreadsheet view. The Spreadsheet View is detached from the Diamond main window.

- 6. Click the **Period/Frequency** icon *i* on the Spreadsheet View tool bar. The Period/Frequency Preference dialog appears.
- 7. Enter the following preference settings:

Туре:	FREQUENCY
Second Type:	Clock Net
Available Clock Nets:	clk_c
Frequency:	100MHz

Click **OK**. The Timing Preferences tab of the Spreadsheet View appears with the new **FREQUENCY** preference defined.

- Click the Input_setup/Clock_to_out button is on the Spreadsheet View toolbar. The INPUT_SETUP/CLOCK_TO_OUT Preference dialog appears.
- 9. Enter the following preference settings:

Туре:	INPUT_SETUP
Second Type:	All Ports
Clock Ports/Nets:	clk
Time:	10ns

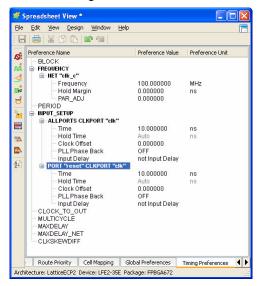
Click **OK**. The Timing Preferences tab of the Spreadsheet View appears with the new **INPUT_SETUP** preference defined. So, you can define preferences in the relevant preference dialog.

- 10. From the Timing Preference tab, right-click the INPUT_SETUP entry, and select **New INPUT_SETUP...** The INPUT_SETUP/CLOCK_TO_OUTPUT Preference dialog appears.
- 11. Enter the following settings:

Туре:	INPUT_SETUP
Second Type:	Individual Ports
Available Input Ports:	reset
Clock Ports/Nets;	clk
Time:	10ns

Click **OK**. The Timing Preference tab of the Spreadsheet View appears with the new INPUT_SETUP preference defined.

The preference dialog can be invoked from the toolbar icon, the menu item (**Edit > Preferences** from the Spreadsheet view), or from the right-click menu of the Spreadsheet view. You can also double click on a



value in Timing Preferences tab and edit the value directly.

- 12. Select the Port Assignments sheet from the Spreadsheet view.
- 13. Right click the IO_Type cell of the All Ports row. A pull-down menu of signal standards appears. Select LVCMOS33. The port attributes display is updated with the new IO_TYPE. Cell entries in the Spread Sheet view are color-coded to indicate the source of a preference setting:
 - Black User-defined setting.
 - Blue Default.
 - Orange Implied by another user-defined setting.
- Click the Name column to sort the port names. Select port count2_0 through count2_8. Right-click a Bank cell of the selection and choose Bank > 3 from the pop-up menu.

	dit View Design 1						
	Type	Name	Pin	Bank	Vref	IO TYPE	PULLM
1			N/A	N/A	N/A	LVCMOS33	UP
2	Output Port	count2_0			N/A	IVCMOS25	UP
3	Output Port	count2_1			Delete Selecte		UP
4	Output Port	count2_2			Clear Show in Pack	Del arre View	UP
5	🔄 🕘 Output Port	count2_3			Assign Pins	ago non	UP
6	Output Port	count2_4			Bank	×.	0
7	Output Port	count2_5			IO_TYPE	۲	1
8	🛛 🦪 Output Port	count2_6			PULLMODE		2
9	🛛 🥶 Output Port	count2_7			DRIVE SLEWRATE	F	3
10	0 🦪 Output Port	count2_8	-		PCICLAMP	×	5
1	1 🗈 Clock Input	clk			OPENDRAIN	٠	6
13	2 🦪 Output Port	count2_9			Outload MaxSkew		7
1	3 🦪 Output Port	count2_10			Maxskew SwitchingID		
14	4 🦪 Output Port	count2_11			Ground plane		UP
15	5 🦪 Output Port	count2 12			Power plane F SSO Allowanc		UP ,

The Bank cells are updated for the selected range of ports.

- Choose File > Save mixedcounter.lpf from the detached Spreadsheet View. The project Logical Preference File (.lpf) is updated. Close the Spreadsheet view.
- 16. From the File List view of the Diamond main window, Constraints Files folder, double-click the mixedcounter.lpf file. The Source Editor appears with the ASCII LPF file. Note the timing and location preferences defined so far. Close the Source Editor.

Task 6: Running Place and Route

Use the Process view to run the Translate Design, Map Design, and Place&Route Design process stages.

To run place and route:

- 1. From the Process List double-click **Place & Route Design**. The place and route tools are run. Intermediate results appear in the Output frame of the Diamond main window.
- From the Design Summary pane of the Reports view, find the Process Reports section. You will find a green check mark appears before the reports generated successfully. Click the
 icon in front of Process Reports to expand the section. Select Place & Route. Details about Place & Route appear in the pane to the right.
- 3. From the Process List double-click **Place & Route Trace**. The TRACE timing analyzer is run.

- 4. From the **Design Summary** pane of the Reports view, expand **Analysis Reports**, and then select **Place & Route Trace** to view the report in the pane to the right.
- 5. From the Process List double-click **I/O Timing Analysis**. The timing analysis is run.
- 6. From the **Design Summary** pane of the Reports view, select the **I/O Timing Analysis** section of Analysis Reports. The I/O Timing Report appears in the right pane of the Reports view.

Task 7: Examine Post Place and Route Results

You can use the Timing Analysis view to examine the timing analysis results.

Examine timing analysis results:

- 1. Choose **Tools > Timing Analysis View**. The Timing Analysis view appears.
- 2. Click the **Detach Tool** icon from the right corner of the Timing Analysis view. The Timing Analysis view is detached from the Diamond main window.

A summary of the post-route static timing analysis settings such as target device information, preference file, performance grade, and environment conditions appear in the upper left pane. The lower left pane provides an index of the available analysis results. Related timing preferences appear in each analysis section.

- 3. From the Analysis pane (on the lower left of the Timing Analysis view), select **INPUT_SETUP ALLPORTS 10ns CLKPORT "clk" setup**. The Path Table is populated in the upper right of the Timing Analysis view, with the Source, Destination, Weighted Slack, Arrival, Required, Data Delay, Route %, Levels, and other details.
- 4. Select Row 1 of the Path Table. The Detailed Path Tables in the lower pane are populated with details.
- 5. Choose **Edit > Settings**, or click the Settings icon from the toolbar in the Timing Analysis view. The Settings dialog appears.
- 6. Enter **20** into the Worst-Case Paths field and click **OK**. The Timing Analysis view is refreshed with the additional path data.

Setup Performa	nce Grade	Hold Performance Grade
Current:	Default 💌	Current: Default
Check Uncons		
Report Async	trained Paths hronous Timing Loops	
The second is		M

- 7. You can use the Source Filter field of the Path Table to filter out all the wanted paths. Delete the text from the Source Filter field, all the sources appear in the Source list again.
- 8. Select the first row in the **Path Table**. The Detailed Path Tables are updated.
- 9. Select the **Data Path Details** tab. Each component of the data path delay is identified alternating between route delays and combinatorial or clock-to-output type delays.

e <u>E</u> dit <u>V</u> iew <u>W</u> indow	Help														
Settings	Values	Path T	Path Table - "INPUT_SETUP ALLPORTS 10.000000 ns CLKPORT "clk" " (setup)										1		
Device Family LatticeECP2 Device LFE2-35E Package FPBGA672 Setup Performance G Default	Source Filter: Destination filter:										Case sensitive				
Hold Performance Gr	Default		Des	stinatio	n	Weighted Sla	ck 🔶 Arrival	Required	Data Delay	Route %	Levels	Clock Skew	Setup/Hold	Jitter	Color
Check Unconstrained Report Asynchronous		1	counter1	6/count:	ai_15	7.795	2.205	10	3.574	45.1	10	0	0.081	0	
Report Style	Verbose Timing	2	counter1	6/count:	2ai_14	7.806	2.194	10	3.563	45.3	9	0	0.081	0	1
Full Name Worst-Case Paths	No 20	3	counter1	6/count2	ai_15	7.873	2.127	10	3.496	46.1	10	0	0.081	0	
Worse Case Faults	20	4	counter1	6/count:	ai_15	7.883	2.117	10	3.486	46.3	9	0	0.081	0	
		5	counter1	6/count;	ai_13	7.883	2.117	10	3.486	46.3	9	0	0.081	0	
	6	counter1	6/count:	ai_14	7.884	2.116	10	3.485	46.3	9	0	0.081	0		
	7	counter1	6/count2	2ai 12	7.894	2.106	10	3.475	46.4	8	0	0.081	0		
ence Name		8	counter1	6/count2	ai_14	7.894	2.106	10	3.475	46.4	8	0	0.081	0	
Analysis Results		9	counter1	6/count:	ai_15	7.961	2.039	10	3.408	47.3	9	0	0.081	0	
🛃 FREQUENCY NET		<		Ū.											>
FREQUENCY NET															
INPUT_SETUPALL		boromo	ed Path Tab												
	PORTS 10.000000 n:	-	Path Detai		urce Clo		1.22								
PUT_SETUP PO	RT "reset" 10.000000 RT "reset" 10.000000					Destination	Resource								
INPUT_SETUP PO		PA				Y17.PADDI									
		R0		1.613											
		C0		0.491		R51C64A									
		R0	10000	0	R51		counter								
		FCI		0.088			counter								
		R0		0	R51	R51C64	counter								
		FCI	. 0	0.088		R51C64	counter								
<	1 (20)	Dete	iled Path Ta	0	ne4 Schoma	tic Path view	Report: setup								

10. Select the **Schematic Path view.** A schematic graphic of the data path timing path appears.

Settings	Values	Path	Table - "INPUT	SETUP ALLPORTS 10.00000	0 ns CLKPORT "clk" "	Path Table - "INPUT_SETUP ALLPORTS 10.000000 ns CLKPORT "ck" " (setup)										
Device LFE2-35		Source Filter:								e sensitive						
Check Unconstrained		_	Source	Destination	Yeighted Slacl 🐣	Arrival	Required	Data Delay	Route %	Levels						
ReportAsynchronous	. No	1	direction	counter16/count2ai_15	6.534	3.466	10	4.835	59.4	10						
Report Style Full Name	Verbose Timing Report No	2	direction	counter16/count2ai_14	6.545	3.455	10	4.824	59.6	9						
Worst-Case Paths	20	3	direction	counter16/count2ai_15	6.612	3.388	10	4.757	60.4	10						
		4	direction	counter16/count2ai_13	6.622	3.378	10	4.747	60.5	9						
ence Name		5	direction	counter16/count2ai_15	6.622	3.378	10	4.747	60.5	9						
Analysis Results		6	direction	counter16/count2ai 14	6.623	3.377	10	4.746	60.6	9						
	alle al 100.000000 MUz	-														
FREQUENCY NET	'clk_c" 100.000000 MHz 'clk_c" 100.000000 MHz PORTS 10.000000 ns CLK PORTS 10.000000 ns CLK PORTS 10.000000 ns CL RT"reset" 10.000000 ns Cl RT"reset" 10.000000 ns Cl	Scher Pin:di	matic Path view matic Path view irrection Pin:counter1	nounterl Elecuntici 14		3 367	10	1 736	en 7	•						
FREQUENCY NET	'clk_c" 100.000000 MHz PORTS 10.000000 ns CLK PORTS 10.000000 ns CLK	Sche Pin:di tion I th De	direction matic Path view	acumtert Glacuptica 1.1		3.367	40	4.736	60.7							
FREQUENCY NET	'clk_c" 100.000000 MHz PORTS 10.000000 ns CLK PORTS 10.000000 ns CLK PORTS 10.000000 ns CLK RT "reset" 10.000000 ns CL	Sche Pin:di tion I th De	direction matic Path view irection Pinscounter 1 elay: 4.835 0.081	acumtert Glacuptica 1.1	E CO Counter16/coun	0.088	FCO counter16/c	0.088	FCO counter16/c	0.0 FCI						
FREQUENCY NET	'clk_c" 100.000000 MHz PORTS 10.000000 ns CLK PORTS 10.000000 ns CLK PORTS 10.000000 ns CLK RT "reset" 10.000000 ns CL	Sche Pin:di tion I th De ime:	direction matic Path view irection Pincounter 1 alay: 4.835 0.081	6/count2ai_15	E CO Counter16/coun	0.088	FCO counter16/c	0.088FCI	FCO counter16/c	0.0 FCI oun						

Task 8: Adjust Static Timing Constraints and Review Results

In this task, you will edit timing constraints for STA (Static Timing Analysis) using the Timing Preference File (TPF) version of Spreadsheet View, and then you will use Timing Analysis view to review the results.

Timing analysis within Lattice Diamond can be performed at three points in a typical design flow: post-synthesis, post-map when the post-synthesis netlist of the design has been translated to the target device, post-placement, and post-route. Each stage provides a progressively more accurate report of delay characteristics. Timing analysis at the synthesis stage is performed by the respective synthesis tool: Synplify Pro or Precision. Additional features are provided by Diamond for post-map stages of STA.

By default, the timing analysis engine, TRACE, uses those timing constraints applied by timing-driven map, place, and route. However, timing preferences can be modified, which allows you to manage the timing objectives of the implementation tools independent of static timing analysis. To accommodate an experimental static timing analysis loop, theTPF Spreadsheet View allows you to edit the timing preferences for use with the Timing Analysis view. This allows you to establish modified or additional timing preferences independent of the constraint set used for MPAR.

Tighten the timing objective of a preference and examine the results:

1. From the Preference Name list on the lower left of Timing Analysis View, select **INPUT_SETUP ALLPORTS 10ns CLKPORT "clk" Setup**, right-click and choose **TPF Preferences**.

Spreadsheet View – TPF appears.

 Select the Timing Preferences sheet of the TPF Spreadsheet View. Right-click 10.00000ns in the Preference Value column for the ALLPORTS CLKPORT "clk" and choose Edit Value. Enter 15ns into the Preference Value field and press Enter.

🗳 Spreadsheet V	/iew - TPF *		
<u>File E</u> dit <u>W</u> indow	r <u>H</u> elp		
1 🖶 🚍 🗶 🖒 1	S 😰 🛍 🛛		
Rreference Nam	ie	Preference Value	Preferenc
부 Frequered Hold I	Margin	100.000000 0.000000 0.000000	MHz ns
INPUT_SET	UP TS CLKPORT "cik"		
Time Hold Clock PLL F Input	Time Offset Phase Back	15.000000 0.000000 0.000000 OFF not Input Delay	ns ns
Time Hold " Clock	Time Offset Phase Back Delay	10.000000 0.000000 0.000000 OFF not Input Delay	ns ns
<	Ш		>
Global Preferen	ces Timing Prefere	ences Group	
Architecture: Lattice	ECP2 Device: LFE2-3	ISE Package: FPBGA6	72 .::

3. After a few moments, return to Timing Analysis View.

The Update button 📓 on the toolbar is now rotating.

4. Click the **Update** button. After a short while, the indicator stops rotating and the new analysis results become available in Timing Analysis View.

In the title bar of Timing Analysis View, "Untitled" appears with an asterisk, which indicates an in-memory change to the timing preferences. You can save the change to a Timing Preference File (.tpf) by choosing **Save > Save Untitled As** and giving it a name and location. The .tpf file will then appear in the Analysis Files folder of the File List Pane. These .tpf files enable you to experiment with different timing settings without affecting the .lpf source file. For more information, see "Using Timing Analysis View" in the "Analyzing Static Timing" section of the Diamond online Help.

5. Close Timing Analysis View and Spreadsheet View – TPF. In the Save dialog box, click **No** to discard the change.

Task 9: Comparing Multiple Place and Route Runs

Use the Run Manager to run multiple synthesis and place and route passes, compare the timing score results, and load the native circuit description (NCD) database of the best run into the workspace for further analysis.

You can create multiple strategies or implementations for the design. Then compare the runs with different implementation and strategy combination. One implementation can only be bound with one active strategy.

Now let's create a new implementation.

To create a new implementation:

1. Choose File > New > Implementation from the Diamond main window.

Or, right click on the project name icon \downarrow from the File List view and choose **Add > New Implementation**.

- 2. In the New Implementation dialog box, type **verilog_vhdl** in the Name text box. By default, the directory and location will be the same name as the implementation name. You can change the directory or location to a desired one.
- 3. Choose Strategy1 from the default strategy drop-down menu.
- 4. Click Add Source and choose Browser.
- In the Import File dialog box, navigate to <...\diamond_install_directory\version#\examples\mixedcounter\source>.
- 6. Select **topcount.v**, **typepackge.vhd**, and **typecount.vhd** and click **Open**. The selected sources are listed in the Source Files field.
- 7. Select the "Copy source to implementation directory" option and click OK.

The new implementation **verilog_vhdl** is now displayed in the File List pane.

Note

If you want to make this new implementation active, right-click **verilog_vhdl** and choose **Set as Active Implementation**. You can have multiple implementations in your project, but you can make only one implementation active in your project at one time.

Now you will compare the run results of the **verilog_vhdl_edif** and **verilog_vhdl** implementations.

- 1. From the Diamond main window, choose **Tools > Run Manager**.
- The Run Manager displays a table of implementation<strategy>: verilog_vhdl_edif<Strategy1> and verilog_vhdl<Strategy1>.
- Enable the verilog_vhdl_edif<Strategy1> and verilog_vhdl<Strategy1> by setting the check boxes for each. You will see the verilog_vhdl_edif<Strategy1> implementation has the status of 100% in Progress.
- 4. Click the **Rerun** button on the Run Manager toolbar. The two implementations start to run simultaneously.

Window								[
Implementation <strategy></strategy>	Status	Progress	Start	Run Time	Score	Unrouted	Level/Cost	Description
🕀 🗹 verilog_vhdl_edif <strategy1></strategy1>	Running	1 9%	Thu May 26 10:53:25 2011	96	NA	NA	NA	verilog_vhdl_ed
veriliog_vhdl <strategy1></strategy1>	Running	19%	Thu May 26 10:53:25 2011	96	NA	NA	NA	veriliog_vhdl

In a few minutes, the results of the run appear in the table. Statistics such as Start time, Run time, Score, Unrouted, Level/Cost, and Description appear. The row in bold font indicates the active implementation that is loaded. The table provides a quick review of the quality of results produced by a particular strategy. To closely examine a particular run with analysis tools, such Timing Analysis View or Power Calculator, you can set the active strategy to be loaded.

If your system provides a multiple-core processor, you can set more implementations to be run concurrently. Go to the **Options** dialog (**Tools** > **Options**) of the Diamond main window, **Environment** > **General** tab, the **Maximum number of processes in run manager** option. Enter a number in the box in front of this option. The default value is 2. The maximum allowed value is 16.

 Choose View > Reports. In Reports View, you can view results related to the run of the current active implementation. The report for verilog_vhdl_edif appears in Reports View.

Note

To view report of the inactive implementation, right click on the inactive implementation in the File List pane and choose **Set as Active Implementation**. Only reports of the current active implementation are displayed in the Reports view.

Task 10: Running Export Utility Programs

Use the Process view to generate files for exporting.

- 1. From the Process view, choose **Export Files**. A set of export files appear under the Export Files process.
- 2. Select the following Export Files:

IBIS Model

VHDL Simulation File

Bitstream File

3. Click the **Run** button Diamond toolbar. Diamond generates the selected files and saves them in your project directory.