NEC LCD Technologies, Ltd.

CONTROLLER FOR TFT COLOR LCD MODULE

S1L50282F23K200

Adaptable LCD Modules

Type: NL2432DR22-xxB
Type: NL2432HC22-xxA
Type: NL2432HC22-xxB

SPECIFICATIONS

(1st edition)

Signature of writer	
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NEC LCD Technologies, Ltd.

INTRODUCTION

• WARRANTY

NEC LCD Technologies, Ltd. (hereinafter called "NEC") warrants that this product meets the product specifications set forth in this document. If this product under normal operation is found to be non-conforming to the product specifications, and such non-conformance is promptly notified to NEC within one (1) year after the delivery date, and further such non-conformance is solely attributable to NEC, NEC shall replace the non-conforming product free of charge. However, this warranty does not apply to any non-conformance that can be found easily by incoming inspections or those resulting from any one of the following:

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2) Any other causes attributable to customer

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If NEC is planning the discontinuation of the product, NEC shall inform it to the customer in advance.

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For the purpose of product improvement, this product design may be changed for specifications, appearance, circuits and so on. In case a design change is affected on the product specifications, NEC shall inform it to customers in advance.

• HANDLING OF DOUBTFUL POINTS

Any question arising out of, or in connection with, this SPECIFICATION or any matter not stipulated herein will be settled each time upon consultation between both parties.

CONTENTS

1. DESCRIPTION

The S1L50282F23K200 is a timing controller LSI for active matrix color LCD display suitable for NEC's NL2432DR22-xxB, NL2432HC22-xxA and NL2432HC22-xxB series.

This controller converts 6 bit per color video signals to interfacing driver signals of LCD modules.

2. FEATURES

- Wide adaptable resolutions (QVGA Portrait / QVGA Landscape / HVGA)
- DE Mode (DE synchronization)
- DE noise reduction function
- Output data inversion function
- Source driver output enable function
- HOE pulse width selection switch
- Over-current protection circuit for gate driver
- Polarity change function
- DCK polarity change function

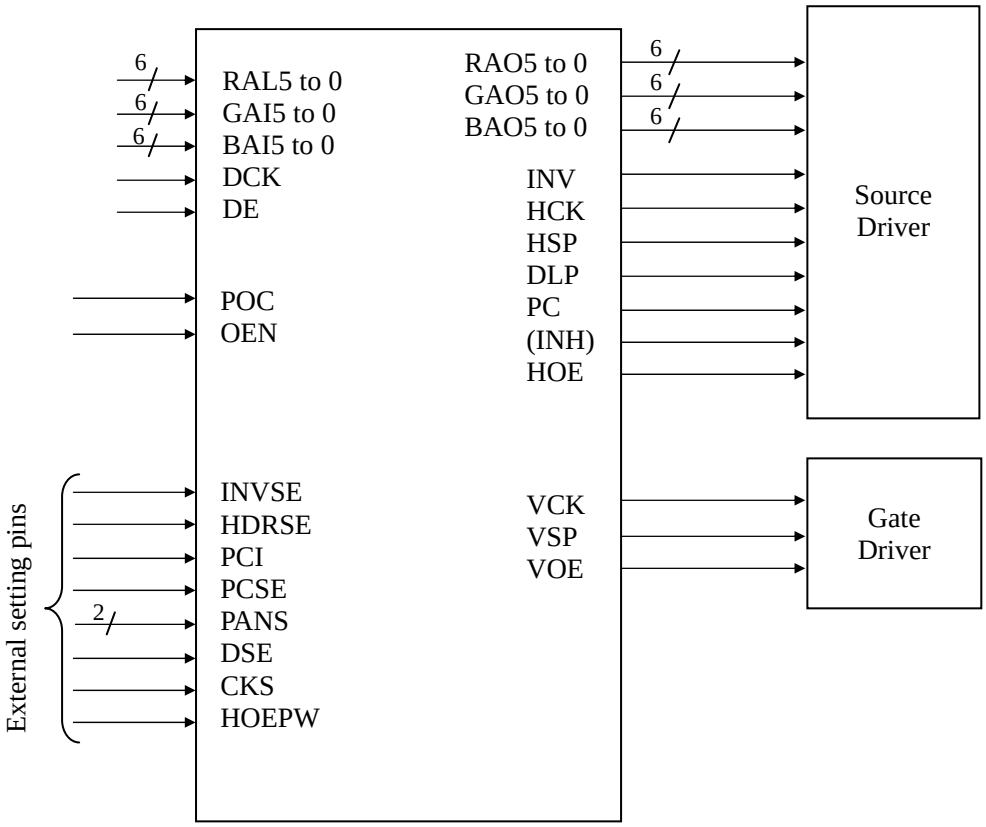
3. APPLICATIONS

- NEC NL2432DR22-xxB, NL2432HC22-xxA, NL2432HC22-xxB
- QVGA (portrait / landscape), HVGA LCD Module (6-bit 1 port input / 6-bit 1 port output)

4. OUTLINES OF CHARACTERISITCS

Resolution	QVGA landscape mode (320×240 pixels)
	QVGA portrait mode (240×320 pixels)
	HVGA mode (640×240 pixels)
Supply Voltage	VDD=2.25 to 3.6V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Power Consumption	12mW (DCK= 6.36MHz, VDD= 3.3V)
Package	TQFP-80pin (12.1mm×12.1mm×1.1mm)

5. BLOCK DIAGRAM



6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remarks
Supply voltage	VDD	-0.3 to +4.0	V	-
Input voltage	VI	-0.3 to VDD+0.5	V	-
Output voltage	VO	-0.3 to VDD +0.5	V	-
Output current	IOUT	±30	mA	-
Storage temperature	Tstg	-65 to +150	℃	-

6.2 Recommended Operating Conditions

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Supply voltage	VDD	2.25	3.0	3.6	V	-
Input voltage	VI	0	-	VDD	V	-
Operating temperature	Ta	-40	-	+85	℃	-

6.3 DC Characteristics (VDD= 3.0V)

Parameter			Symbol	Conditions	min.	typ.	max.	Unit	Remarks
Static current consumption			IDDS	VI=VDD or VSS VDD= max. IOH=IOL=0	-	-	415	µA	-
Input leakage current			ILI	VDD= max. VIH=VDD VIL=VSS	-1	-	1	µA	-
Input Characteristics	IBC, IBCD1	H level input voltage	VIH1	VDD= max.	1.9	-	-	V	-
		L level input voltage	VIL1	VDD= min.	-	-	0.8	V	-
	IBH	H level input voltage	VT+	VDD= max.	1.0	-	2.3	V	-
		L level input voltage	VT-	VDD= min.	0.5	-	1.7	V	-
		Hysteresis voltage	VH1	VDD= min.	0.1	-	-	V	-
	Pull down resistance (IBCD1)	-	RPD1	VI=VDD	24	60	144	kΩ	-
Output Characteristics	OB1T	H level output voltage	VOH1	VDD= min. IOH= -1.0mA	VDD-0.4	-	-	V	-
		L level output voltage	VOL1	VDD= min. IOL= 1.0mA	-	-	VSS+0.4	V	-
	OB2T	H level output voltage	VOH2	VDD= min. IOH= -3mA	VDD-0.4	-	-	V	-
		L level output voltage	VOL2	VDD= min. IOL= 3mA	-	-	VSS+0.4	V	-

7. PIN DESCRIPTION

Pin	Symbol	I/O	I/O Buffer	Output Current	Capacitance	Frequency	Remarks
1	VDD	P	-	-	-	-	Supply Voltage (2.25V to 3.6V)
2	BI5	I	IBC	-	-	7.5MHz	Input Data Blue Bit5
3	BI4	I	IBC	-	-	7.5MHz	Input Data Blue Bit4
4	BI3	I	IBC	-	-	7.5MHz	Input Data Blue Bit3
5	BI2	I	IBC	-	-	7.5MHz	Input Data Blue Bit2
6	BI1	I	IBC	-	-	7.5MHz	Input Data Blue Bit1
7	GND	P	-	-	-	-	Ground
8	BI0	I	IBC	-	-	7.5MHz	Input Data Blue Bit0
9	GI5	I	IBC	-	-	7.5MHz	Input Data Green Bit5
10	GI4	I	IBC	-	-	7.5MHz	Input Data Green Bit4
11	GI3	I	IBC	-	-	7.5MHz	Input Data Green Bit3
12	GI2	I	IBC	-	-	7.5MHz	Input Data Green Bit2
13	GI1	I	IBC	-	-	7.5MHz	Input Data Green Bit1
14	VDD	P	-	-	-	-	Supply Voltage (2.25V to 3.6V)
15	GI0	I	IBC	-	-	7.5MHz	Input Data Green Bit0
16	RI5	I	IBC	-	-	7.5MHz	Input Data Red Bit5
17	RI4	I	IBC	-	-	7.5MHz	Input Data Red Bit4
18	RI3	I	IBC	-	-	7.5MHz	Input Data Red Bit3
19	RI2	I	IBC	-	-	7.5MHz	Input Data Red Bit2
20	GND	P	-	-	-	-	Ground
21	VDD	P	-	-	-	-	Supply Voltage (2.25V to 3.6V)
22	RI1	I	IBC	-	-	7.5MHz	Input Data Red Bit1
23	RI0	I	IBC	-	-	7.5MHz	Input Data Red Bit0
24	GND	P	-	-	-	-	Ground
25	DCK	I	IBC	-	-	15MHz	Dot Clock
26	GND	P	-	-	-	-	Ground
27	DE	I	IBC	-	-	18.75kHz	Data Enable Signal
28	TSTEN2	P	-	-	-	DC	TEST Terminal (0: Normal, 1: Test Mode)
29	OEN	I	IBCD1	-	-	DC	Gate-Driver Output Enable Terminal
30	POC	I	IBH	-	-	-	Power On Clear (0: Reset, 1: Reset OFF)
31	VDD	P	-	-	-	-	Supply Voltage (2.25V to 3.6V)
32	PC	O	OB1T	2mA	40pF	18.75kHz	Polarity Change
33	HOE	O	OB1T	2mA	40pF	18.75kHz	Source-Driver Output Enable Signal
34	INV	O	OB1T	2mA	40pF	7.5MHz	Output Data Inversion Signal
35	DLP	O	OB1T	2mA	40pF	18.75kHz	H-Driver Latch Pulse
36	INH	O	OB1T	2mA	40pF	9.375MHz	H-Driver Inhibit Pulse (not used for NL2432DR22-xxB)
37	HSP	O	OB1T	2mA	20pF	18.75kHz	H-Driver Start Pulse
38	GND	P	-	-	-	-	Ground
39	HCK	O	OB2T	6mA	40pF	15MHz	H-Driver Clock
40	GND	P	-	-	-	-	Ground
41	VDD	P	-	-	-	-	Supply Voltage (2.25V to 3.6V)
42	BO0	O	OB1T	2mA	40pF	7.5MHz	Output Data Blue Bit0
43	BO1	O	OB1T	2mA	40pF	7.5MHz	Output Data Blue Bit1
44	BO2	O	OB1T	2mA	40pF	7.5MHz	Output Data Blue Bit2
45	BO3	O	OB1T	2mA	40pF	7.5MHz	Output Data Blue Bit3
46	BO4	O	OB1T	2mA	40pF	7.5MHz	Output Data Blue Bit4
47	GND	P	-	-	-	-	Ground

Pin	Symbol	I/O	I/O Buffer	Output Current	Capacitance	Frequency	Remarks
48	BO5	O	OB1T	2mA	40pF	7.5MHz	Output Data Blue Bit5
49	GO0	O	OB1T	2mA	40pF	7.5MHz	Output Data Green Bit0
50	GO1	O	OB1T	2mA	40pF	7.5MHz	Output Data Green Bit1
51	GO2	O	OB1T	2mA	40pF	7.5MHz	Output Data Green Bit2
52	GO3	O	OB1T	2mA	40pF	7.5MHz	Output Data Green Bit3
53	GO4	O	OB1T	2mA	40pF	7.5MHz	Output Data Green Bit4
54	VDD	P	-	-	-	-	Supply Voltage (2.25V to 3.6V)
55	GO5	O	OB1T	2mA	40pF	7.5MHz	Output Data Green Bit5
56	RO0	O	OB1T	2mA	40pF	7.5MHz	Output Data Red Bit0
57	RO1	O	OB1T	2mA	40pF	7.5MHz	Output Data Red Bit1
58	RO2	O	OB1T	2mA	40pF	7.5MHz	Output Data Red Bit2
59	RO3	O	OB1T	2mA	40pF	7.5MHz	Output Data Red Bit3
60	GND	P	-	-	-	-	Ground
61	VDD	P	-	-	-	-	Supply Voltage (2.25V to 3.6V)
62	RO4	O	OB1T	2mA	40pF	7.5MHz	Output Data Red Bit4
63	RO5	O	OB1T	2mA	40pF	7.5MHz	Output Data Red Bit5
64	GND	P	-	-	-	-	Ground
65	VCK	O	OB1T	2mA	20pF	18.75kHz	V-Driver Clock
66	VOE	O	OB1T	2mA	20pF	18.75kHz	V-Driver Output Enable Signal
67	VSP	O	OB1T	2mA	20pF	71Hz	V-Driver Start Pulse
68	GND	P	-	-	-	-	Ground
69	HOEPW	I	IBCD1	-	-	DC	HOE Pulse Width Selecting Function
70	DSE	I	IBCD1	-	-	DC	Source-Driver Switching (Set up Terminal)
71	PCI	I	IBCD1	-	-	DC	Polarity Inversion (0: Line inversion, 1: Frame inversion)
72	PANS1	I	IBCD1	-	-	DC	Resolution setting pin 1
73	PANS0	I	IBCD1	-	-	DC	Resolution setting pin 0
74	VDD	P	-	-	-	-	Supply Voltage (2.25V to 3.6V)
75	INVSE	I	IBCD1	-	-	DC	Output Data Reverse (0: OFF, 1: ON)
76	HDRSE	I	IBCD1	-	-	DC	Data Reverse of Internal PC (0: OFF, 1: ON)
77	PCSE	I	IBCD1	-	-	DC	PC Switching (0: Internal PC, 1: Internal PC Reverse)
78	TSTEN	I	ITST1	-	-	DC	Test Terminal (0: Normal, 1: Test Mode)
79	CKS	I	IBCD1	-	-	DC	DCK Reverse (0: Non Reverse, 1: Reverse)
80	GND	P	-	-	-	-	Ground

Buffer and Function

I/O	Buffer	Function
I	IBC	Standard
	IBCD1	Pull down 50kΩ
	IBH	Schmitt
	ITST1	Test Pin
O	OB1T	2mA
	OB2T	6mA

8. FUNCTION

	Setting for NL2432DR22-xxB	Setting for NL2432HC22-xxA NL2432HC22-xxB

8.1 Inversion Setting

PCI	Inversion Mode
0	Line inversion
1	Frame inversion

→ 0 0

8.2 Resolution Setting (Setting of the DLP Start Up)

PANS		Resolution
1	0	
0	0	320×240 (QVGA Landscape)
0	1	640 × 240 (HVGA)
1	1	240 × 320 (QVGA Portrait)

→ 1, 1 1, 1

8.3 Output Data Reverse Setting

INVSE	Output Data Reverse	INV
0	OFF	Low
1	ON	-

→ 1 1

Note1: This function is to change the polarity of video data according to the number of the data change. When the output video data are changed from the previous video data more than 9 times, the High level of the INV signal is output.

8.4 Data Reverse Function for PC

HDRSE	Data Reverse
0	OFF
1	ON

→ 0 0

8.5 PC Setting

PCSE	PC
0	Positive polarity PC signal
1	Negative polarity PC signal

→ 0 0

8.6 DSE Setting

DSE	Driver Selection
0	µPD161602 (NEC)
1	-

→ 0 0

8.7 CKS Setting

CKS	Internal DCK
0	Non Reverse
1	Reverse

→ 0 0

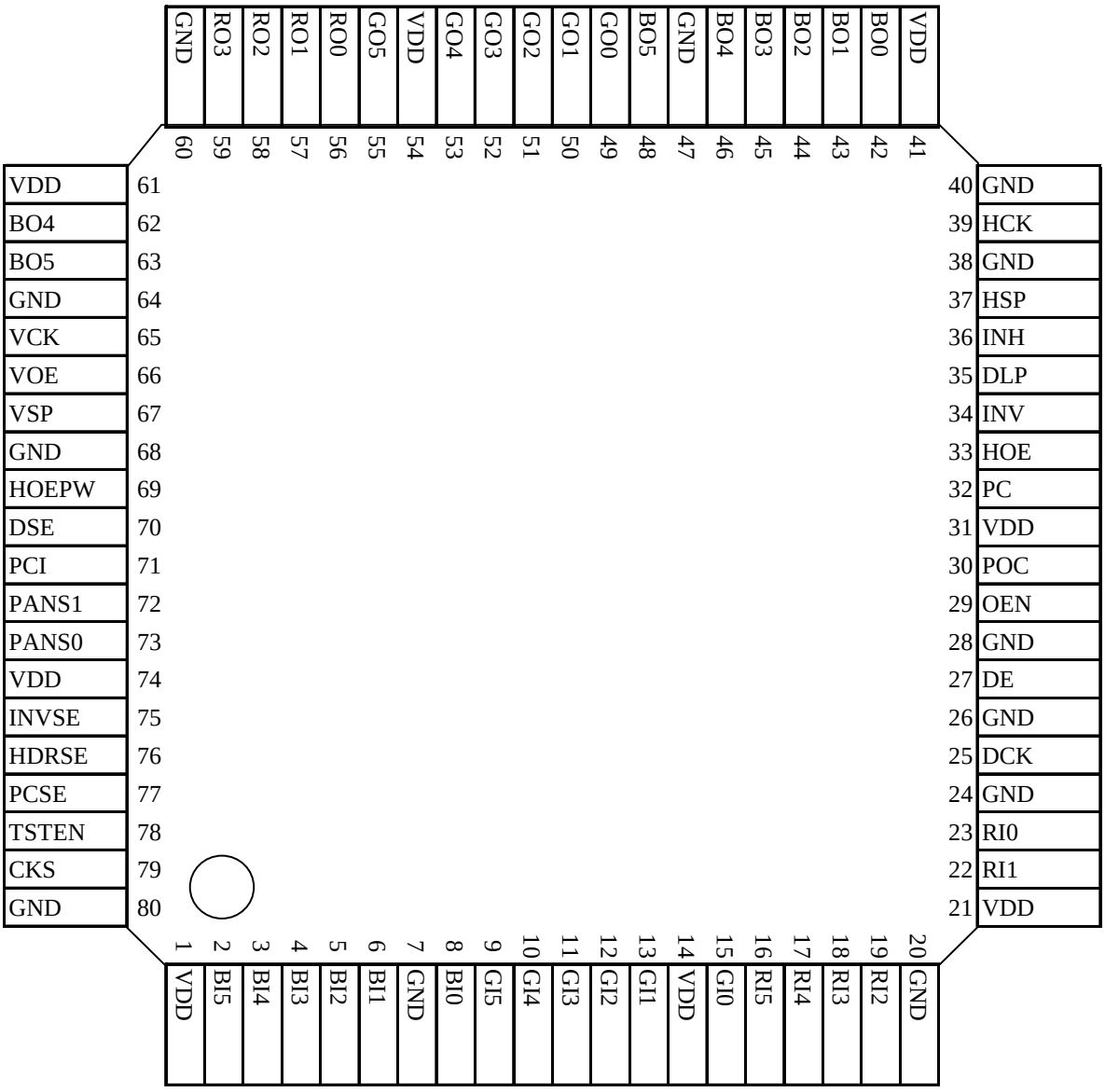
(It will start after CLK down.)

8.8 HOEPW Setting

HOEPW	P
0	20µs
1	15µs

→ 0 1

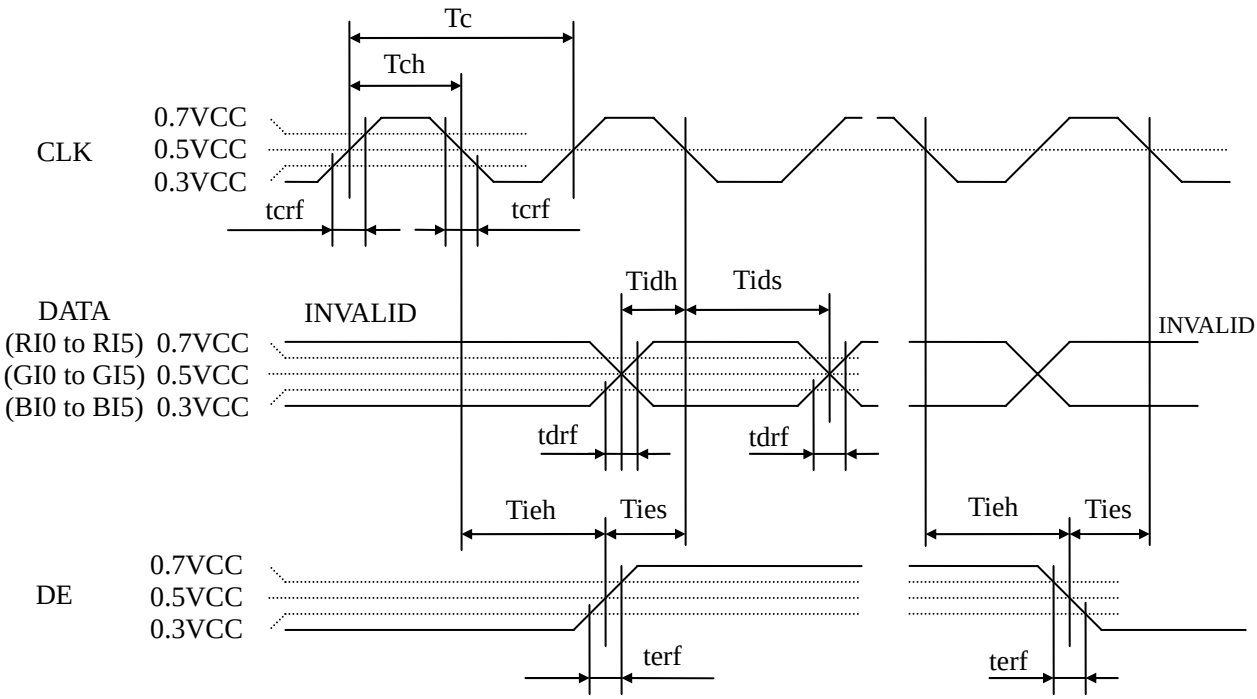
9. PIN ASSIGNMENT

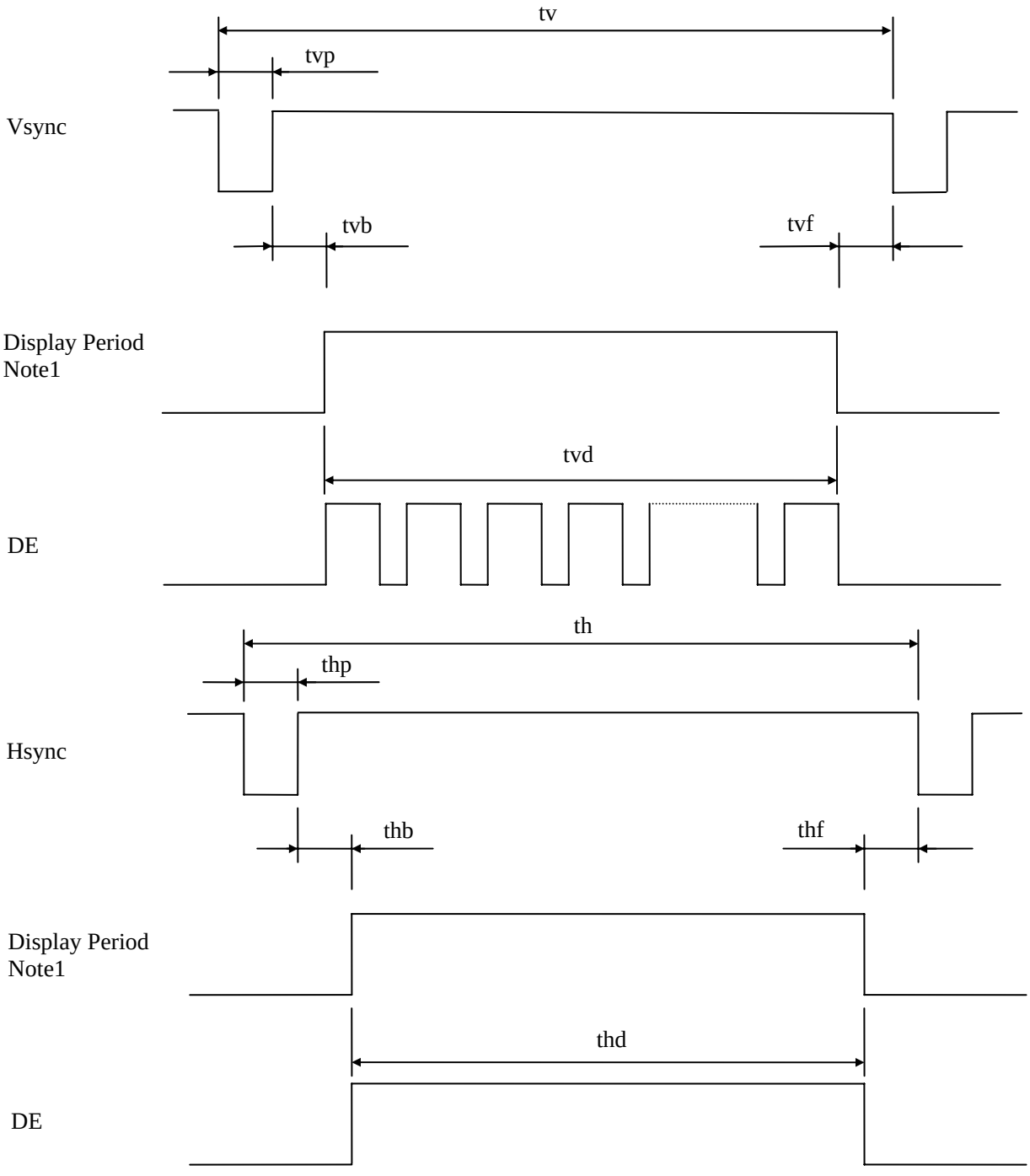


10. INTERFACE CONDITION

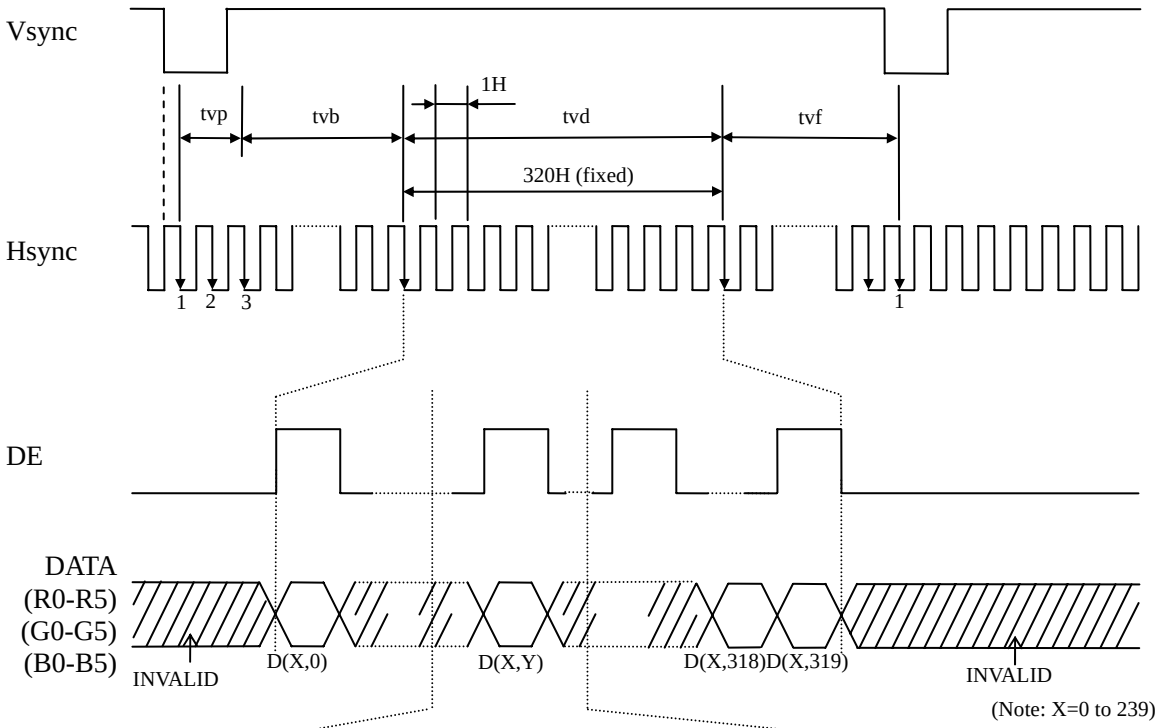
10.1 Input Signal AC Timing

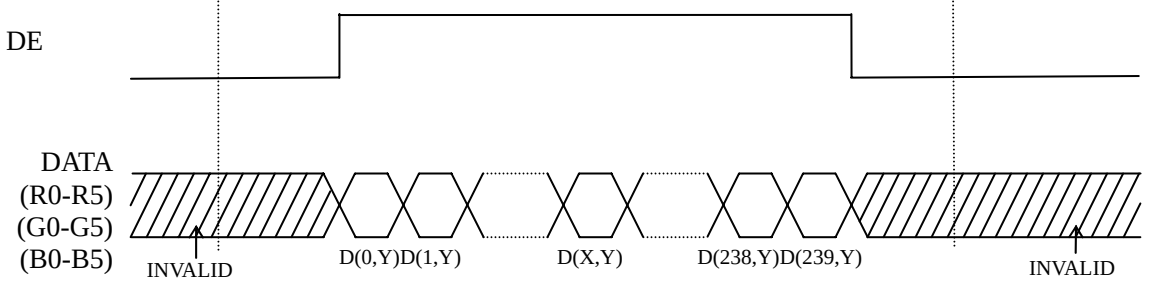
Parameter		Symbol	min.	typ.	max.	Unit	Remarks
DCK	Frequency	1/Tc	-	-	15	MHz	-
	Duty	Tch/Tc	0.4	-	0.6	-	-
	Rise, Fall	tcrf	-	-	10	ns	-
DE - DCK	Setup	Ties	2	-	-	ns	-
	Hold	Tieh	2	-	-		
	Rise, Fall	terf	-	-	10		
RI5:0 to BI5:0 - DCK	Setup	Tids	2	-	-	ns	-
	Hold	Tidh	2	-	-		
	Rise, Fall	tdrf	-	-	10		

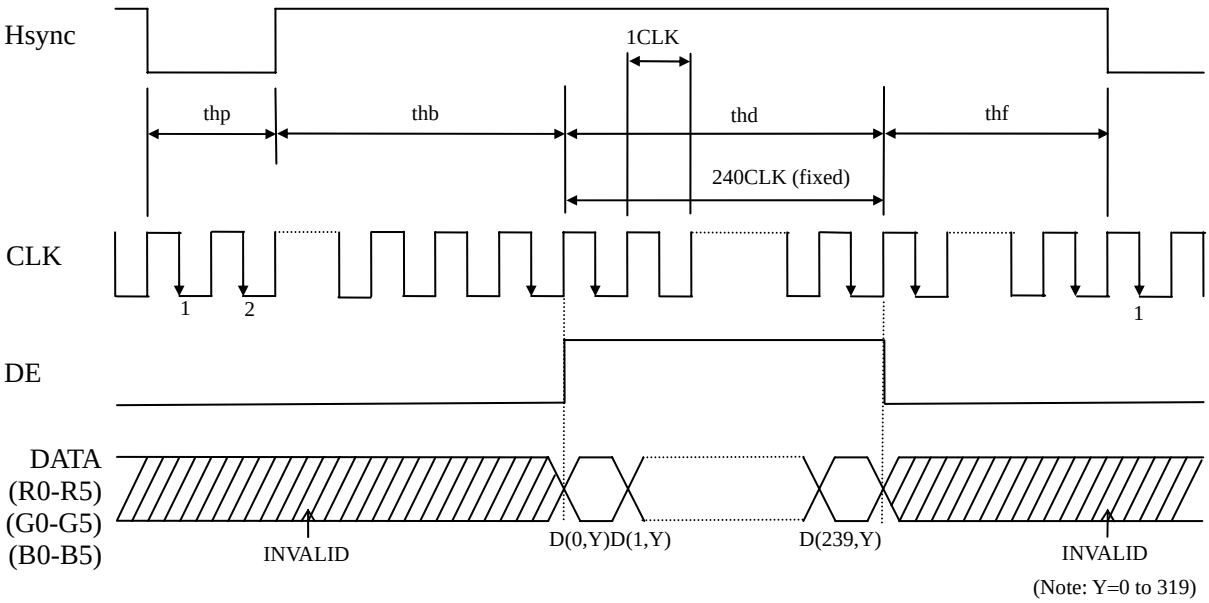




Note1: Those signals do not exist. Also, this controller does not refer Vsync and Hsync signals.


Vsync
1H
tvp
tvb
tvd
tvf
320H (fixed)
Hsync
1 2 3
1
DE
DATA
(R0-R5)
(G0-G5)
(B0-B5)
INVALID
D(X,0)
D(X,Y)
D(X,318)D(X,319)
INVALID
(Note: X=0 to 239)


DE
DATA
(R0-R5)
(G0-G5)
(B0-B5)
INVALID
D(0,Y)D(1,Y)
D(X,Y)
D(238,Y)D(239,Y)
INVALID


Hsync
1CLK
thp
thb
thd
thf
240CLK (fixed)
CLK
1 2
1
DE
DATA
(R0-R5)
(G0-G5)
(B0-B5)
INVALID
D(0,Y)D(1,Y)
D(239,Y)
INVALID
(Note: Y=0 to 319)

10.2 Normal Timing (Ex.)

(1) NL2432DR22-xxB

Parameter	Time	Unit	Pixel count	Unit	Remarks
Horizontal Pixels	240	Pixels	-	-	-
Vertical Pixels	320	Lines	-	-	-
Horizontal Frequency	19.920	kHz	-	-	-
Vertical Frequency	60.000	Hz	-	-	-
Pixel Clock	5.737	MHz	1	Pixels	-
Horizontal Total Time	50.201	μs	288	Pixels	-
Horizontal Address Time	41.834	μs	240	Pixels	-
Vertical Total Time	16.667	ms	332	Lines	-
Vertical Address Time	16.064	ms	320	Lines	-

(2) NL2432HC22-xxA and NL2432HC22-xxB

Parameter	Time	Unit	Pixel count	Unit	Remarks
Horizontal Pixels	240	Pixels	-	-	-
Vertical Pixels	320	Lines	-	-	-
Horizontal Frequency	19.440	kHz	-	-	-
Vertical Frequency	60.000	Hz	-	-	-
Pixel Clock	5.6	MHz	1	Pixels	-
Horizontal Total Time	51.440	μs	288	Pixels	-
Horizontal Address Time	44.092	μs	240	Pixels	-
Vertical Total Time	16.667	ms	324	Lines	-
Vertical Address Time	16.461	ms	320	Lines	-

10.3 Minimum Timing

Parameter	min.
H total	255DCK (50μs)
V blank	2H
H blank	8CLK

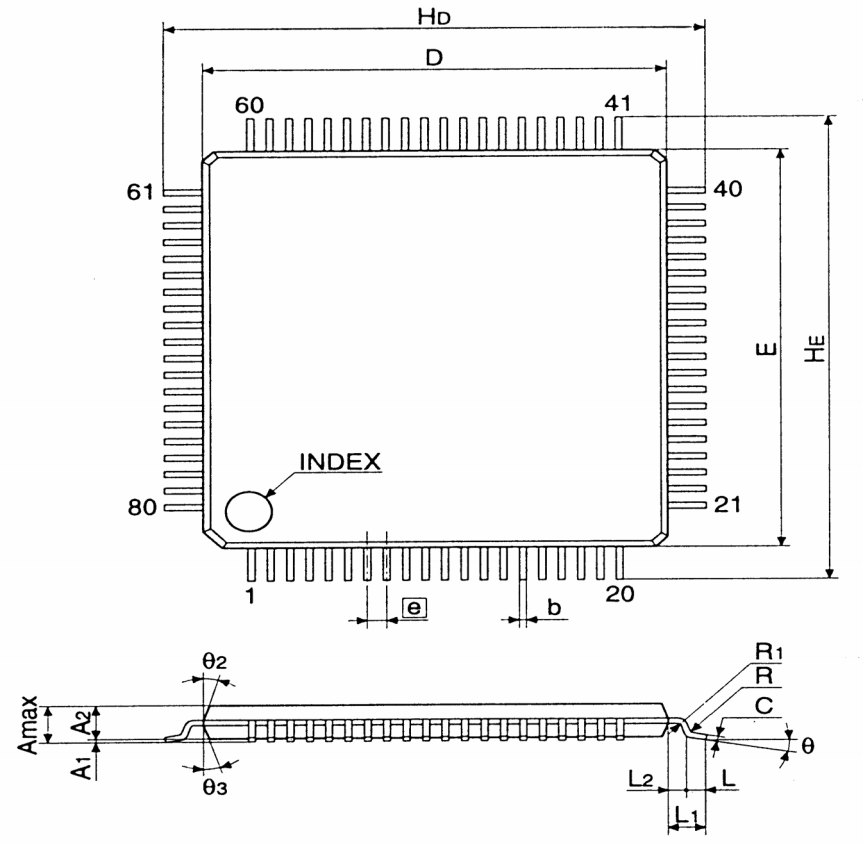
Note1: Need to set the H total time up over 50μs.

11. DISPLAY POSITION

D(0, 0)	D(1, 0)	• • •	D(X, 0)	• • •	D(238, 0)	D(239, 0)
D(0, 1)	D(1, 1)	• • •	D(X, 1)	• • •	D(238, 1)	D(239, 1)
• • •	• • •	• • •	• • •	• • •	• • •	• • •
D(0, Y)	D(1, Y)	• • •	D(X, Y)	• • •	D(238, Y)	D(239, Y)
• • •	• • •	• • •	• • •	• • •	• • •	• • •
D(0, 318)	D(1, 318)	• • •	D(X, 318)	• • •	D(238, 318)	D(239, 318)
D(0, 319)	D(1, 319)	• • •	D(X, 319)	• • •	D(238, 319)	D(239, 319)

12. OUTLINE DRAWINGS

Plastic TQFP 80pin Body size 12×12×1mm (TQFP14)

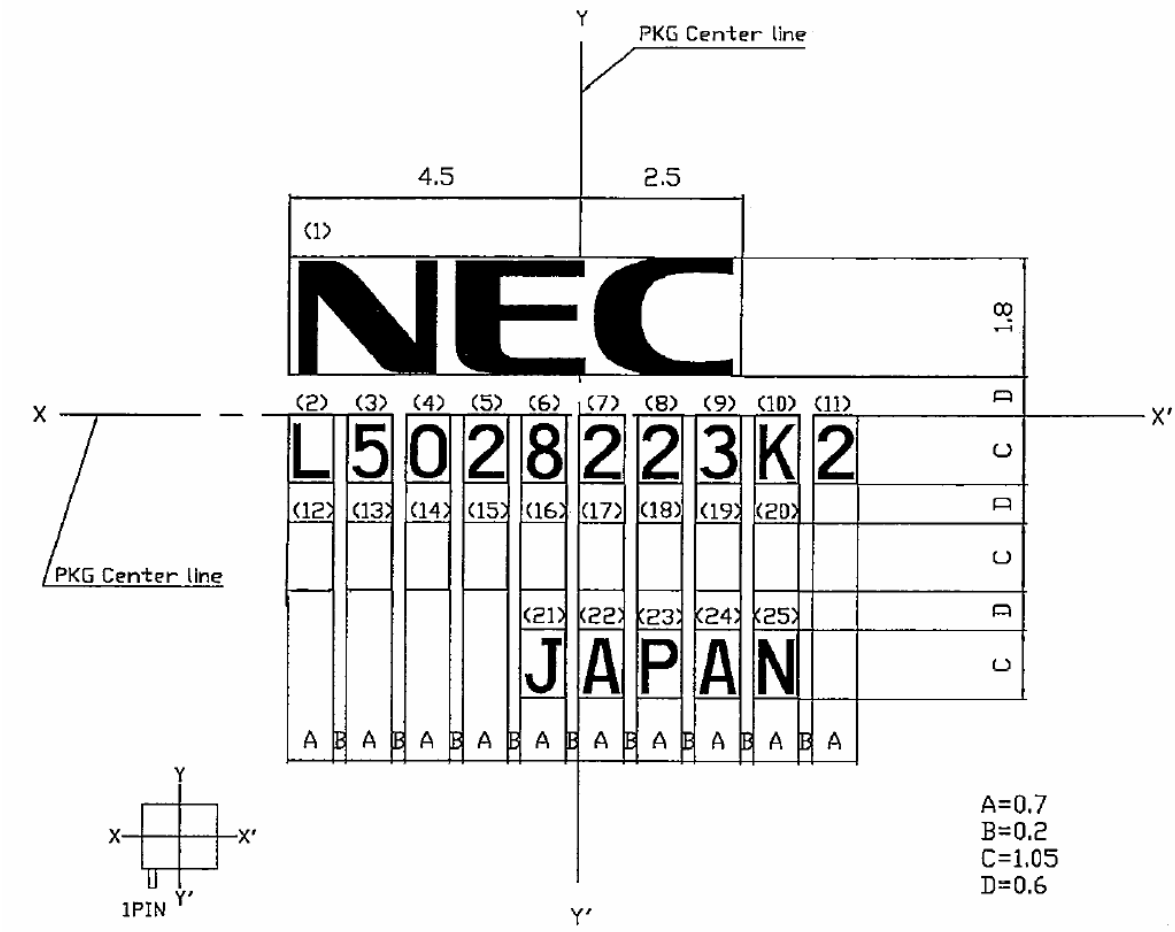


Lead type STD (TQFP14-80pin STD)

Symbol	Dimension in Millimeters			Dimension in Inches		Note1
	min.	typ.	max.	min.	typ.	max.
E	11.9	12	12.1	(0.469)	(0.472)	(0.476)
D	11.9	12	12.1	(0.469)	(0.472)	(0.476)
A	-	-	1.2	-	-	(0.047)
A_1	-	0.1	-	-	(0.004)	-
A_2	0.9	1	1.1	(0.036)	(0.039)	(0.043)
e	-	0.5	-	-	(0.020)	-
b	0.11	0.16	0.26	(0.005)	(0.006)	(0.010)
C	0.1	0.125	0.175	(0.004)	(0.005)	(0.006)
θ	0˚	-	8˚	(0˚)	-	(8˚)
L	0.3	0.5	0.7	(0.012)	(0.020)	(0.027)
L_1	-	1	-	-	(0.039)	-
L_2	-	0.5	-	-	(0.020)	-
H_E	13.6	14	14.4	(0.536)	(0.551)	(0.566)
H_D	13.6	14	14.4	(0.536)	(0.551)	(0.566)
θ_2	-	-	-	-	-	-
θ_3	-	-	-	-	-	-
R	-	-	-	-	-	-
R1	-	-	-	-	-	-

Note1: These dimensions are for reference.

Package Marking



Unit: mm

13. RELIABILITY TEST

No.	TEST ITEM	TEST CONDITION	STANDARD	CRITERIA
1	High temperature with bias	Ta=120°C, (Absolute maximum rating) V, (A certain frequency) Hz	EIAJ-ED-4701 D-101 MIL-STD-883 1005	Must meet the electrical characteristics specification.
2	Temperature/humidity with bias	Ta=85°C, RH=85%, (Absolute maximum rating) V, (A certain frequency) Hz	EIAJ-ED-4701 B-122	Must meet the electrical characteristics specification.
3	High temperature storage	Ta=150°C, 1000hours	EIAJ-ED-4701 B-111 MIL-STD-883 1008	Must meet the electrical characteristics specification.
4	Temperature cycling	-65°C ⇔ 150°C, Each 30 min., 1 cycle/1 hour (Air), 200 cycles	EIAJ-ED-4701 B-131 MIL-STD-883 1010	Must meet the electrical characteristics specification.
5	Pressure cooker	Ta=121 °C, 2.0E5 Pa, 200 hours	EIAJ-ED-4701 B-123	Must meet the electrical characteristics specification.
6	Thermal shock	0 °C ⇔ 100 °C, Each 5 min., 1cycle / 10minutes (Liquid), 10 cycles	EIAJ-ED-4701 B-141 MIL-STD-883 1011	Must meet the electrical characteristics specification.
7	Salt atmosphere	Ta=35°C, Na=5%, 48 hours	EIAJ-ED-4701 B-144 MIL-STD-883 1009	Must meet the electrical characteristics specification.
8	Soldering heat resistance	Re-flow under our recommended heat temp. profile	EIAJ-ED-4701 A-132, A-133	Must meet the electrical characteristics specification.
9	Solvent resistance	Isopropyl Alcohol 10 minutes 5 times brushing	EIAJ-ED-4701 C-121 MIL-STD-883 2015	The marking should be read.
10	ESD 1 C= 200pF, R= 0Ω, 1 time	Pin - VDD - GND 500V VSS – GND> 500V Pin + VDD - GND 350V VSS – GND 450V	-	Should not be broken.
11	ESD 2 C=100pF, R=1.5kΩ, 3 times	Pin - VDD - GND > 4,000V VSS – GND> 4,000V Pin + VDD - GND > 4,000V VSS – GND 3,500V	-	Should not be broken.
12	Latch-up	- Trigger voltage=2.0V<, Trigger current=476.7mA<	-	Latch-up should not be occurred.
		+ Trigger voltage=1.8kV<, Trigger current=555.8mA<	-	
13	Other mechanical tests	Lead fatigues, Solderability	EIAJ-ED-4701 MIL-STD-883	-

14. CONDITIONS FOR SOLDERING PRODUCT

This product is Surface Mount Device (SMD).

The resistance to soldering heat for SMD depends on the storage conditions, methods and conditions of the soldering.

Therefore this product should be assembled under the preceding recommended conditions.

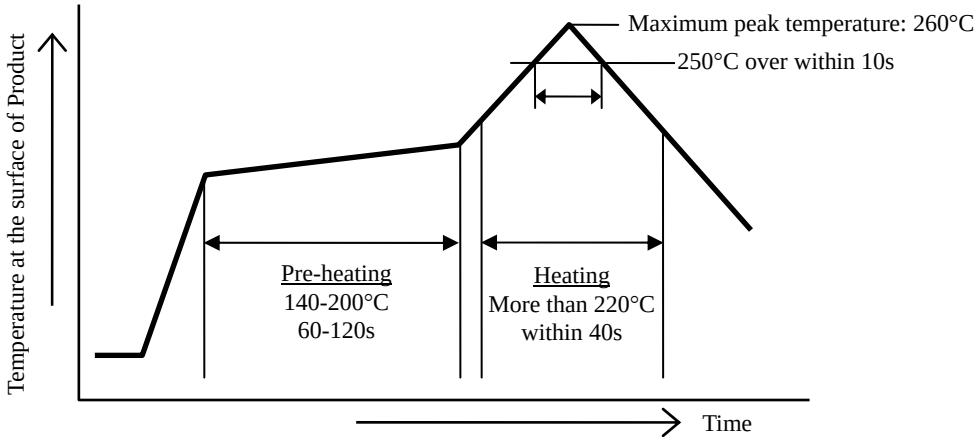
(1) Recommended Storage Conditions

- Permissible storage period before opening the dry-pack is within 12 months.
- The storage from opening the dry-pack to assembly is shown on the following chart:

Storage Conditions	Allowable period
30°C, RH= 70% or less	Within 168 hours (7 days)

Note1: This product should be stored under the preceding conditions.

(2) Reflow Temperature Profile Guideline



- The product should be assembled with the IR reflow or the Air reflow.
- The reflow should be less than two times. When the product is performed reflow two times, they should be assembled within 168hours (7 days) after opening the dry-pack.

(3) Recommended Baking Conditions

- When the product is exceeded 168hours (7 days) after opening the dry-pack, they should be baked with the following recommended conditions:

Temperature	Time
125±5°C	20hours to 36hours

- The product should be baked and assembled under the preceding storage conditions.

15. PACKING SPECIFICATION

NEC will pack products to be delivered to customer in accordance with NEC's packing specifications, and will deliver them to customer in such a condition that products will not suffer from damage during transportation. The delivery conditions are as follows.

(1) Tray

The products are packed with JEDEC tray of 322.6×135.9×7.62mm. The one tray can contain 119 products as the maximum. The trays are stacked with 5.

(2) Inner Box

The inner box contains total 500 products after sealed with a moisture barrier bag. The parts number and quantity are shown on the inner box label.

(3) Outer Box

There are two different box sizes. One size contains 3 inner boxes and another size contains 6 inner boxes. The parts number and quantity are shown on the outer box label.

There is a risk of damage to the products if the outer box is dropped from a height of 60cm or more, and therefore care should be taken in handling the box during transportation.

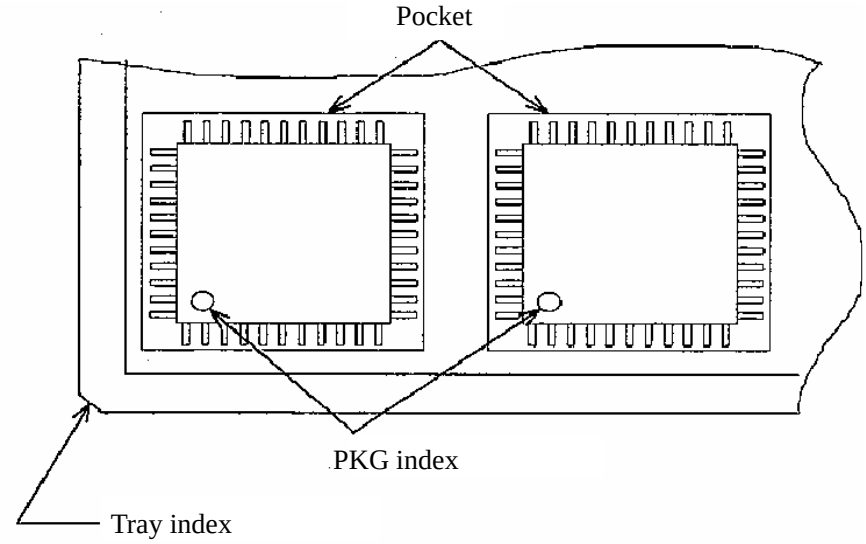
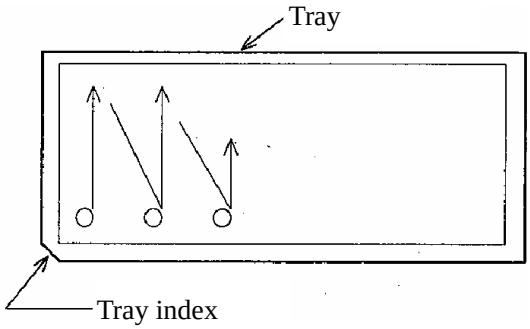
(4) Transportation

Products are to be transported by vehicle or aircraft.

Reference data

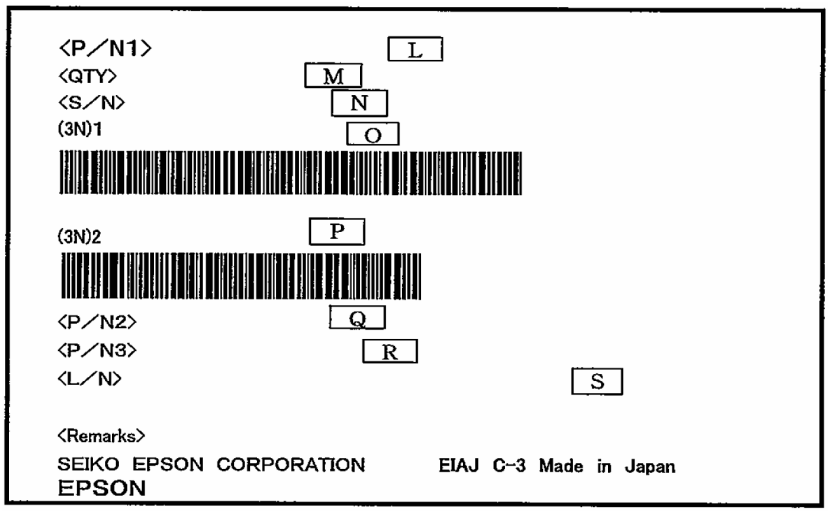
Dimensions/Weight	Inner/Outer	Type	Reference data
Box sizes	Inner box	-	325mm (W) × 161mm (D) × 44mm (H)
	Outer box	Large size	347mm (W) × 342mm (D) × 225mm (H)
		Small size	347mm (W) × 178mm (D) × 225mm (H)
Total box weight	Inner box	-	Approx. 1kg
	Outer box	Small size	Approx. 3.5kg
		Large size	Approx. 7.2kg

(5) Tray

PKG Arrangement (1)	 PKG is oriented to place PKG index at the tray index corner.
PKG Arrangement (2)	 Placing the tray index at the lower-left, PKG is arranged upward from tray index corner. PKG is arranged to the top of the row, next PKG is arranged upward from the bottom of the next right row, and so on.
Tray stack	Trays are stacked same directions and an empty tray is added to the top as a cover. If there is a tray that is not loaded standard quantities, it is stacked at the top of the loaded tray.

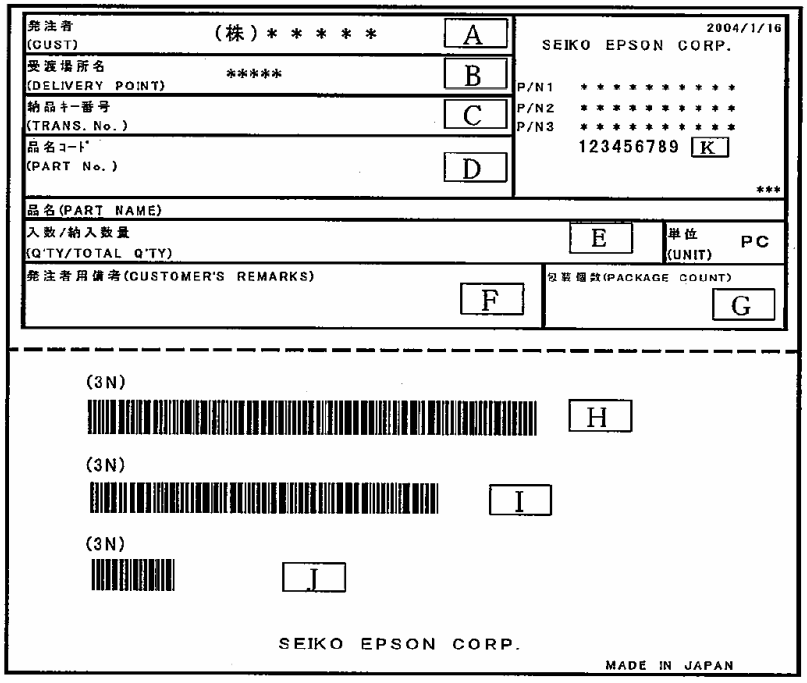
(6) Package Label

①Inner Box "C-3" Label



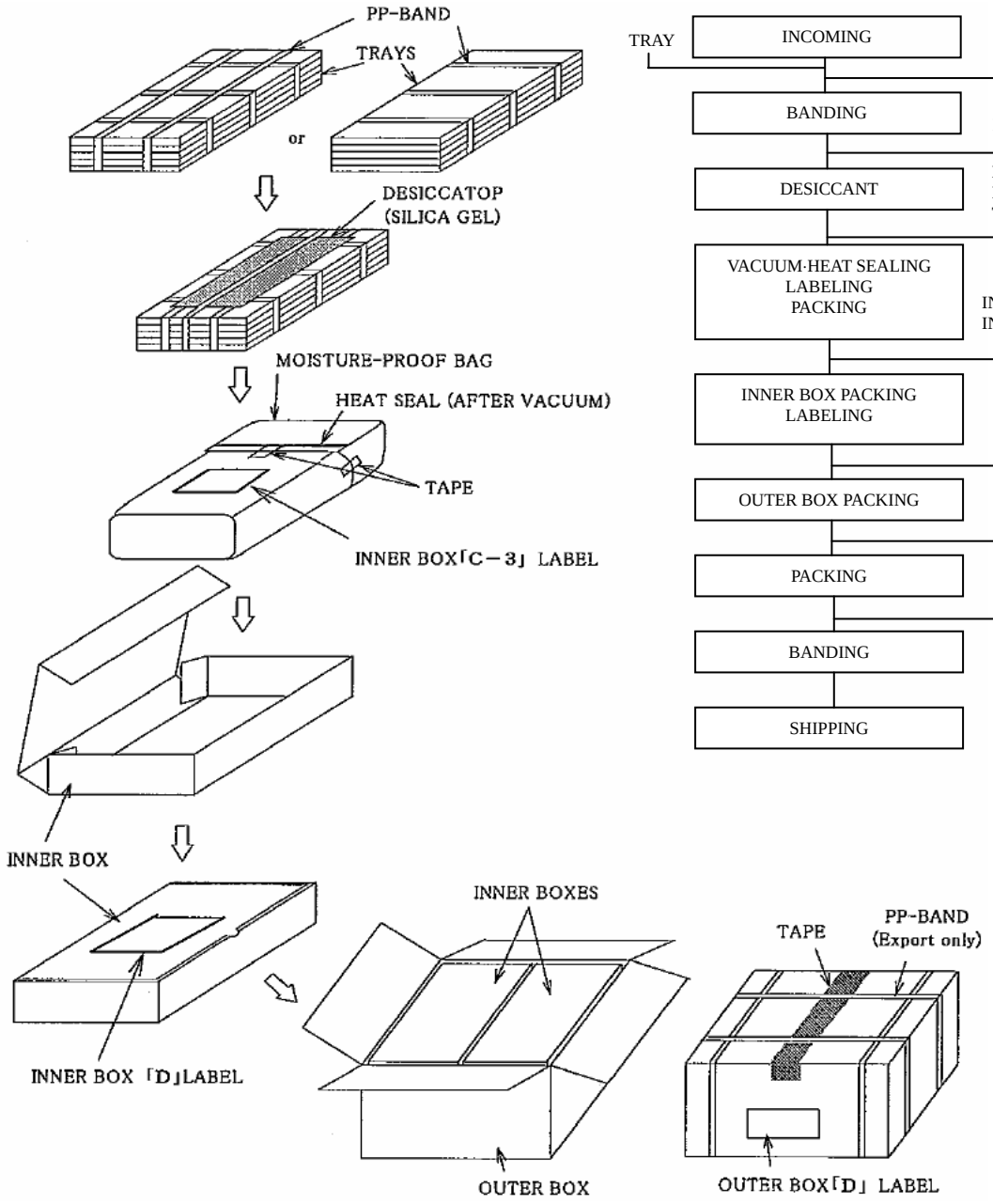
L: Part name
M: Quantity

②Inner Box "D" Label, Outer Box "D" Label



D: Part name
E: Quantity

(7) Package flow



16. PRODUCT INSPECTIONS

The following inspections are carried out on products before shipment

100% inspection

- Electrical
- Appearance

17. GENERAL CAUTIONS

(1) ESD precaution

Although all pins have the electrostatic discharge protection circuits, excessive electrostatic stress can damage ICs. Please use anti-static containers for packaging and transportation. Also, ensure that all personnel who handle ICs wear appropriate anti-static overalls and grounding wrist strap.

(2) Mounting precaution

When soldering surface mount devices using an overall soldering method such as reflow or vapor phase soldering, be sure to observe the storage conditions.

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Prepared date	Revision contents and signature	Issued date
1st edition	Feb. 1, 2005	**Revision contents** New issue **Signature of writer** *Approved by*: T. ITO *Checked by*: *Prepared by*: R. KAWASHIMA **Signature of acknowledger** *Product Design Department*: H. YAMAGUCHI *Product Design Department*: Y. HIRANO *Production Engineering Department*: A. YANO *Quality Assurance Department*: M. SHIMIZU *Product Planning Department*: I. TOKUDA	