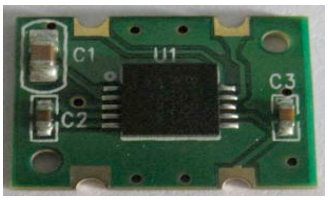
HDMM01 V1.0

Dual-axis Magnetic Sensor Module With I²C Interface



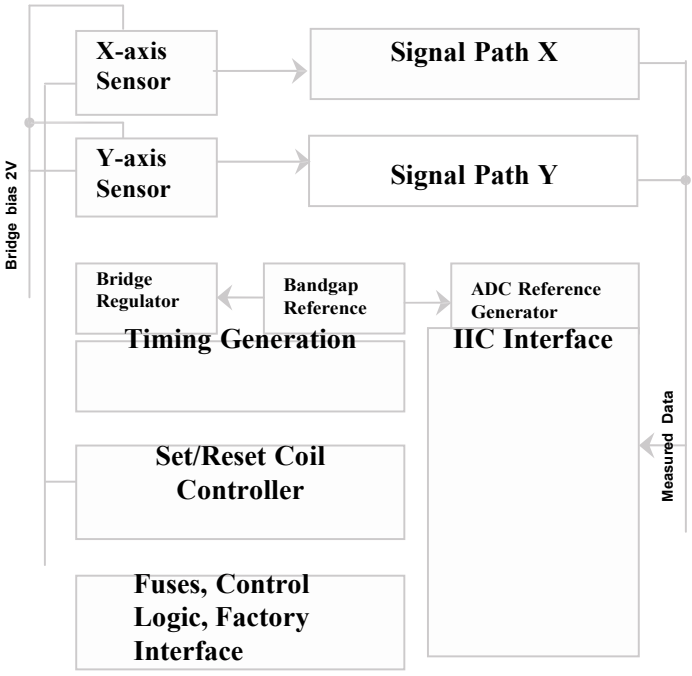
FEATURES

- **Low power consumption: typically 0.4mA@3V with 50 measurements per second**
- **Power up/down function available through I²C interface**
- **SET/RESET coil drive**

- **512counts/gauss**
- **I²C Slave, FAST (≤400 KHz) mode**
- **1.8V compatible IO**
- **2.7V~5.25V wide power supply operation supported**
- **RoHS compliant**

APPLICATIONS :

Electronic Compass
GPS Navigation
Position Sensing
Vehicle Detection
Magnetometry



FUNCTIONAL BLOCK DIAGRAM

DESCRIPTIONS :

The HDMM01 is a dual-axis magnetic sensor module, it is a complete sensing system with on-chip signal processing and integrated I²C bus, allowing The module to be connected directly to a microprocessor eliminating the need for A/D converters or timing resources. It can measure magnetic field with a full range of ±5 gausses and a sensitivity of 512counts/gauss @3.0 V at 25°C.

The HDMM01 is available in operating temperature ranges of -40°C to +85°C.

The HDMM01 provides an I²C digital output with 400 KHz, fast mode operation.

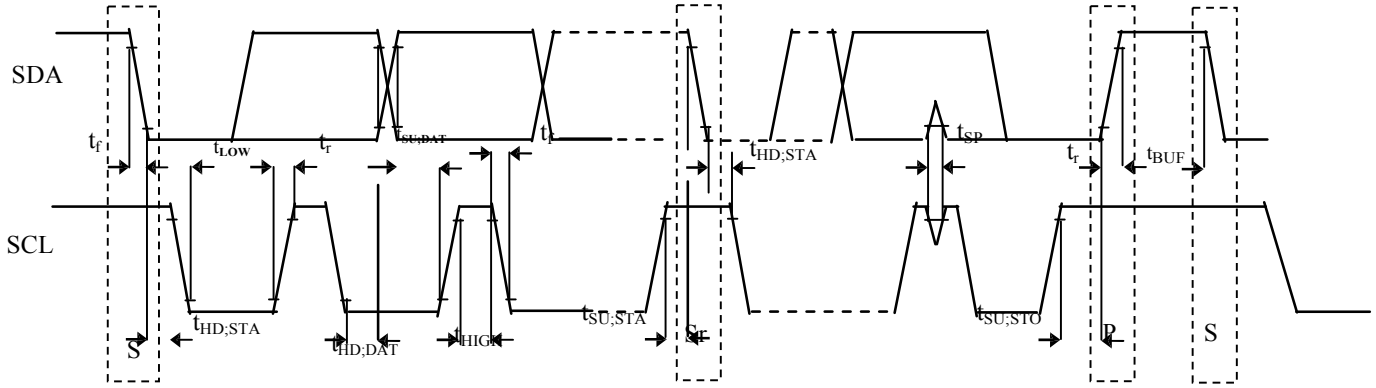
SPECIFICATION: (Measurements @° 25C, unless otherwise noted; V_{DA} = V_{DD}= 3.0V unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Field Range (Each Axis)	Total applied field	-2		+2	gauss
Supply Voltage	V_{DA}	2.7	3.0	5.25	V
	V_{DD} (I^2C interface)	1.62	3.0	5.25	V
Supply Current	50 measurements/second		0.40		mA
Power Down Current				1.0	µA
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C
Linearity Error (Best fit straight line)	±1 gauss		0.1		%FS
	±2gauss		0.5		%FS
Hysteresis	3 sweeps across ±2 gauss		0.05		%FS
Repeatability Error	3 sweeps across ±2 gauss		0.1		%FS
Alignment Error			±1.0	±3.0	degrees
Transverse Sensitivity			±2.0	±5.0	%
Noise Density	1~25Hz, RMS		600		µgauss
Accuracy[1]			±2	±5	deg
Bandwidth			25		Hz
Sensitivity		-10		+10	%
		461	512	563	counts/gauss
Sensitivity Change Over Temperature	Based on 512counts/gauss		±1100		ppm/°C
Null Field Output		-0.2		+0.2	gauss
			2048		counts
Null Field Output Change Over Temperature	Without Set/Reset Delta from 25°C		+0.4		mgauss/°C
	With Set/Reset [2] Delta from 25°C		1/50		Ratio to the result without set/reset
Disturbing Field	Sensitivity start to degrade, use Set/Reset pulse to restore	5.5			gauss
Maximum Exposed Field				10000	gauss

Note: [1]: Accuracy is dependent on system design, calibration and compensation algorithms used. The specification is based upon using the HDMM01 evaluation board and associate software.
[2]: By design.

I²C INTERFACE I/O CHARACTERISTICS (V_{DD}=3.0V)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic Input Low Level	V_{IL}		-0.5		0.3* V_{DD}	V
Logic Input High Level	V_{IH}		0.7*V_{DD}		V_{DD}	V
Hysteresis of Schmitt input	V_{hys}		0.2			V
Logic Output Low Level	V_{OL}				0.4	V
Input Leakage Current	I_i	0.1V_{DD}<V_{in}<0.9V_{DD}		-10	10	μa
SCL Clock Frequency	f_{SCL}			0	400	kHz
START Hold Time	$t_{HD;STA}$		0.6			μS
START Setup Time	$t_{SU;STA}$		0.6			μS
LOW period of SCL	t_{LOW}		1.3			μS
HIGH period of SCL	t_{HIGH}		0.6			μS
Data Hold Time	$t_{HD;DAT}$		0		0.9	μS
Data Setup Time	$t_{SU;DAT}$		0.1			μS
Rise Time	t_r	From V_{IL} to V_{IH}			0.3	μS
Fall Time	t_f	From V_{IH} to V_{IL}			0.3	μS
Bus Free Time Between STOP and START	t_{BUF}		1.3			μS
STOP Setup Time	$t_{SU;STO}$		0.6			μS



Timing Definition

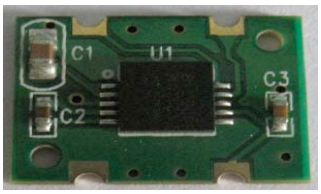
HDMM01 V1.0

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{DD}) .....-0.5 to +7.0V

Storage Temperature .....-55 ° Cto+125 ° C Maximum Exposed Field .....10000 gauss

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to The module. This is a stress rating only; the functional operation of The module at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



Pin Description: LGA-10 (3x3x0.7mm) Package

Pin	Name	Description	I/O
1	GND	Connect to Ground	P
2	V_{DD}	Power Supply for I C bus	P
3	SDA	Serial Data Line for I^2C bus	I/O
4	SCL	Serial Clock Line for I^2C bus	I

THEORY:

The anisotropic magnetoresistive (AMR) sensors are special resistors made of permalloy thin film deposited on a silicon wafer. During manufacturing, a strong magnetic field is applied to the film to orient its magnetic domains in the same direction, establishing a magnetization vector. Subsequently, an external magnetic field applied perpendicularly to the sides of the film causes the magnetization to rotate and change angle. This in turn causes the film's resistance to vary. The HDMM01 AMR sensor is included in a Wheatstone bridge, so that the change in resistance is detected as a change in differential voltage and the strength of the applied magnetic field may be inferred.

However, the influence of a strong magnetic field (more than 5.5 gausses) along the magnetization axis could upset, or flip, the polarity of the film, thus changing the sensor characteristics. A strong restoring magnetic field must be applied magnetically to restore, or set, the sensor characteristics. The HDMM01 magnetic sensor has an on-chip magnetically coupled coil: a SET/RESET coil pulsed with a high current, to provide the restoring magnetic field.

PIN DESCRIPTIONS:

GND – This is the ground pin for the magnetic sensor.

SDA – This pin is the I^2C serial data line, and operates in FAST (400 KHz) mode.

SCL– This pin is the I^2C serial clock line, and operates in FAST (400 KHz) mode.

V_{DD} – This is the power supply input for the I^2C bus, and is 1.8V compatible can be 1.62V to 5.25V.

POWER CONSUMPTION

The HDMM01 magnetic sensor consumes 0.40mA (typical) current at 3V with 50 measurements/second, but the current is proportional to the number of measurements carried out, for example, if only 20 measurements/second are performed, the current will be 0.40*20/50=0.16mA.

I^2C INTERFACE DESCRIPTION

A slave mode I^2C circuit has been implemented into the HDMM01 magnetic sensor as a standard interface for customer applications. The A/D converter and MCU functionality have been added to the HDMM01 sensor, thereby increasing ease-of-use, and lowering power consumption, footprint and total solution cost.

The I^2C (or Inter IC bus) is an industry standard bi-directional two-wire interface bus. A master I^2C device can operate READ/WRITE controls to an unlimited number of devices by device addressing. The HDMM01 magnetic sensor operates only in a slave mode, i.e. only responding to calls by a master device.

I^2C BUS CHARACTERISTICS

The two wires in I^2C bus are called SDA (serial data line) and SCL (serial clock line). In order for a data transfer to start, the bus has to be free, which is defined by both wires in a HIGH output state. Due to the open-drain/pull-up resistor structure and wired Boolean “AND” operation, any device on the bus can pull lines low and overwrite a HIGH signal. The data on the SDA line has to be stable during the HIGH period of the SCL line. In other words, valid data can only change when the SCL line is LOW.

Note: Rp selection guide: 4.7Kohm for a short I^2C bus length (less than 4inches), and 10Kohm for less than 2inches I^2C bus.

DATA TRANSFER

A data transfer is started with a "START" condition and ended with a "STOP" condition. A "START" condition is defined by a HIGH to LOW transition on the SDA line while SCL line is HIGH. A "STOP" condition is defined by a LOW to HIGH transition on the SDA line while SCL line is HIGH. All data transfer in I^2C system is 8-bits long. Each byte has to be followed by an acknowledge bit. Each data transfer involves a total of 9 clock cycles. Data is transferred starting with the most significant bit (MSB). After a "START" condition, master device calls specific slave device, in our case, a HDMM01 device with a 7-bit device address "**[0110xx0]**". To avoid potential address conflict, either by ICs from other manufacturers or by other HDMM01 device on the same bus, a fix **addresses** can be pre-programmed into HDMM01 module by the factory.
Following the 7-bit address, the 8th bit determines the direction of data transfer: [1] for READ and [0] for WRITE. After being addressed, available HDMM01 module being called should respond by an "Acknowledge" signal, which is pulling SDA line LOW.
In order to read sensor signal, master device should operate a WRITE action with a code of [xxxxxxx1] into HDMM01 module 8-bit internal register. Note that this action also serves as a "wake-up" call.

Bit	Name	Function
0	TM (Take Measurements)	Initiate measurement sequence for "1", this bit will be cleared by circuit outside of I2C core after measurement and A/D are finished. More specifically, it will be automatically cleared by TM_DONE signal after the action is finished.
1	SET (Set Coil)	Writing "1" will set the MR by passing a large current through Set/Reset Coil. It will be automatically cleared by SETRESET_DONE signal after the action is finished.
2	RESET (Reset Coil)	Writing "1" will reset the MR by passing a large current through Set/Reset Coil in a reversed direction. It will be automatically cleared by SETRESET_DONE signal after the action is finished.

HDMM01 ADDRESS=60H

After writing code of [xxxxxxx1] into control register and a zero memory address pointer is also written, and if a "READ" command is received, the HDMM01 device being called transfers 8-bit data to I^2C bus. If "Acknowledge" by master device is received, HDMM01 module will continue to transfer next byte. The same procedure repeats until 5 byte of data are transferred to master device. Those 5 bytes of data are defined as following:

1. Internal register
2. MSB X-axis
3. LSB X-axis
4. MSB Y-axis
5. LSB Y-axis

Even though each axis consists two bytes, which are 16bits of data, the actual resolution is limited 12bits. Unused MSB should be simply filled by "0"s.

POWER DOWN MODE

HDMM01 MR sensor will enter power down mode automatically after data acquisition is finished. A data acquisition is initiated when master writes in to the control register a code of [xxxxxxx1].

EXAMPLE OF TAKE MEASUREMENT

First cycle: START followed by a calling to slave address [0110xx0] to WRITE (8th SCL, SDA keep low). [xx] is determined by factory programming, total 4 different addresses are available.

Second cycle: After a acknowledge signal is received by master device (HDMM01 module pulls SDA line low
during 9th SCL pulse), master device sends "[00000000]" as the target address to be written into. HDMM01 module should acknowledge at the end (9th SCL pulse). Note: since HDMM01 module has only one internal register that can be written into, so user should always use "[00000000]" as the write address.

Third cycle: Master device writes to internal HDMM01 device memory the code "[00000001]" as a wake-up call to initiate a data acquisition. HDMM01 device should send acknowledge.

A STOP command indicates the end of write operation.

A minimal 5ms wait period should be given to HDMM01 module to finish a data acquisition and return a valid output. The TM bit (Take Measurement bit in control register) will be automatically reset to "0" after data from A/D converter is ready. The transition from "1" to "0" of TM bit also indicates "data ready". The module will go into sleep mode afterwards. Analog
circuit will be powered off, but I^2C portion will continue be active and data will not be lost.

Fourth cycle: Master device sends a START command followed by calling HDMM01 module address with a WRITE (8th SCL, SDA keep low). A

acknowledge should be send by HDMM01 module at the end.

Fifth cycle: Master device writes to HDMM01 module a "[00000000]" as the starting address to read from which internal memory. Since "[00000000]" is the address of internal control register, reading from this address can serve as a verification operation to confirm the write command has been successful. Note: the starting address in principle can be any of the 5 addresses. For example, user can start read from address [0000001], which is X channel MSB.

Sixth cycle: Master device calls HDMM01 module address with a READ (8th SCL cycle SDA line high). HDMM01 module should acknowledge at the end.

Seventh cycle: Master device cycles SCL line, first addressed memory data appears on SDA line. If in step 7, "[00000000]" was sent, internal control register data should appear (in the following steps, this case is assumed). Master device should send acknowledge at the end.

Eighth cycle: Master device continues to cycle the SCL line, next byte of internal memory should appear on SDA line (MSB of X channel). The internal memory address pointer automatically moves to the next byte. Master acknowledges.

Ninth cycle: LSB of X channel.

Tenth cycle: MSB of Y channel.

Eleventh cycle: LSB of Y channel.

Master ends communications by NOT sending 'Acknowledge' and also followed by a 'STOP' command.

EXAMPLE OF SET/RESET COIL

First cycle: START followed by a calling to slave address [0110xx0] to WRITE (8th SCL, SDA keep low). [xx] is determined by factory programming, total 4 different addresses are available.

Second cycle: After a acknowledge signal is received by master device (HDMM01 module pulls SDA line low during 9th SCL pulse), master device sends "[00000000]" as the target address. HDMM01 module should acknowledge at the end (9th SCL pulse). Note: since HDMM01 module has only one internal register can be written into, user should always use "[00000000]" as the write address.

Third cycle: Master device writes to internal HDMM01 module memory the code "[00000010]" as a wake-up call to initiate a SET action, or the code "[00000100]" to initiate a RESET action. Note that in low voltage mode, master need to issue SET command if the previous command is RESET, and issue a RESET command if the previous command is SET. In the case of a cold start (device just powered on), master should only issue SET command. The wait time from power on to SET command should be a minimal 10ms. HDMM01 module should send acknowledge. Note that SET and RESET bits should not be set to "1" at the same time. In case of that happens, The module will only do a SET action. A STOP command indicates the end of write operation.

A minimal of 50us wait should be given to HDMM01 module to finish SET/RESET action before taking a measurement. The SET or RESET bit will be automatically reset to "0" after SET/RESET is done. And The module will go into sleep mode afterwards.

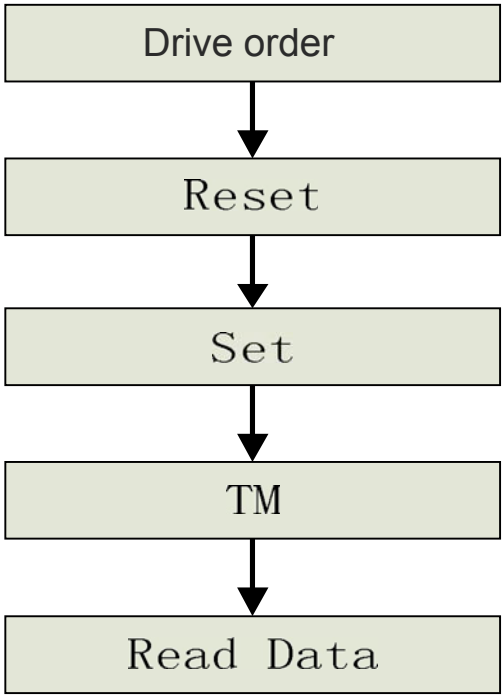
In low voltage operation mode, SET/RESET commands have to alternate. In other words, one can not do a SET following a SET, same for RESET. The first command after initial power up should be SET. If RESET command is attempted as the first command, it will be ignored Between SET and RESET, a minimal 5ms is needed for the voltage on capacitor to settle.

Note 1: at power-on, internal register and memory address pointer are reset to "0".

Note 2: In low voltage operation mode, device requires an additional capacitor to be able to do SET/RESET at lower supply voltage.

HDMM01Drive process

Flowchart：



PACKAGE DRAWING