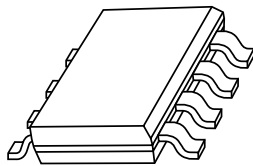


# DATA SHEET



## **PHC2300**

Complementary enhancement  
mode MOS transistors

Product specification  
Supersedes data of 1997 Oct 24

2002 Jul 09

# Complementary enhancement mode MOS transistors

PHC2300

**FEATURES**

- High-speed switching
- No secondary breakdown.

**APPLICATIONS**

- Universal line interface in telephone sets
- Relay, high-speed and line transformer drivers.

**DESCRIPTION**

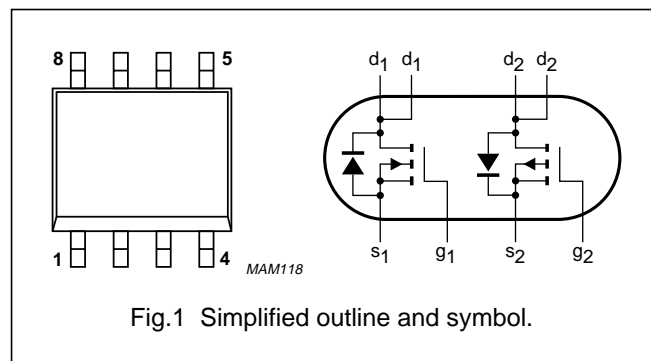
One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

**PINNING - SOT96-1 (SO8)**

PIN	SYMBOL	DESCRIPTION
1	s <sub>1</sub>	source 1
2	g <sub>1</sub>	gate 1
3	s <sub>2</sub>	source 2
4	g <sub>2</sub>	gate 2
5	d <sub>2</sub>	drain 2
6	d <sub>2</sub>	drain 2
7	d <sub>1</sub>	drain 1
8	d <sub>1</sub>	drain 1

**CAUTION**

The device is supplied in an antistatic package.  
The gate-source input must be protected against static discharge during transport or handling.



**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per FET</b>					
V <sub>DS</sub>	drain-source voltage (DC) N-channel P-channel		–	300 –300	V V
V <sub>GS</sub>	gate-source voltage (DC)		–	±20	V
V <sub>GSth</sub>	gate-source threshold voltage N-channel P-channel	V <sub>DS</sub> = V <sub>GS</sub> ; I <sub>D</sub> = 1 mA V <sub>DS</sub> = V <sub>GS</sub> ; I <sub>D</sub> = –1 mA	0.8 –0.8	2 –2	V V
I <sub>D</sub>	drain current (DC) N-channel P-channel	T <sub>s</sub> = 80 °C	– –	340 –235	mA mA
R <sub>DSon</sub>	drain-source on-state resistance N-channel P-channel	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 170 mA V <sub>GS</sub> = –10 V; I <sub>D</sub> = –115 mA	– –	6 17	Ω Ω
P <sub>tot</sub>	total power dissipation	T <sub>s</sub> = 80 °C	–	1.6	W

# Complementary enhancement mode MOS transistors

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

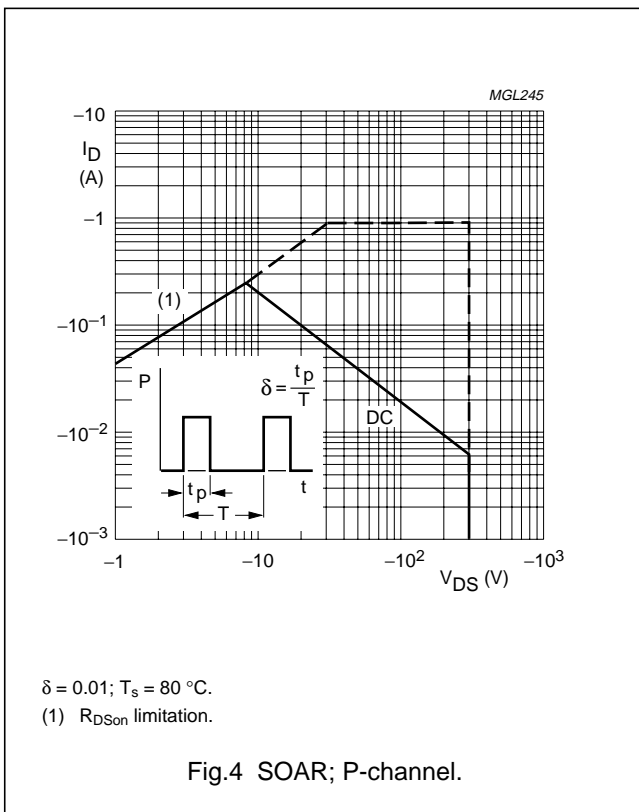
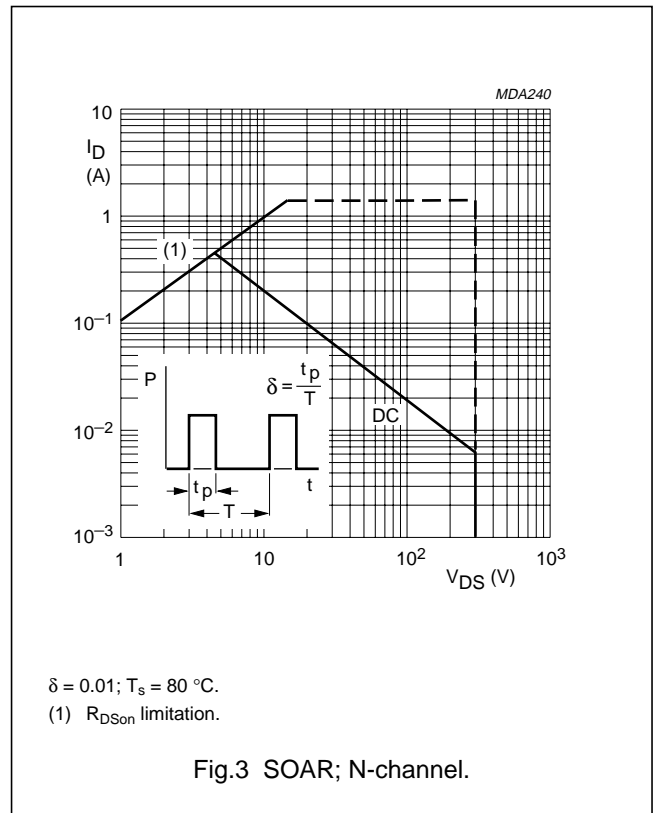
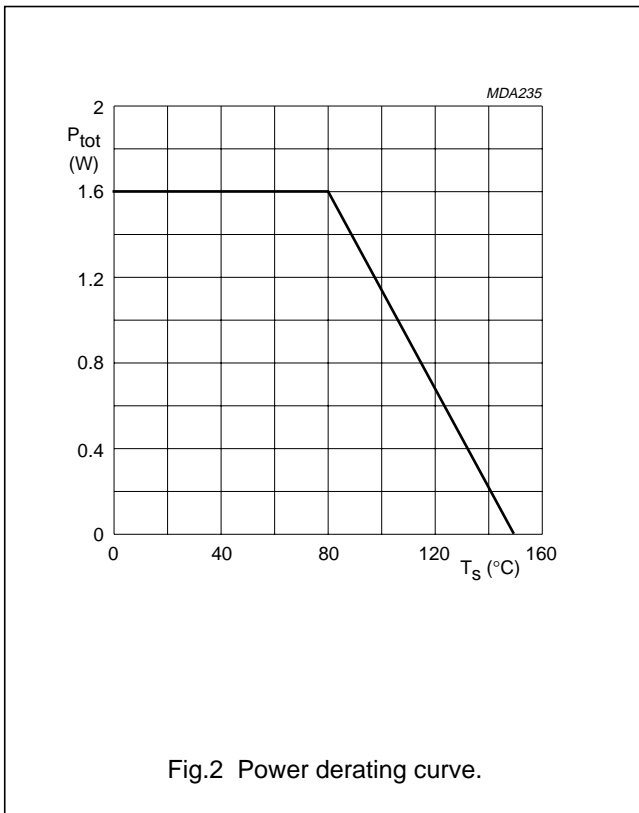
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per FET</b>					
V <sub>DS</sub>	drain-source voltage (DC)				
	N-channel		–	300	V
	P-channel		–	–300	V
V <sub>GS</sub>	gate-source voltage (DC)		–	±20	V
I <sub>D</sub>	drain current (DC)	T <sub>s</sub> = 80 °C; note 1			
	N-channel		–	340	mA
	P-channel		–	–235	mA
I <sub>DM</sub>	peak drain current	note 2			
	N-channel		–	1.4	A
	P-channel		–	–0.9	A
P <sub>tot</sub>	total power dissipation	T <sub>s</sub> = 80 °C; note 3	–	1.6	W
		T <sub>amb</sub> = 25 °C; note 4	–	1.8	W
		T <sub>amb</sub> = 25 °C; note 5	–	0.9	W
		T <sub>amb</sub> = 25 °C; note 6	–	1.2	W
T <sub>stg</sub>	storage temperature		–55	+150	°C
T <sub>j</sub>	operating junction temperature		–55	+150	°C

### Notes

1. T<sub>s</sub> is the temperature at the soldering point of the drain leads.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor (both devices may thus be loaded up to 1.6 W at the same time).
4. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an R<sub>th a-tp</sub> (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an R<sub>th a-tp</sub> (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Value based on a printed-circuit board with an R<sub>th a-tp</sub> (ambient to tie-point) of 90 K/W.

Complementary enhancement mode  
MOS transistors

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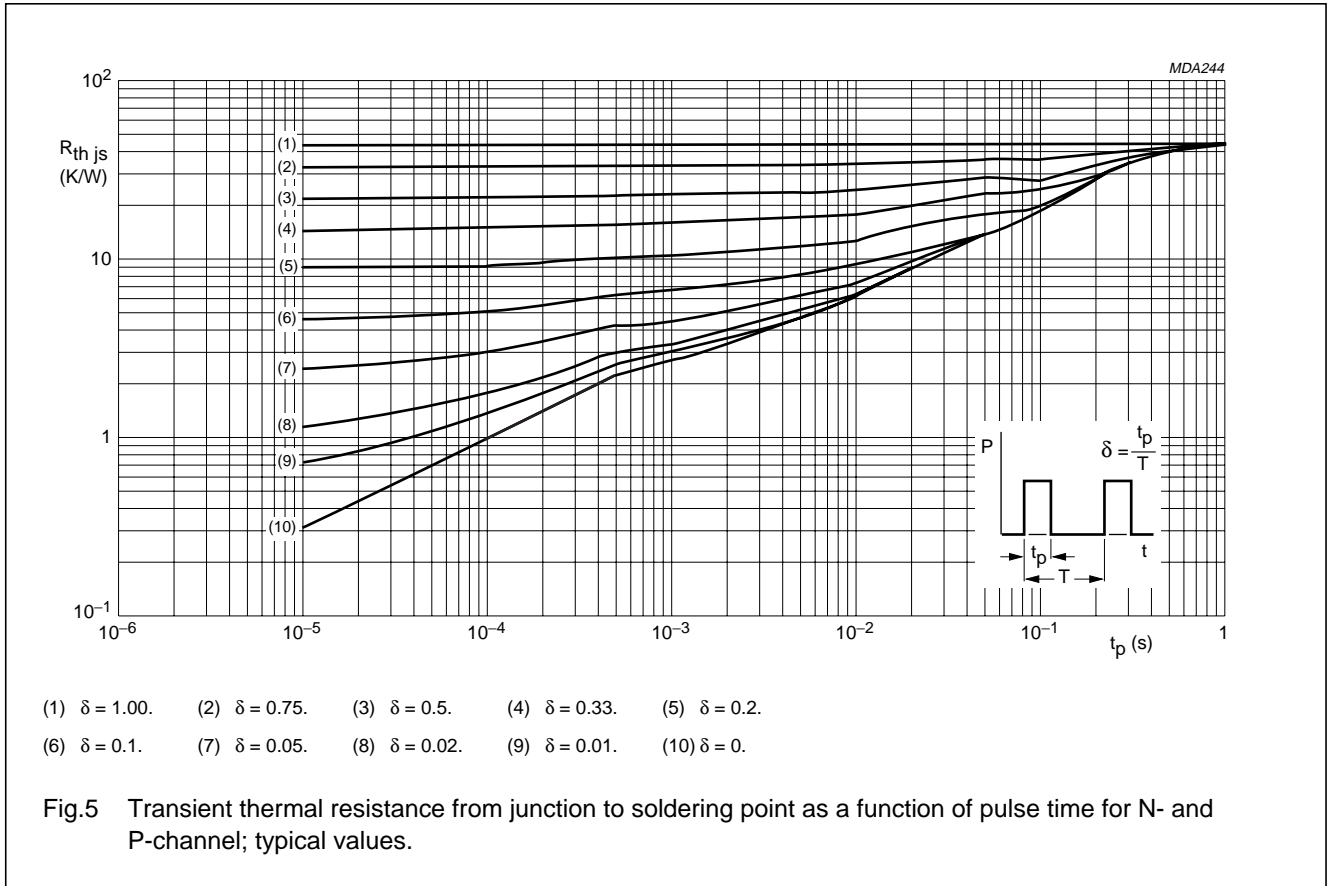


Complementary enhancement mode  
MOS transistors

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	43	K/W



CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per FET</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage					
	N-channel	$V_{GS} = 0; I_D = 10\ \mu\text{A}$	300	–	–	V
	P-channel	$V_{GS} = 0; I_D = -10\ \mu\text{A}$	-300	–	–	V
$V_{GSth}$	gate-source threshold voltage					
	N-channel	$V_{GS} = V_{DS}; I_D = 1\ \text{mA}$	0.8	–	2	V
	P-channel	$V_{GS} = V_{DS}; I_D = -1\ \text{mA}$	-0.8	–	-2	V
$I_{DSS}$	drain-source leakage current					
	N-channel	$V_{GS} = 0; V_{DS} = 240\ \text{V}$	–	–	100	nA
	P-channel	$V_{GS} = 0; V_{DS} = -240\ \text{V}$	–	–	-100	nA

## Complementary enhancement mode MOS transistors

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = ±20 V; V <sub>DS</sub> = 0	–	–	±100	nA	
	N-channel						
	P-channel				±100	nA	
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 170 mA V <sub>GS</sub> = –10 V; I <sub>D</sub> = –115 mA	–	–	6	Ω	
	N-channel						
	P-channel				17	Ω	
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0; V <sub>DS</sub> = 50 V; f = 1 MHz V <sub>GS</sub> = 0; V <sub>DS</sub> = –50 V; f = 1 MHz	–	102	–	pF	
	N-channel						
	P-channel				45	pF	
C <sub>oss</sub>	output capacitance	V <sub>GS</sub> = 0; V <sub>DS</sub> = 50 V; f = 1 MHz V <sub>GS</sub> = 0; V <sub>DS</sub> = –50 V; f = 1 MHz	–	15	–	pF	
	N-channel						
	P-channel				15	pF	
C <sub>rss</sub>	reverse transfer capacitance	V <sub>GS</sub> = 0; V <sub>DS</sub> = 50 V; f = 1 MHz V <sub>GS</sub> = 0; V <sub>DS</sub> = –50 V; f = 1 MHz	–	7.3	–	pF	
	N-channel						
	P-channel				3	pF	
Q <sub>G</sub>	total gate charge	V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 50 V; I <sub>D</sub> = 170 mA V <sub>GS</sub> = –10 V; V <sub>DS</sub> = –50 V; I <sub>D</sub> = –115 mA	–	6240	–	pC	
	N-channel						
	P-channel				2137	pC	
Q <sub>GS</sub>	gate-source charge	V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 50 V; I <sub>D</sub> = 170 mA V <sub>GS</sub> = –10 V; V <sub>DS</sub> = –50 V; I <sub>D</sub> = –115 mA	–	226	–	pC	
	N-channel						
	P-channel				68	pC	
Q <sub>GD</sub>	gate-drain charge	V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 50 V; I <sub>D</sub> = 170 mA V <sub>GS</sub> = –10 V; V <sub>DS</sub> = –50 V; I <sub>D</sub> = –115 mA	–	1385	–	pC	
	N-channel						
	P-channel				674	pC	
<b>Switching times</b>							
t <sub>on</sub>	turn-on time	V <sub>GS</sub> = 0 to 10 V; V <sub>DD</sub> = 50 V; I <sub>D</sub> = 170 mA V <sub>GS</sub> = 0 to –10 V; V <sub>DD</sub> = –50 V; I <sub>D</sub> = –115 mA	–	7	12	ns	
	N-channel						
	P-channel				4	10	ns
t <sub>off</sub>	turn-off time	V <sub>GS</sub> = 10 to 0 V; V <sub>DD</sub> = 50 V; I <sub>D</sub> = 170 mA V <sub>GS</sub> = –10 to 0 V; V <sub>DD</sub> = –50 V; I <sub>D</sub> = –115 mA	–	53	65	ns	
	N-channel						
	P-channel				25	35	ns

Complementary enhancement mode  
MOS transistors

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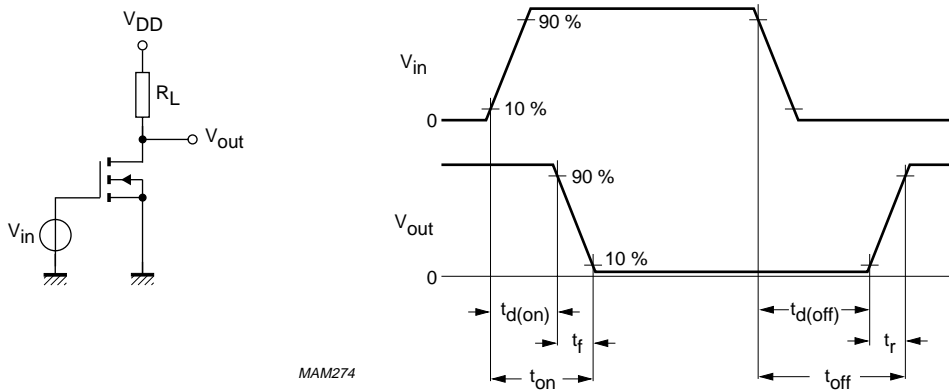


Fig.6 Switching times test circuit with input and output waveforms; N-channel.

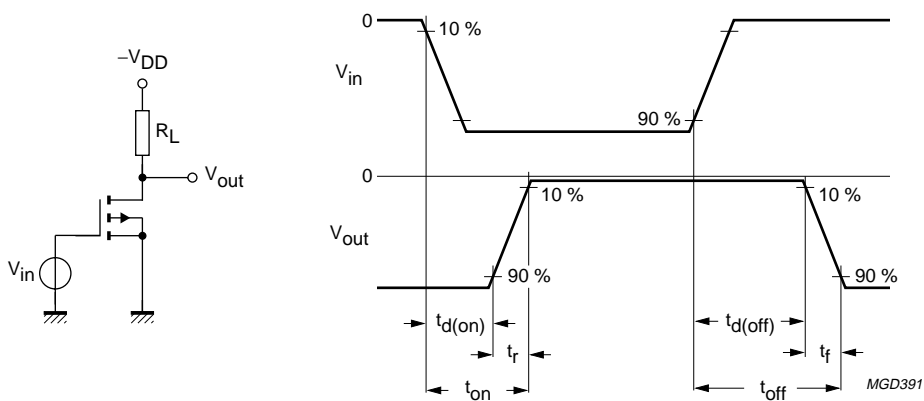
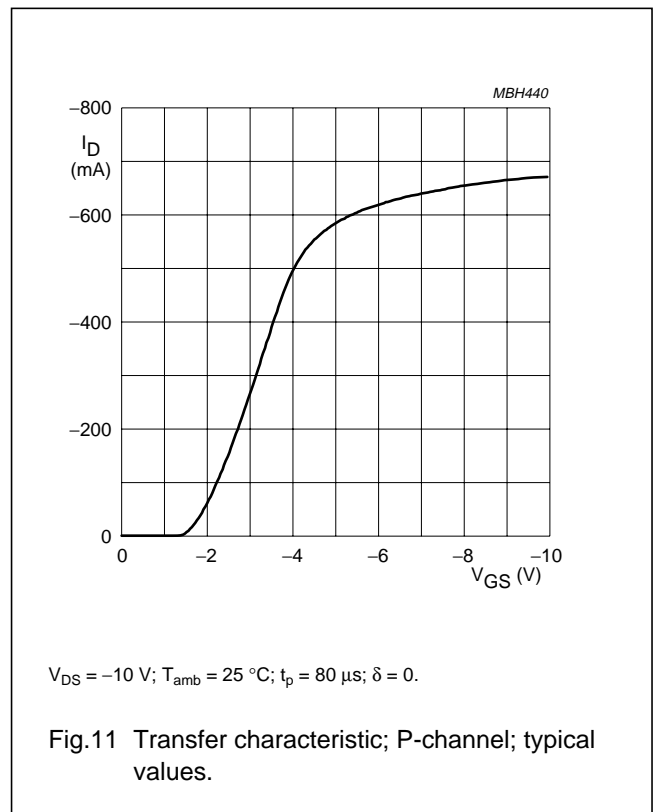
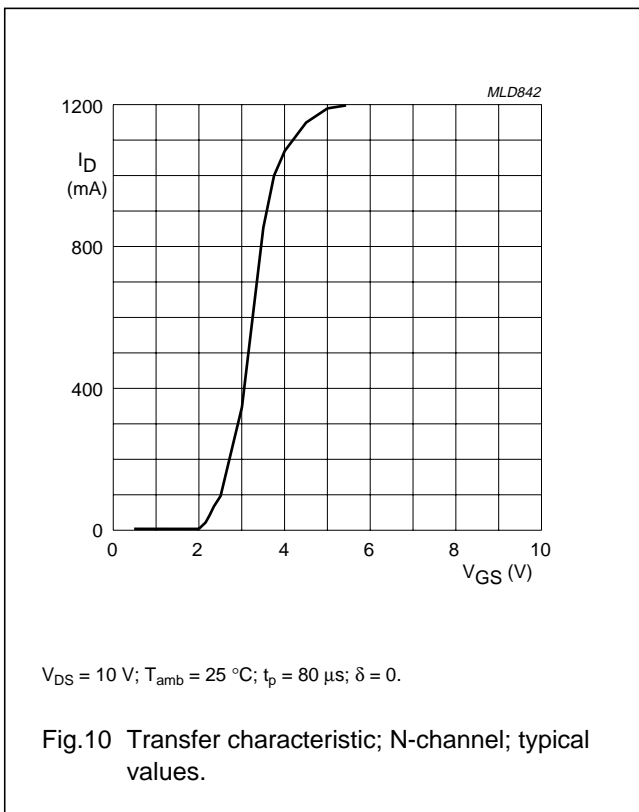
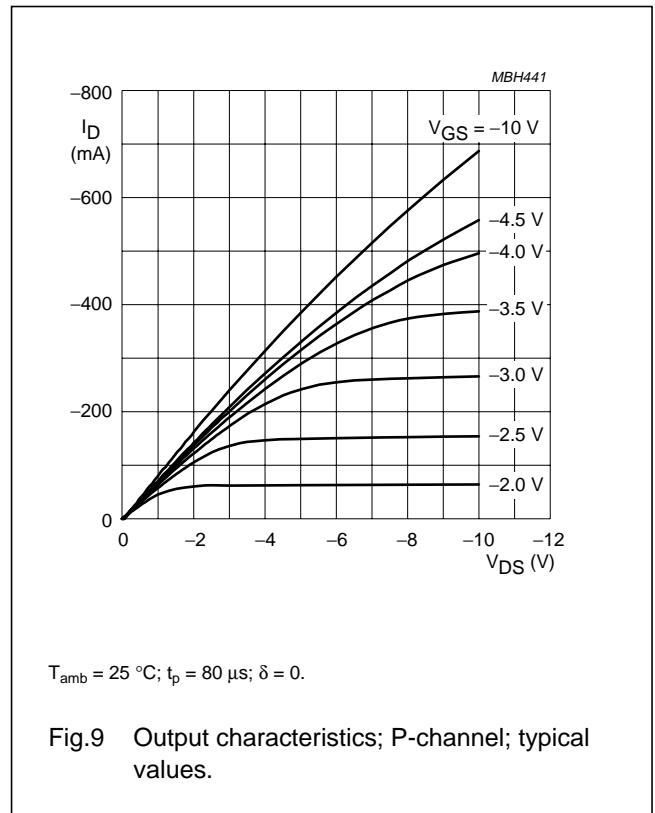
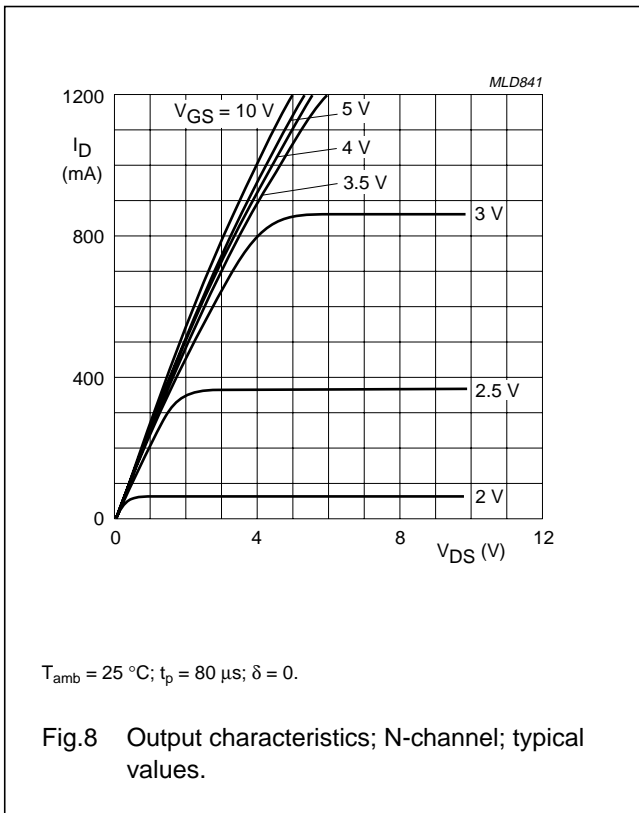


Fig.7 Switching times test circuit with input and output waveforms; P-channel.

Complementary enhancement mode  
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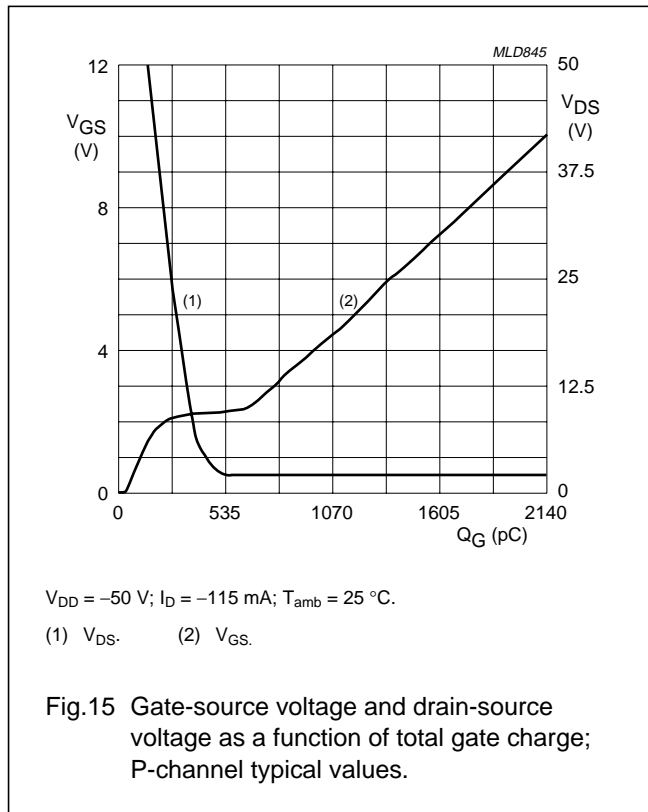
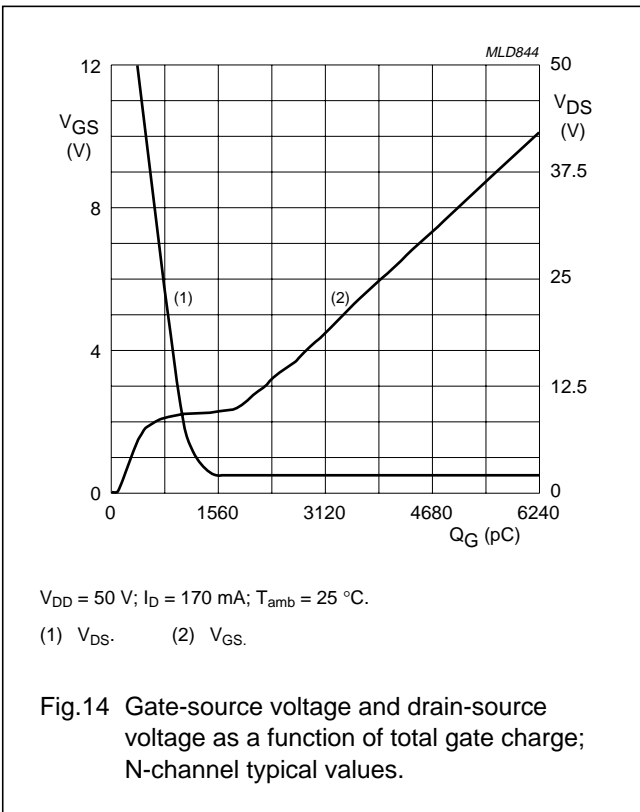
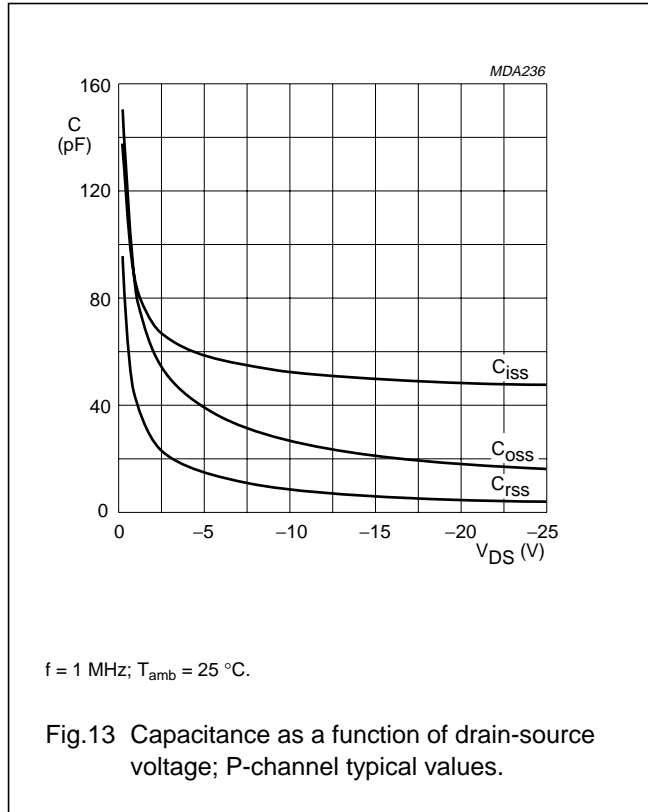
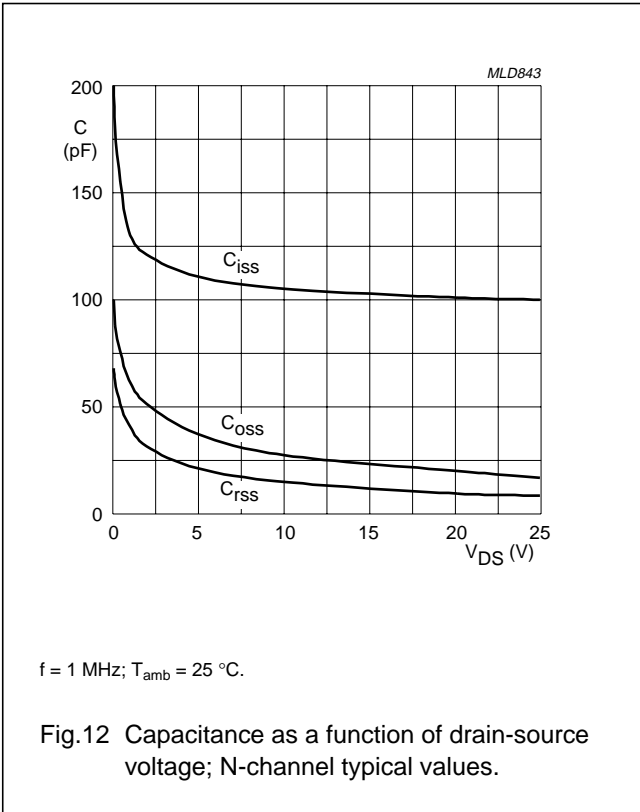
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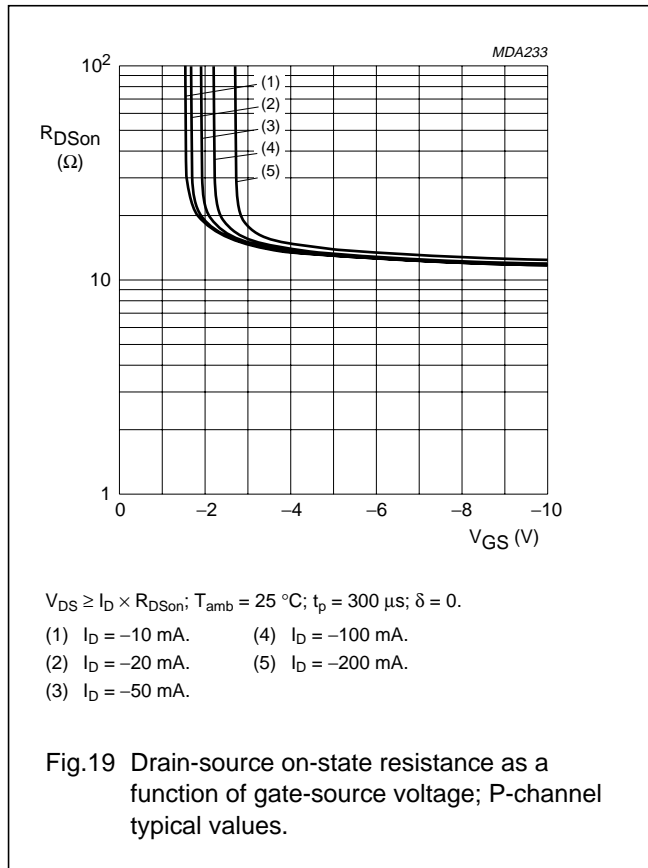
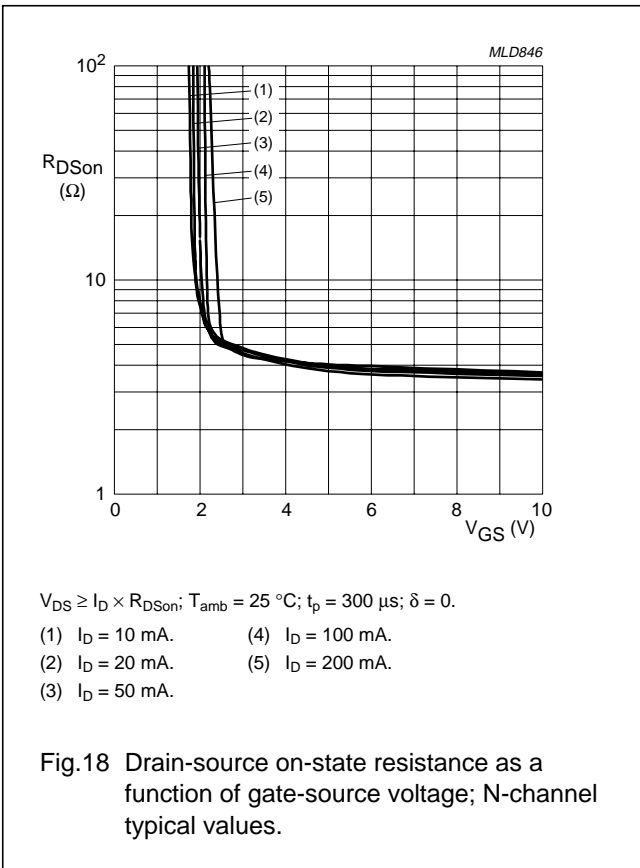
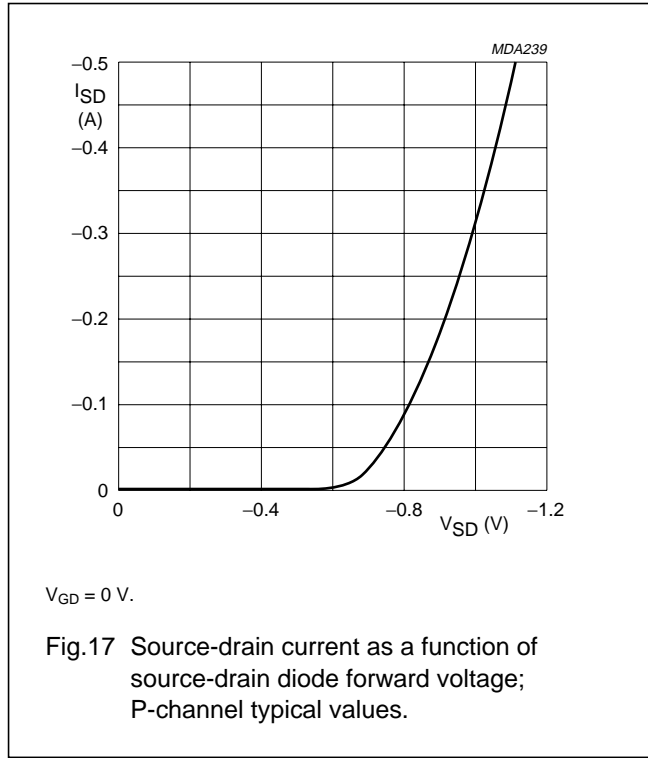
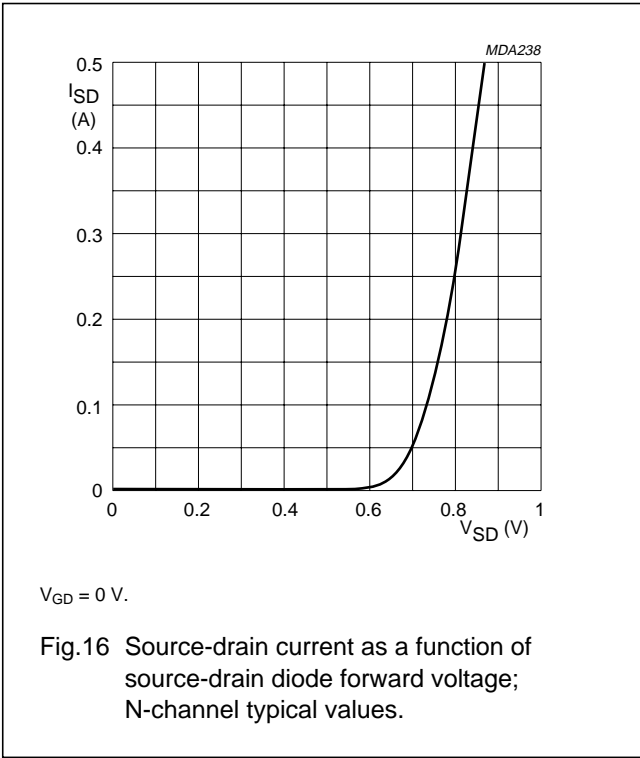
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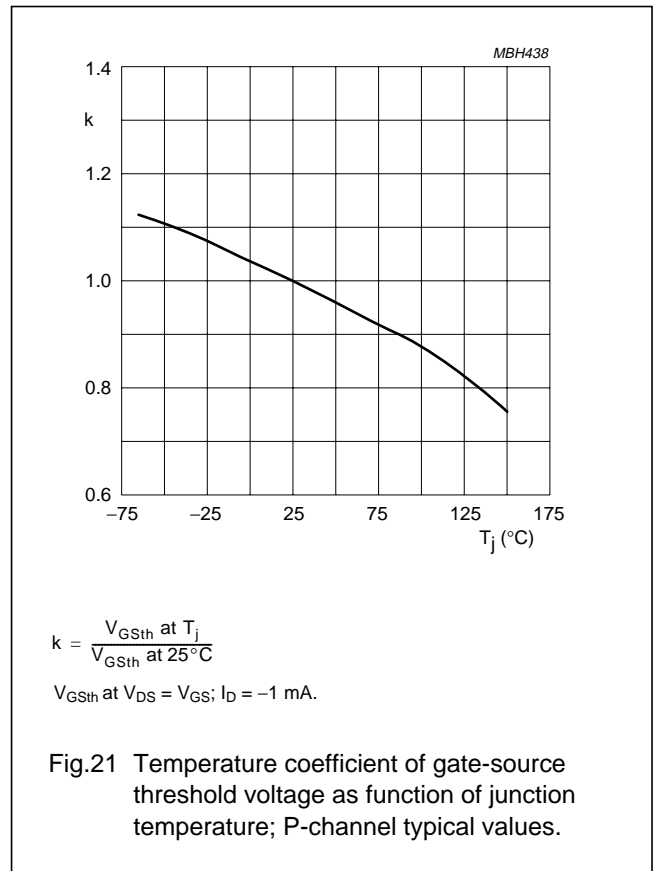
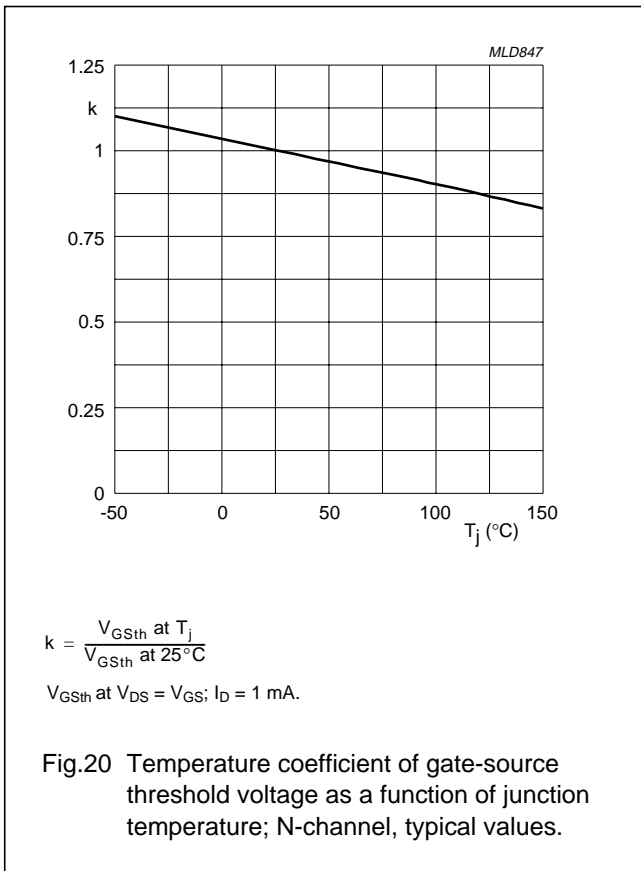
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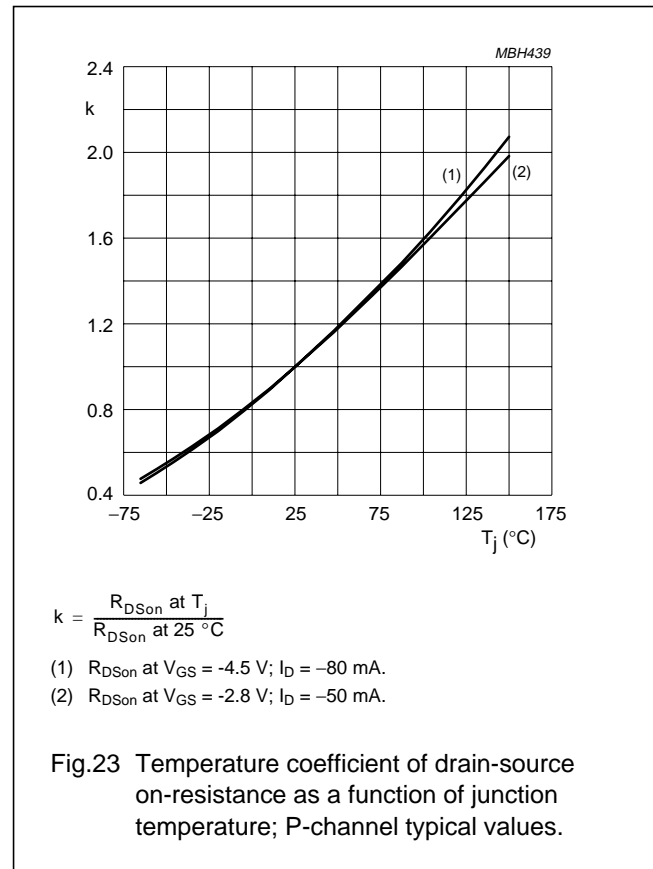
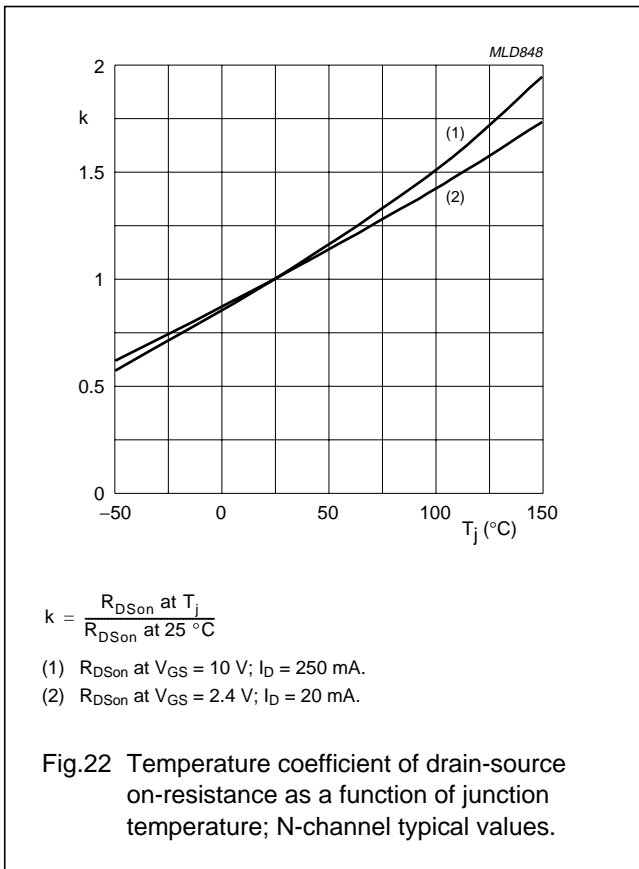
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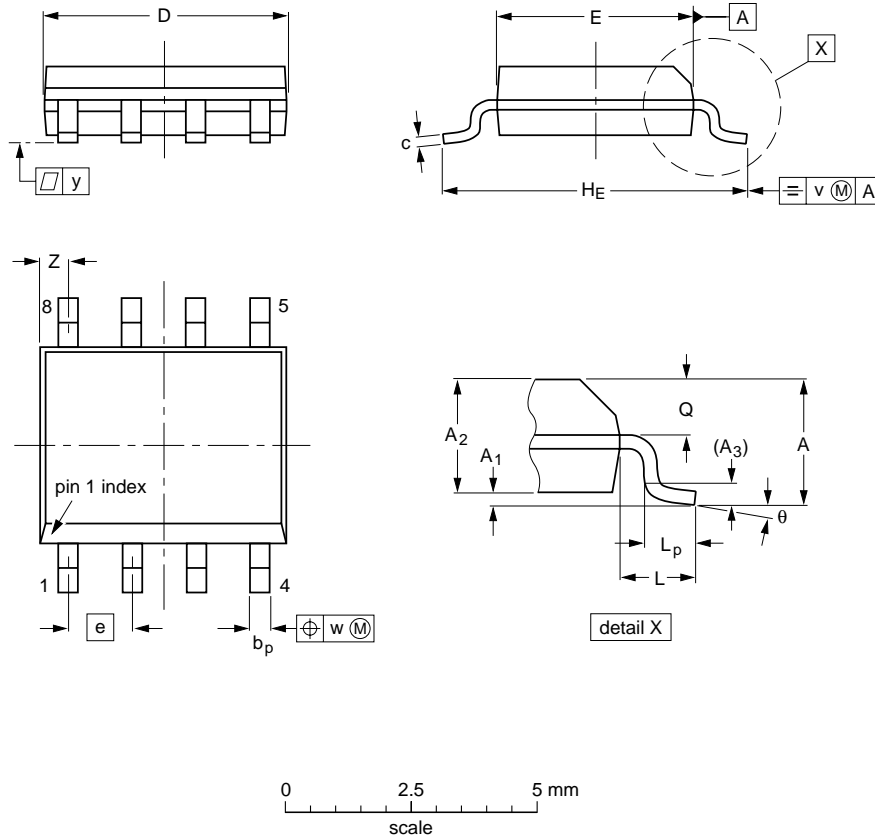
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PACKAGE OUTLINE

S08: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT96-1	076E03	MS-012			97-05-22 99-12-27

# Complementary enhancement mode MOS transistors

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DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
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