

Table 5. Format of 1st data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
MUTE	SM	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 6. Description of 1st data byte bits

Bit	Symbol	Description
7	MUTE	if MUTE = 1 then L and R audio are muted; if MUTE = 0 then L and R audio are not muted
6	SM	Search mode: if SM = 1 then in search mode; if SM = 0 then not in search mode
5 to 0	PLL[13:8]	setting of synthesizer programmable counter for search or preset

Table 7. Format of 2nd data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 8. Description of 2nd data byte bits

Bit	Symbol	Description
7 to 0	PLL[7:0]	setting of synthesizer programmable counter for search or preset

Table 9. Format of 3rd data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
SUD	SSL1	SSL0	HLSI	MS	MR	ML	SWP1

Table 10. Description of 3rd data byte bits

Bit	Symbol	Description
7	SUD	Search Up/Down: if SUD = 1 then search up; if SUD = 0 then search down
6 and 5	SSL[1:0]	Search Stop Level: see Table 11
4	HLSI	High/Low Side Injection: if HLSI = 1 then high side LO injection; if HLSI = 0 then low side LO injection
3	MS	Mono to Stereo: if MS = 1 then forced mono; if MS = 0 then stereo ON
2	MR	Mute Right: if MR = 1 then the right audio channel is muted and forced mono; if MR = 0 then the right audio channel is not muted
1	ML	Mute Left: if ML = 1 then the left audio channel is muted and forced mono; if ML = 0 then the left audio channel is not muted
0	SWP1	Software programmable port 1: if SWP1 = 1 then port 1 is HIGH; if SWP1 = 0 then port 1 is LOW

Table 11. Search stop level setting

SSL1	SSL0	Search stop level
0	0	not allowed in search mode
0	1	low; level ADC output = 5
1	0	mid; level ADC output = 7
1	1	high; level ADC output = 10

Table 12. Format of 4th data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
SWP2	STBY	BL	XTAL	SMUTE	HCC	SNC	SI

Table 13. Description of 4th data byte bits

Bit	Symbol	Description
7	SWP2	Software programmable port 2: if SWP2 = 1 then port 2 is HIGH; if SWP2 = 0 then port 2 is LOW
6	STBY	Standby: if STBY = 1 then in Standby mode; if STBY = 0 then not in Standby mode
5	BL	Band Limits: if BL = 1 then Japanese FM band; if BL = 0 then US/Europe FM band
4	XTAL	Clock frequency: see Table 16
3	SMUTE	Soft Mute: if SMUTE = 1 then soft mute is ON; if SMUTE = 0 then soft mute is OFF
2	HCC	High Cut Control: if HCC = 1 then high cut control is ON; if HCC = 0 then high cut control is OFF
1	SNC	Stereo Noise Cancelling: if SNC = 1 then stereo noise cancelling is ON; if SNC = 0 then stereo noise cancelling is OFF
0	SI	Search Indicator: if SI = 1 then pin SWPORT1 is output for the ready flag; if SI = 0 then pin SWPORT1 is software programmable port 1

Table 14. Format of 5th data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
PLLREF	DTC	-	-	-	-	-	-

Table 15. Description of 5th data byte bits

Bit	Symbol	Description
7	PLLREF	if PLLREF = 1 then the 6.5 MHz reference frequency for the PLL is enabled; if PLLREF = 0 then the 6.5 MHz reference frequency for the PLL is disabled; see Table 16
6	DTC	if DTC = 1 then the de-emphasis time constant is 75 μ s; if DTC = 0 then the de-emphasis time constant is 50 μ s
5 to 0	-	not used; position is don't care

Table 16. Clock bits setting

PLLREF	XTAL	Clock frequency
0	0	13 MHz
0	1	32.768 kHz
1	0	6.5 MHz
1	1	not allowed

8.5 Reading data

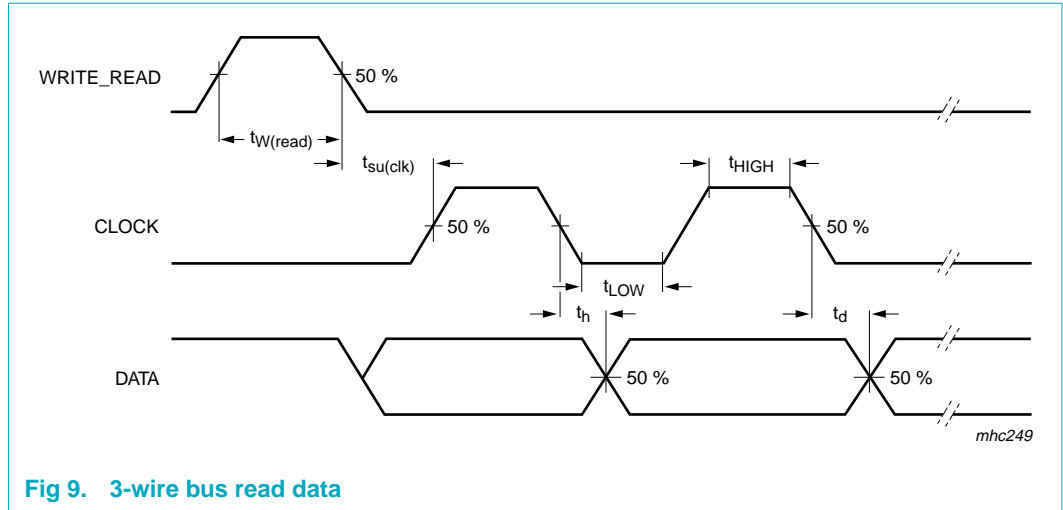


Fig 9. 3-wire bus read data

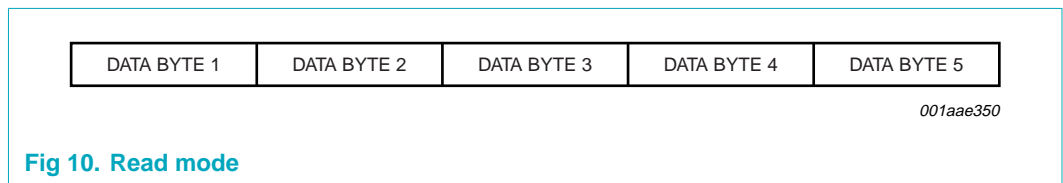


Fig 10. Read mode

Table 17. Format of 1st data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
RF	BLF	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 18. Description of 1st data byte bits

Bit	Symbol	Description
7	RF	Ready Flag: if RF = 1 then a station has been found or the band limit has been reached; if RF = 0 then no station has been found
6	BLF	Band Limit Flag: if BLF = 1 then the band limit has been reached; if BLF = 0 then the band limit has not been reached
5 to 0	PLL[13:8]	setting of synthesizer programmable counter after search or preset

Table 19. Format of 2nd data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 20. Description of 2nd data byte bits

Bit	Symbol	Description
7 to 0	PLL[7:0]	setting of synthesizer programmable counter after search or preset

Table 21. Format of 3rd data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
STEREO	IF6	IF5	IF4	IF3	IF2	IF1	IF0

Table 22. Description of 3rd data byte bits

Bit	Symbol	Description
7	STEREO	Stereo indication: if STEREO = 1 then stereo reception; if STEREO = 0 then mono reception
6 to 0	PLL[13:8]	IF counter result

Table 23. Format of 4th data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
LEV3	LEV2	LEV1	LEV0	CI3	CI2	CI1	0

Table 24. Description of 4th data byte bits

Bit	Symbol	Description
7 to 4	LEV[3:0]	level ADC output
3 to 1	CI[3:1]	Chip Identification: these bits have to be set to logic 0
0	-	this bit is internally set to logic 0

Table 25. Format of 5th data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
0	0	0	0	0	0	0	0

Table 26. Description of 5th data byte bits

Bit	Symbol	Description
7 to 0	-	reserved for future extensions; these bits are internally set to logic 0

9. Internal circuitry

Table 27. Internal circuitry

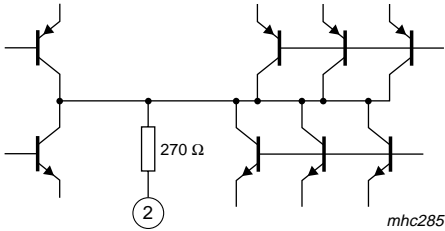
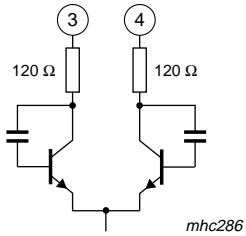
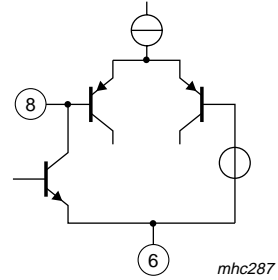
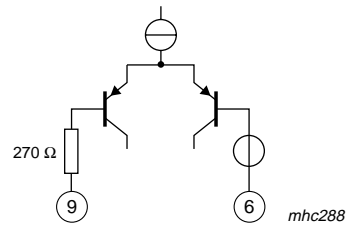
Pin	Symbol	Equivalent circuit
1	n.c.	
2	CPOUT	 <p style="text-align: right;"><i>mhc285</i></p>
3	VCOTANK1	
4	VCOTANK2	 <p style="text-align: right;"><i>mhc286</i></p>
5	V _{CC(VCO)}	

Table 27. Internal circuitry

Pin	Symbol	Equivalent circuit
6	DGND	
7	V _{CCD}	
8	DATA	

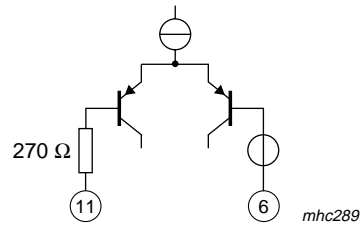


9 CLOCK

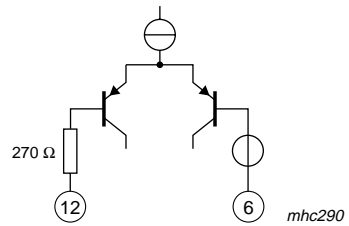


10 n.c.

11 WRITE/READ



12 BUSMODE



13 BUSENABLE

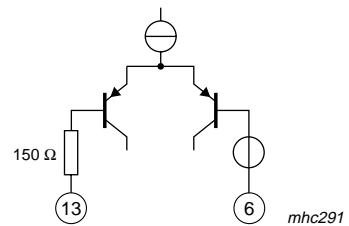


Table 27. Internal circuitry

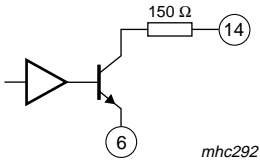
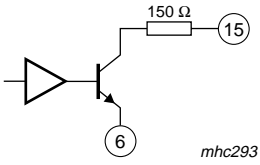
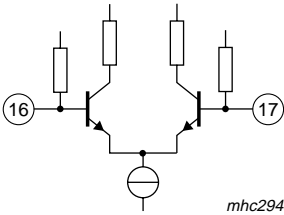
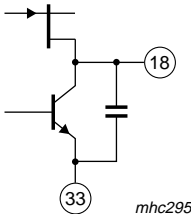
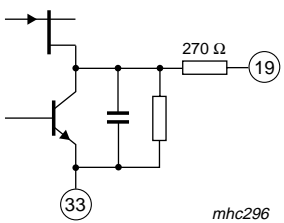
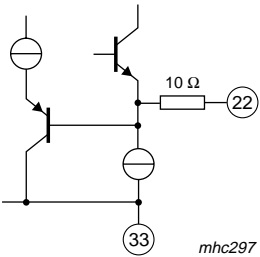
Pin	Symbol	Equivalent circuit
14	SWPORT1	 <p><i>mhc292</i></p>
15	SWPORT2	 <p><i>mhc293</i></p>
16	XTAL1	 <p><i>mhc294</i></p>
17	XTAL2	
18	PHASEFIL	 <p><i>mhc295</i></p>
19	PILFIL	 <p><i>mhc296</i></p>
20	n.c.	
21	n.c.	
22	V _{AFL}	 <p><i>mhc297</i></p>

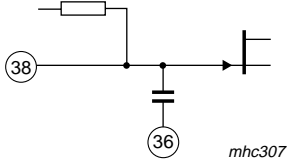
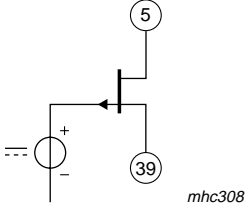
Table 27. Internal circuitry

Pin	Symbol	Equivalent circuit
23	V_{AFR}	<p style="text-align: right;"><i>mhc298</i></p>
24	TMUTE	<p style="text-align: right;"><i>mhc299</i></p>
25	MPXO	<p style="text-align: right;"><i>mhc300</i></p>
26	V_{ref}	<p style="text-align: right;"><i>mhc301</i></p>
27	TIFC	<p style="text-align: right;"><i>mhc302</i></p>

Table 27. Internal circuitry

Pin	Symbol	Equivalent circuit
28	LIMDEC1	
29	LIMDEC2	
30	n.c.	
31	n.c.	
32	I _{gain}	
33	AGND	
34	V _{CCA}	
35	RF1	
36	RFGND	
37	RFI2	

Table 27. Internal circuitry

Pin	Symbol	Equivalent circuit
38	TAGC	 <p>mhc307</p>
39	LOOPSW	 <p>mhc308</p>
40	n.c.	

10. Limiting values

Table 28. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{VCOTANK1}$	VCO tuned circuit output voltage 1		-0.3	+8	V	
$V_{VCOTANK2}$	VCO tuned circuit output voltage 2		-0.3	+8	V	
V_{CCD}	digital supply voltage		-0.3	+5	V	
V_{CCA}	analog supply voltage		-0.3	+8	V	
T_{stg}	storage temperature		-55	+150	°C	
T_{amb}	ambient temperature		-10	+75	°C	
V_{esd}	electrostatic discharge voltage	all pins except pin DATA	[1]	-200	+200	V
			[2]	-2000	+2000	V
		pin DATA	[1]	-150	+200	V
			[2]	-2000	+2000	V

[1] Machine model (R = 0 Ω, C = 200 pF).

[2] Human body model (R = 1.5 kΩ, C = 100 pF).

11. Thermal characteristics

Table 29. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	29	K/W

12. Static characteristics

Table 30. Static characteristics

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD} = 2.7\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Supply voltages^[1]							
V_{CCA}	analog supply voltage		2.5	3.0	5.0	V	
$V_{CC(VCO)}$	voltage controlled oscillator supply voltage		2.5	3.0	5.0	V	
V_{CCD}	digital supply voltage		2.5	3.0	5.0	V	
Supply currents							
I_{CCA}	analog supply current	operating					
		$V_{CCA} = 3\text{ V}$	6.0	8.4	10.5	mA	
		$V_{CCA} = 5\text{ V}$	6.2	8.6	10.7	mA	
		Standby mode					
		$V_{CCA} = 3\text{ V}$	-	3	6	μA	
		$V_{CCA} = 5\text{ V}$	-	3.2	6.2	μA	
$I_{CC(VCO)}$	voltage controlled oscillator supply current	operating					
		$V_{VCOTANK1} = V_{VCOTANK2} = 3\text{ V}$	560	750	940	μA	
		$V_{VCOTANK1} = V_{VCOTANK2} = 5\text{ V}$	570	760	950	μA	
		Standby mode					
		$V_{VCOTANK1} = V_{VCOTANK2} = 3\text{ V}$	-	1	2	μA	
		$V_{VCOTANK1} = V_{VCOTANK2} = 5\text{ V}$	-	1.2	2.2	μA	
I_{CCD}	digital supply current	operating					
		$V_{CCD} = 3\text{ V}$	2.1	3.0	3.9	mA	
		$V_{CCD} = 5\text{ V}$	2.25	3.15	4.05	mA	
		Standby mode; $V_{CCD} = 3\text{ V}$					
		bus enable line HIGH	30	56	80	μA	
		bus enable line LOW	11	19	26	μA	
		Standby mode; $V_{CCD} = 5\text{ V}$					
		bus enable line HIGH	50	78	105	μA	
		bus enable line LOW	20	33	45	μA	

[1] V_{CCA} , $V_{CC(VCO)}$ and V_{CCD} must not differ more than 200 mV.

Table 31. DC operating points, unloaded DC voltage

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD} = 2.7\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Operating point	Conditions	Min	Typ	Max	Unit
V_{CPOUT}		0.1	-	$V_{CC(VCO)} - 0.1$	V
V_{XTAL2}	data byte 4 bit 4 = 1	1.64	1.72	1.8	V
	data byte 4 bit 4 = 0	1.68	1.75	1.82	V
V_{XTAL2}	data byte 4 bit 4 = 1	1.64	1.72	1.8	V
	data byte 4 bit 4 = 0	1.68	1.75	1.82	V
$V_{PHASEFIL}$		0.4	1.2	$V_{CCA} - 0.4$	V

Table 31. DC operating points, unloaded DC voltage ...continued

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD} = 2.7\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Operating point	Conditions	Min	Typ	Max	Unit
V_{PILFIL}		0.65	0.9	1.3	V
V_{AFL}	$f_{RF} = 98\text{ MHz}$; $V_{RF} = 1\text{ mV}$	720	850	940	mV
V_{AFR}	$f_{RF} = 98\text{ MHz}$; $V_{RF} = 1\text{ mV}$	720	850	940	mV
V_{TMUTE}	$V_{RF} = 0\text{ V}$	1.5	1.65	1.8	V
V_{MPXO}	$f_{RF} = 98\text{ MHz}$; $V_{RF} = 1\text{ mV}$	680	815	950	mV
V_{ref}		1.45	1.55	1.65	V
V_{TIFC}		1.34	1.44	1.54	V
$V_{LIMDEC1}$		1.86	1.98	2.1	V
$V_{LIMDEC2}$		1.86	1.98	2.1	V
V_{Igain}		480	530	580	mV
V_{RF1}		0.93	1.03	1.13	V
V_{RF12}		0.93	1.03	1.13	V
V_{TAGC}	$V_{RF} = 0\text{ V}$	1	1.57	2	V

13. Dynamic characteristics

Table 32. Dynamic characteristics

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD} = 2.7\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; measured in the circuit of [Figure 13](#); AC values are given in RMS; for V_{RF} the EMF value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage controlled oscillator						
f_{osc}	oscillator frequency		150	-	217	MHz
Crystal oscillator						
Circuit input: pin XTAL2						
$V_{i(osc)}$	oscillator input voltage	oscillator externally clocked	140	-	350	mV
R_i	input resistance	oscillator externally clocked				
		data byte 4 bit 4 = 0	2	3	4	k Ω
		data byte 4 bit 4 = 1	230	330	430	k Ω
C_i	input capacitance	oscillator externally clocked				
		data byte 4 bit 4 = 0	3.9	5.6	7.3	pF
		data byte 4 bit 4 = 1	5	6	7	pF
Crystal: 32.768 kHz						
f_r	series resonance frequency	data byte 4 bit 4 = 1	-	32.768	-	kHz
$\Delta f/f_r$	frequency deviation		-20×10^{-6}	-	$+20 \times 10^{-6}$	
C_0	shunt capacitance		-	-	3.5	pF
R_S	series resistance		-	-	80	k Ω
$\Delta f_r/f_r(25\text{ }^{\circ}\text{C})$	temperature drift	$-10\text{ }^{\circ}\text{C} < T_{amb} < +60\text{ }^{\circ}\text{C}$	-50×10^{-6}	-	$+50 \times 10^{-6}$	
Crystal: 13 MHz						
f_r	series resonance frequency	data byte 4 bit 4 = 0	-	13	-	MHz

Table 32. Dynamic characteristics ...continued

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD} = 2.7 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; measured in the circuit of [Figure 13](#); AC values are given in RMS; for V_{RF} the EMF value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta f/f_r$	frequency deviation		-30×10^{-6}	-	$+30 \times 10^{-6}$	
C_0	shunt capacitance		-	-	4.5	pF
C_{mot}	motional capacitance		1.5	-	3.0	fF
R_S	series resistance		-	-	100	k Ω
$\Delta f/f_r(25 \text{ }^\circ\text{C})$	temperature drift	$-40 \text{ }^\circ\text{C} < T_{amb} < +85 \text{ }^\circ\text{C}$	-30×10^{-6}	-	$+30 \times 10^{-6}$	

SynthesizerProgrammable divider^[1]

N_{prog}	programmable divider ratio	data byte 1 = XX11 1111; data byte 2 = 1111 1110	-	-	8191	
		data byte 1 = XX01 0000; data byte 2 = 0000 0000	2048	-	-	
ΔN_{step}	programmable divider step size		-	1	-	

Reference frequency divider

N_{ref}	crystal oscillator divider ratio	data byte 4 bit 4 = 0	-	260	-	
		data byte 5 bit 7 = 1; data byte 4 bit 4 = 0	-	130	-	
		data byte 4 bit 4 = 1	-	1	-	

Charge pump: pin CPOUT

I_{sink}	charge pump peak sink current	$0.2 \text{ V} < V_{CPOUT} < V_{VCOTANK2} - 0.2 \text{ V}$; $f_{VCO} > f_{ref} \times N_{prog}$	-	0.5	-	μA
I_{source}	charge pump peak source current	$0.2 \text{ V} < V_{CPOUT} < V_{VCOTANK2} - 0.2 \text{ V}$; $f_{VCO} < f_{ref} \times N_{prog}$	-	-0.5	-	μA

IF counter

V_{RF}	RF input voltage for correct IF count		-	12	18	μV
N_{IF}	IF counter length		-	7	-	bit
$N_{precount}$	IF counter prescaler ratio		-	64	-	
$T_{count(IF)}$	IF counter period	$f_{xtal} = 32.768 \text{ kHz}$	-	15.625	-	ms
		$f_{xtal} = 13 \text{ MHz}$	-	15.754	-	ms
$RES_{count(IF)}$	IF counter resolution	$f_{xtal} = 32.768 \text{ kHz}$	-	4.096	-	kHz
		$f_{xtal} = 13 \text{ MHz}$	-	4.0625	-	kHz
IF_{count}	IF counter result for search tuning stop	$f_{xtal} = 32.768 \text{ kHz}$	29h	-	3Dh	
		$f_{xtal} = 13 \text{ MHz}$	30h	-	3Dh	

Pins DATA, CLOCK, WRITE/READ, BUSMODE and BUSENABLE

R_i	input resistance		10	-	-	M Ω
-------	------------------	--	----	---	---	------------

Table 32. Dynamic characteristics ...continued

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD} = 2.7 \text{ V}$; $T_{amb} = 25^\circ \text{C}$; measured in the circuit of [Figure 13](#); AC values are given in RMS; for V_{RF} the EMF value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Software programmable ports						
Pin SWPORT1						
$I_{\text{sink(max)}}$	maximum sink current	data byte 3 bit 0 = 0; data byte 4 bit 0 = 0; $V_{\text{SWPORT1}} < 0.5 \text{ V}$	500	-	-	μA
$I_{\text{leak(max)}}$	maximum leakage current	data byte 3 bit 0 = 1; $V_{\text{SWPORT1}} < 5 \text{ V}$	-1	-	+1	μA
Pin SWPORT2						
$I_{\text{sink(max)}}$	maximum sink current	data byte 4 bit 7 = 0; $V_{\text{SWPORT1}} < 0.5 \text{ V}$	500	-	-	μA
$I_{\text{leak(max)}}$	maximum leakage current	data byte 4 bit 7 = 1; $V_{\text{SWPORT1}} < 5 \text{ V}$	-1	-	+1	μA
FM signal channel						
FM RF input						
$f_{\text{FM(ant)}}$	FM input frequency		76	-	108	MHz
R_i	input resistance at pins RFI1 and RFI2 to RFGND		75	100	125	Ω
C_i	input capacitance at pins RFI1 and RFI2 to RFGND		2.5	4	6	pF
V_{RF}	RF sensitivity input voltage	$f_{\text{RF}} = 76 \text{ MHz to } 108 \text{ MHz}$; $\Delta f = 22.5 \text{ kHz}$; $f_{\text{mod}} = 1 \text{ kHz}$; (S+N)/N = 26 dB; L = R; de-emphasis = 75 μs ; $B_{\text{AF}} = 300 \text{ Hz to } 15 \text{ kHz}$	-	2	3.5	μV
IP3_{in}	in-band 3rd-order intercept point related to $V_{\text{RFI1-RFI2}}$ (peak value)	$\Delta f_1 = 200 \text{ kHz}$; $\Delta f_2 = 400 \text{ kHz}$; $f_{\text{tune}} = 76 \text{ MHz to } 108 \text{ MHz}$	81	84	-	$\text{dB}\mu\text{V}$
IP3_{out}	out-band 3rd-order intercept point related to $V_{\text{RFI1-RFI2}}$ (peak value)	$\Delta f_1 = 4 \text{ MHz}$; $\Delta f_2 = 8 \text{ Hz}$; $f_{\text{tune}} = 76 \text{ MHz to } 108 \text{ MHz}$	82	85	-	$\text{dB}\mu\text{V}$
RF AGC						
V_{RF1}	RF input voltage for start of AGC	$f_{\text{RF1}} = 93 \text{ MHz}$; $f_{\text{RF2}} = 98 \text{ MHz}$; $V_{\text{RF2}} = 50 \text{ dB}\mu\text{V}$; $\left \frac{\Delta V_{\text{TMUTE}}}{V_{\text{RF1}}} \right < \frac{14 \text{ mV}}{3 \text{ dB}\mu\text{V}}$	[2] 66	72	78	$\text{dB}\mu\text{V}$
IF filter						
f_{IF}	IF filter center frequency		215	225	235	kHz
B_{IF}	IF filter bandwidth		85	94	102	kHz
S_{+200}	high side 200 kHz selectivity	$\Delta f = +200 \text{ kHz}$; $f_{\text{tune}} = 76 \text{ MHz to } 108 \text{ MHz}$	[3] 39	43	-	dB
S_{-200}	low side 200 kHz selectivity	$\Delta f = -200 \text{ kHz}$; $f_{\text{tune}} = 76 \text{ MHz to } 108 \text{ MHz}$	[3] 32	36	-	dB
S_{+100}	high side 100 kHz selectivity	$\Delta f = +100 \text{ kHz}$; $f_{\text{tune}} = 76 \text{ MHz to } 108 \text{ MHz}$	[3] 8	12	-	dB

Table 32. Dynamic characteristics ...continued

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD} = 2.7 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; measured in the circuit of [Figure 13](#); AC values are given in RMS; for V_{RF} the EMF value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
S ₋₁₀₀	low side 100 kHz selectivity	$\Delta f = -100 \text{ kHz}$; $f_{\text{tune}} = 76 \text{ MHz to } 108 \text{ MHz}$	[3] 8	12	-	dB
IR	image rejection	$f_{\text{tune}} = 76 \text{ MHz to } 108 \text{ MHz}$; $V_{RF} = 50 \text{ dB}\mu\text{V}$	24	30	-	dB
FM IF level detector and mute voltage						
V_{RF}	RF input voltage for start of level ADC	read mode data byte 4 bit 4 = 1	2	3	5	μV
ΔV_{step}	level ADC step size		2	3	5	dB
Pin TMUTE						
V_{level}	level output DC voltage	$V_{RF} = 0 \mu\text{V}$	1.55	1.65	1.80	V
		$V_{RF} = 3 \mu\text{V}$	1.60	1.70	1.85	V
$V_{\text{level(slope)}}$	slope of level voltage	$V_{RF} = 10 \mu\text{V to } 500 \mu\text{V}$	150	165	180	$\frac{\text{mV}}{20 \text{ dB}}$
R_o	output resistance		280	400	520	k Ω
FM demodulator: pin MPXO						
V_{MPXO}	demodulator output voltage	$V_{RF} = 1 \text{ mV}$; $L = R$; $\Delta f = 22.5 \text{ kHz}$; $f_{\text{mod}} = 1 \text{ kHz}$; de-emphasis = 75 μs ; $B_{AF} = 300 \text{ Hz to } 15 \text{ kHz}$	60	75	90	mV
(S+N)/N	maximum signal plus noise-to-noise ratio	$V_{RF} = 1 \text{ mV}$; $L = R$; $\Delta f = 22.5 \text{ kHz}$; $f_{\text{mod}} = 1 \text{ kHz}$; de-emphasis = 75 μs ; $B_{AF} = 300 \text{ Hz to } 15 \text{ kHz}$	54	60	-	dB
THD	total harmonic distortion	$V_{RF} = 1 \text{ mV}$; $L = R$; $\Delta f = 75 \text{ kHz}$; $f_{\text{mod}} = 1 \text{ kHz}$; de-emphasis = 75 μs	-	0.5	1.5	%
α_{AM}	AM suppression	$V_{RF} = 300 \mu\text{V}$; $L = R$; $\Delta f = 22.5 \text{ kHz}$; $f_{\text{mod}} = 1 \text{ kHz}$; $m = 0.3$; de-emphasis = 75 μs ; $B_{AF} = 300 \text{ Hz to } 15 \text{ kHz}$	40	-	-	dB
R_o	demodulator output resistance		-	-	500	Ω
I_{sink}	demodulator output sink current		-	-	30	μA
Soft mute						
V_{RF}	RF input voltage for soft mute start	$\alpha_{\text{mute}} = 3 \text{ dB}$; data byte 4 bit 3 = 1	3	5	10	μV
α_{mute}	mute attenuation	$V_{RF} = 1 \mu\text{V}$; $L = R$; $\Delta f = 22.5 \text{ kHz}$; $f_{\text{mod}} = 1 \text{ kHz}$; de-emphasis = 75 μs ; $B_{AF} = 300 \text{ Hz to } 15 \text{ kHz}$; data byte 4 bit 3 = 1	10	20	30	dB

Table 32. Dynamic characteristics ...continued

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD} = 2.7 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; measured in the circuit of [Figure 13](#); AC values are given in RMS; for V_{RF} the EMF value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MPX decoder						
V_{AFL}	left audio frequency output voltage	$V_{RF} = 1 \text{ mV}$; $L = R$; $\Delta f = 22.5 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; de-emphasis = $75 \text{ } \mu\text{s}$	60	75	90	mV
V_{AFR}	right audio frequency output voltage	$V_{RF} = 1 \text{ mV}$; $L = R$; $\Delta f = 22.5 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; de-emphasis = $75 \text{ } \mu\text{s}$	60	75	90	mV
R_{AFL}	left audio frequency output resistance		-	-	50	Ω
R_{AFR}	right audio frequency output resistance		-	-	50	Ω
$I_{sink(AFL)}$	left audio frequency output sink current		170	-	-	μA
$I_{sink(AFR)}$	right audio frequency output sink current		170	-	-	μA
$V_{MPXIN(max)}$	input overdrive margin	THD < 3 %	4	-	-	dB
V_{AFL}	left audio frequency output voltage difference	$V_{RF} = 1 \text{ mV}$; $L = R$; $\Delta f = 75 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; de-emphasis = $75 \text{ } \mu\text{s}$	-1	-	+1	dB
V_{AFR}	right audio frequency output voltage difference	$V_{RF} = 1 \text{ mV}$; $L = R$; $\Delta f = 75 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; de-emphasis = $75 \text{ } \mu\text{s}$	-1	-	+1	dB
$\alpha_{cs(stereo)}$	stereo channel separation	$V_{RF} = 1 \text{ mV}$; $R = L = 0$ or $R = 0$ and $L = 1$ including 9 % pilot; $\Delta f = 75 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; data byte 3 bit 3 = 0; data byte 4 bit 1 = 1	24	30	-	dB
(S+N)/N	maximum signal plus noise-to-noise ratio	$V_{RF} = 1 \text{ mV}$; $L = R$; $\Delta f = 22.5 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; de-emphasis = $75 \text{ } \mu\text{s}$; $B_{AF} = 300 \text{ Hz to } 15 \text{ kHz}$	54	60	-	dB
THD	total harmonic distortion	$V_{RF} = 1 \text{ mV}$; $L = R$; $\Delta f = 75 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; de-emphasis = $75 \text{ } \mu\text{s}$	-	0.4	1	%
α_{pilot}	pilot suppression measured at pins V_{AFL} and V_{AFR}	related to $\Delta f = 75 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; de-emphasis = $75 \text{ } \mu\text{s}$	40	50	-	dB
Δf_{pilot}	stereo pilot frequency deviation	$V_{RF} = 1 \text{ mV}$; read mode				
		data byte 3 bit 7 = 1	-	3.6	5.8	kHz
		data byte 3 bit 7 = 0	1	3	-	kHz
$\frac{\Delta f_{pilot1}}{\Delta f_{pilot2}}$	pilot switch hysteresis	$V_{RF} = 1 \text{ mV}$	2	-	-	dB

Table 32. Dynamic characteristics ...continued

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD} = 2.7 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; measured in the circuit of [Figure 13](#); AC values are given in RMS; for V_{RF} the EMF value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High cut control						
TC_{de-em}	de-emphasis time constant	$V_{RF} = 1 \text{ mV}$				
		data byte 5 bit 6 = 0	38	50	62	μs
		data byte 5 bit 6 = 1	57	75	93	μs
		$V_{RF} = 1 \text{ } \mu\text{V}$				
		data byte 5 bit 6 = 0	114	150	186	μs
		data byte 5 bit 6 = 1	171	225	279	μs
Mono to stereo blend control						
$\alpha_{cs(\text{stereo})}$	stereo channel separation	$V_{RF} = 45 \text{ } \mu\text{V}$; $R = L = 0$ or $R = 0$ and $L = 1$ including 9 % pilot; $\Delta f = 75 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; data byte 3 bit 3 = 0; data byte 4 bit 1 = 1	4	10	16	dB
Mono to stereo switched						
$\alpha_{cs(\text{stereo})}$	stereo channel separation switching from mono to stereo with increasing RF input level	$R = L = 0$ or $R = 0$ and $L = 1$ including 9 % pilot; $\Delta f = 75 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; data byte 3 bit 3 = 0; data byte 4 bit 1 = 0				
		$V_{RF} = 1 \text{ mV}$	24	-	-	dB
		$V_{RF} = 20 \text{ } \mu\text{V}$	-	-	1	dB
Bus-driven mute functions						
Tuning mute						
α_{mute}	V_{AFL} and V_{AFR} muting depth	data byte 1 bit 7 = 1	-	-	-60	dB
$\alpha_{mute(L)}$	V_{AFL} muting depth	data byte 3 bit 1 = 1; $f_{AF} = 1 \text{ kHz}$; $R_{load(L)} < 30 \text{ k}\Omega$	-	-	-80	dB
$\alpha_{mute(R)}$	V_{AFR} muting depth	data byte 3 bit 2 = 1; $f_{AF} = 1 \text{ kHz}$; $R_{load(R)} < 30 \text{ k}\Omega$	-	-	-80	dB

[1] Calculation of this 14-bit word can be done as follows:

$$\text{formula for high side injection: } N = \frac{4 \times (f_{RF} + f_{IF})}{f_{ref}}; \text{ formula for low side injection: } N = \frac{4 \times (f_{RF} - f_{IF})}{f_{ref}}$$

where:

N = decimal value of PLL word;

f_{RF} = the wanted tuning frequency [Hz];

f_{IF} = the intermediate frequency [Hz] = 225 kHz;

f_{ref} = the reference frequency [Hz] = 32.768 kHz for the 32.768 kHz crystal; $f_{ref} = 50 \text{ kHz}$ for the 13 MHz crystal or when externally clocked with 6.5 MHz.

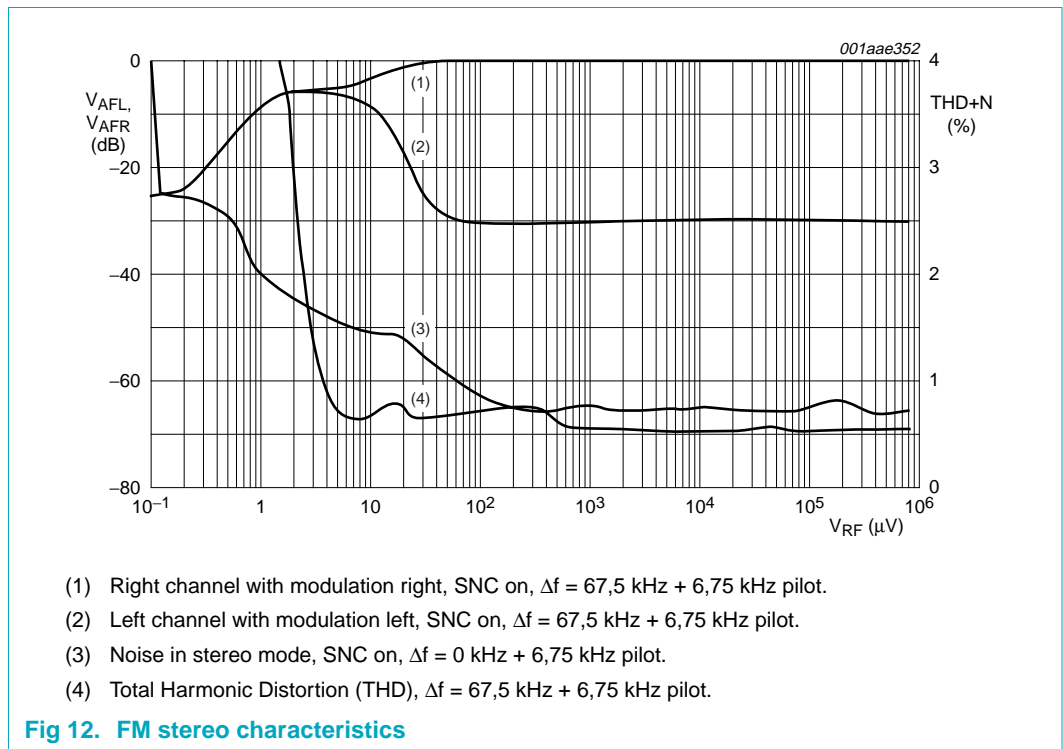
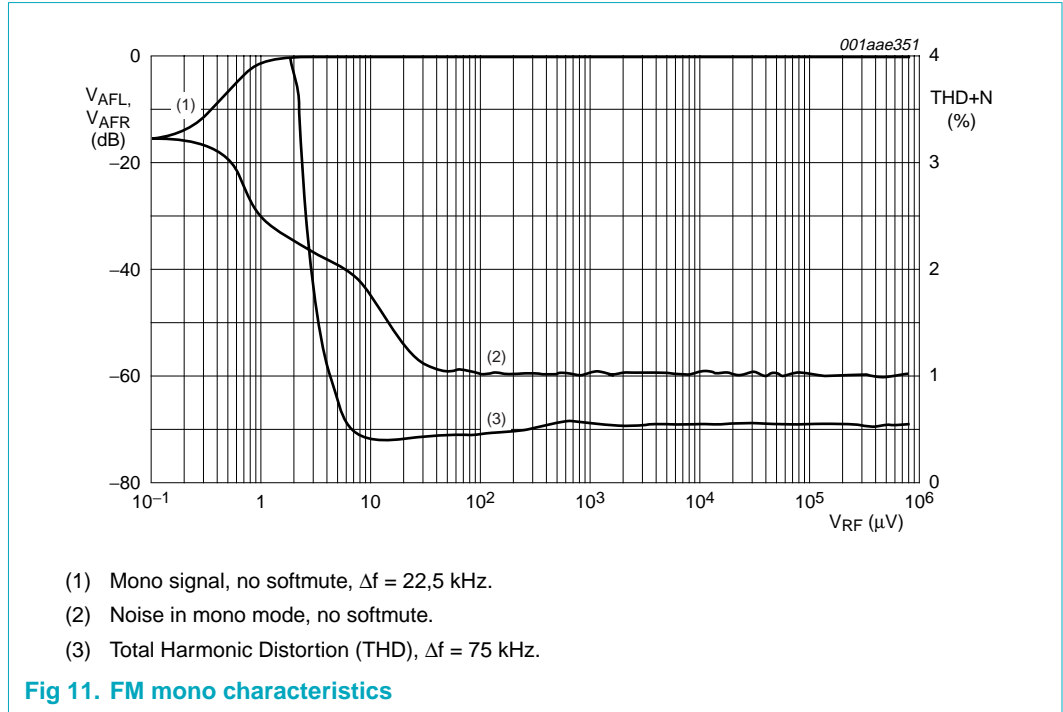
$$\text{Example for receiving a channel at 100 MHz with high side injection: } N = \frac{4 \times (100 \times 10^6 + 225 \times 10^3)}{32768} = 12234$$

The PLL word becomes 2FCAh.

[2] V_{RF} in [Figure 13](#) is replaced by $V_{RF1} + V_{RF2}$. The radio is tuned to 98 MHz (high side injection).

[3] Low side and high side selectivity can be switched by changing the mixer from high side to low side LO injection.

14. FM characteristics



15. I²C-bus characteristics

Table 33. Digital levels and timing

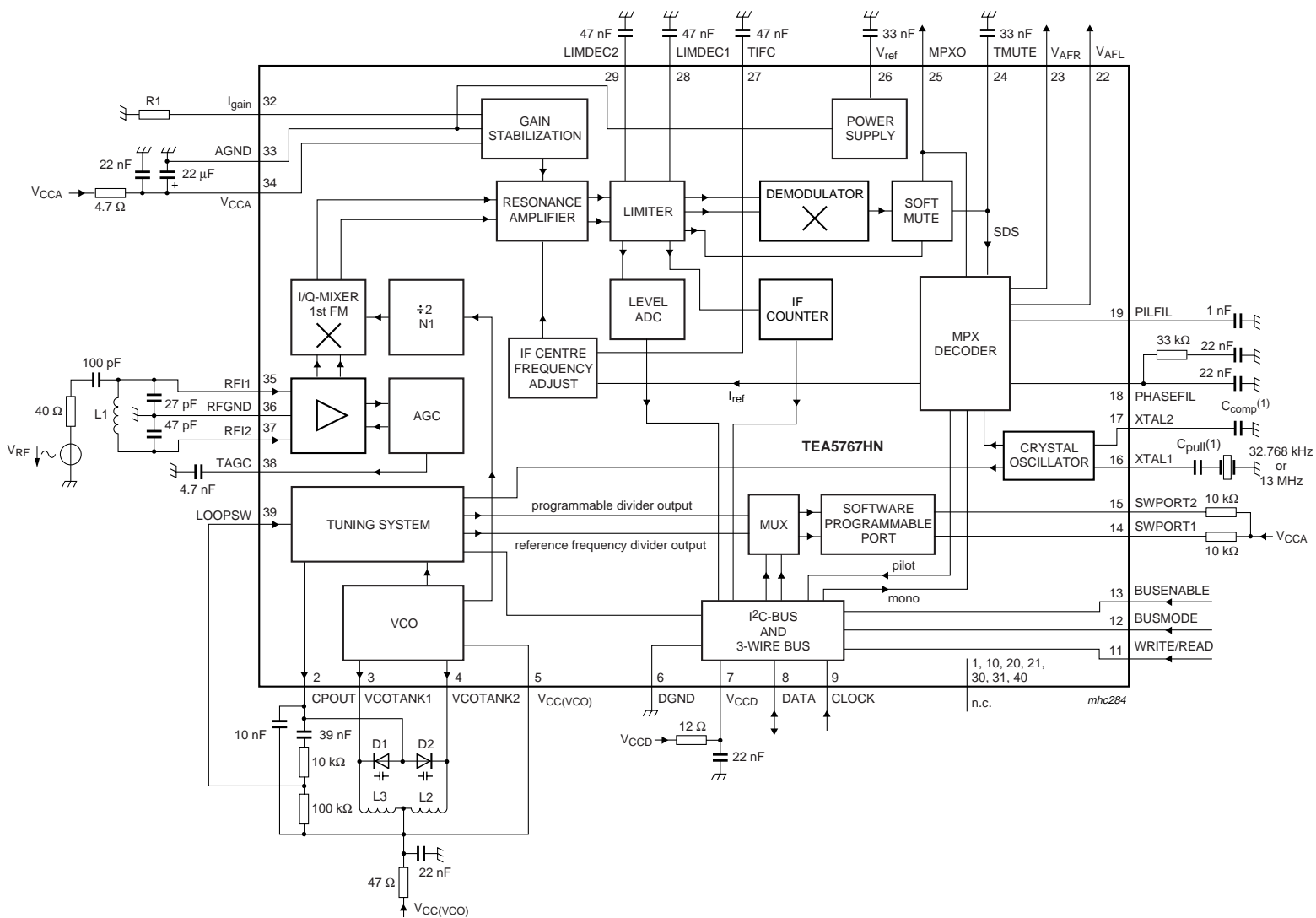
Symbol	Parameter	Conditions	Min	Max	Unit
Digital inputs					
V _{IH}	HIGH-level input voltage		0.45V _{CCD}	-	V
V _{IL}	LOW-level input voltage		-	0.2V _{CCD}	V
Digital outputs					
I _{sink(L)}	LOW-level sink current		500	-	μA
V _{OL}	LOW-level output voltage	I _{OL} = 500 μA	-	450	mV
Timing					
f _{clk}	clock input frequency	I ² C-bus enabled	-	400	kHz
		3-wire bus enabled	-	400	kHz
t _{HIGH}	clock HIGH time	I ² C-bus enabled	1	-	μs
		3-wire bus enabled	1	-	μs
t _{LOW}	clock LOW time	I ² C-bus enabled	1	-	μs
		3-wire bus enabled	1	-	μs
t _{W(write)}	pulse width for write enable	3-wire bus enabled	1	-	μs
t _{W(read)}	pulse width for read enable	3-wire bus enabled	1	-	μs
t _{SU(clk)}	clock set-up time	3-wire bus enabled	300	-	ns
t _{h(out)}	read mode data output hold time	3-wire bus enabled	10	-	ns
t _{d(out)}	read mode output delay time	3-wire bus enabled	-	400	ns
t _{SU(write)}	write mode set-up time	3-wire bus enabled	100	-	ns
t _{h(write)}	write mode hold time	3-wire bus enabled	100	-	ns

16. Test information

Table 34. Component list for [Figure 1](#) and [Figure 13](#)

Component	Parameter	Value	Tolerance	Type	Manufacturer
R1	resistor with low temperature coefficient	18 kΩ	±1 %	RC12G	Philips
D1 and D2	varicap for VCO tuning	-	-	BB202	Philips
L1	RF band filter coil	120 nH	±2 %	Q _{min} = 40	
L2 and L3	VCO coil	33 nH	±2 %	Q _{min} = 40	
XTAL13MHz	13 MHz crystal	-	-	NX4025GA	
C _{pull}	pulling capacitor for NX4025GA	10 pF	-		
XTAL32768Hz	32,768 kHz crystal	-	-		
C _{pull}	pulling capacitor for XTAL32768Hz	C _{load} ^[1]	-		

[1] Value of the C_{pull} must be as close as possible to the value of C_{load} of the crystal.



Value of C_{pull} must be as close as possible to the value of C_{load} of the crystal.

(1) C_{comp} and C_{pull} data depends on crystal specification.

Fig 13. Application and test diagram

17. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm

SOT618-1

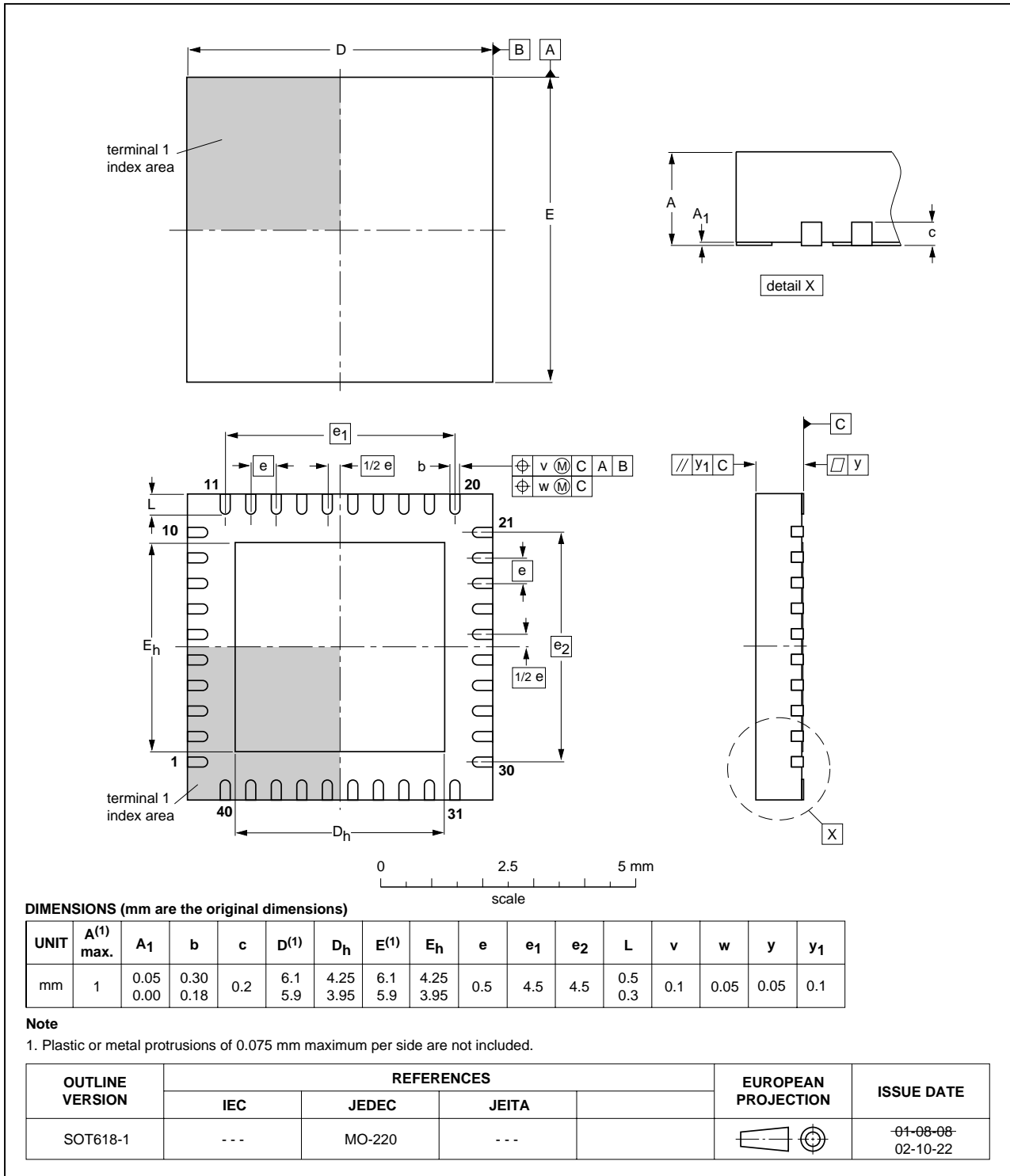


Fig 14. Package outline SOT618-1 (HVQFN40)

18. Soldering

18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
 - for all BGA, HTSSON..T and SSOP..T packages
 - for packages with a thickness ≥ 2.5 mm
 - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm³ so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm³ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

18.5 Package related soldering information

Table 35. Suitability of surface mount IC packages for wave and reflow soldering methods

Package ^[1]	Soldering method	
	Wave	Reflow ^[2]
BGA, HTSSON..T ^[3] , LBGA, LFBGA, SQFP, SSOP..T ^[3] , TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable ^[4]	suitable
PLCC ^[5] , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ^{[5][6]}	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended ^[7]	suitable
CWQCCN..L ^[8] , PMFP ^[9] , WQCCN..L ^[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note (AN01026)*; order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

19. Revision history

Table 36. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA5767HN_4	20060220	Product data sheet	-	TEA5767HN_3 (9397 750 13531)
Modifications:		<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Modified: Section 3 “Quick reference data” an EMF value remark is added to the header description Added: Figure 3 Modified: Section 13 “Dynamic characteristics” values of $I_{F_{count}}$ changed and EMF value remark is added to the header description Replaced: Figure 11 and Figure 12 Modified: component list of Table 34 updated 		
TEA5767HN_3 (9397 750 13531)	20040920	Product data sheet	-	TEA5767HN_2 (9397 750 12071)
TEA5767HN_2 (9397 750 12071)	20031112	Preliminary specification	-	TEA5767HN_1 (9397 750 09626)
TEA5767HN_1 (9397 750 09626)	20020913	Preliminary specification	-	-

20. Legal information

20.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.semiconductors.philips.com>.

20.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Philips Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Philips Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

20.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, Philips Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — Philips Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Philips Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a Philips Semiconductors product can reasonably be expected

to result in personal injury, death or severe property or environmental damage. Philips Semiconductors accepts no liability for inclusion and/or use of Philips Semiconductors products in such equipment or applications and therefore such inclusion and/or use is for the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — Philips Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.semiconductors.philips.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by Philips Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of Koninklijke Philips Electronics N.V.

21. Contact information

For additional information, please visit: <http://www.semiconductors.philips.com>

For sales office addresses, send an email to: sales.addresses@www.semiconductors.philips.com

22. Contents

1	General description	1	17	Package outline	33
2	Features	1	18	Soldering	34
3	Quick reference data	2	18.1	Introduction to soldering surface mount packages	34
4	Ordering information	3	18.2	Reflow soldering	34
5	Block diagram	4	18.3	Wave soldering	34
6	Pinning information	5	18.4	Manual soldering	35
6.1	Pinning	5	18.5	Package related soldering information	35
6.2	Pin description	5	19	Revision history	37
7	Functional description	6	20	Legal information	38
7.1	Low-noise RF amplifier	6	20.1	Data sheet status	38
7.2	FM mixer	6	20.2	Definitions	38
7.3	VCO	6	20.3	Disclaimers	38
7.4	Crystal oscillator	7	20.4	Trademarks	38
7.5	PLL tuning system	7	21	Contact information	38
7.6	RF AGC	7	22	Contents	39
7.7	IF filter	7			
7.8	FM demodulator	7			
7.9	Level voltage generator and analog-to-digital converter	7			
7.10	IF counter	7			
7.11	Soft mute	7			
7.12	MPX decoder	7			
7.13	Signal dependent mono to stereo blend	8			
7.14	Signal dependent AF response	8			
7.15	Software programmable ports	8			
7.16	I ² C-bus and 3-wire bus	8			
8	I²C-bus, 3-wire bus and bus-controlled functions	10			
8.1	I ² C-bus specification	10			
8.1.1	Data transfer	10			
8.1.2	Power-on reset	11			
8.2	I ² C-bus protocol	11			
8.3	3-wire bus specification	12			
8.3.1	Data transfer	12			
8.3.2	Power-on reset	13			
8.4	Writing data	13			
8.5	Reading data	16			
9	Internal circuitry	17			
10	Limiting values	22			
11	Thermal characteristics	22			
12	Static characteristics	23			
13	Dynamic characteristics	24			
14	FM characteristics	30			
15	I²C-bus characteristics	31			
16	Test information	31			

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© Koninklijke Philips Electronics N.V. 2006. All rights reserved.

For more information, please visit: <http://www.semiconductors.philips.com>.

For sales office addresses, email to: sales.addresses@www.semiconductors.philips.com.

Date of release: 20 February 2006

Document identifier: TEA5767HN_4