

- STRUCTURE                    Silicon Monolithic Integrated Circuit
- NAME OF PRODUCT         DC-AC Inverter Control IC
- TYPE                            **BD9886FV**
- FUNCTION
- 2ch control with Push-Pull
  - Lamp current and voltage sense feed back control
  - Sequencing easily achieved with Soft Start Control
  - Short circuit protection with Timer Latch
  - Under Voltage Lock Out
  - Short circuit protection with over voltage
  - Mode-selectable the operating or stand-by mode by stand-by pin
  - Synchronous operating the other BD9886FV IC' s
  - BURST mode controlled by PWN and DC input

○Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage	Vcc	15	V
Operating Temperature Range	Topr	-40~+90	°C
Storage Temperature Range	Tstg	-55~+125	°C
Power Dissipation	Pd	850*	mW
Maximum Junction Temperature	Tjmax	+125	°C

\*Pd derated at 8.5mW/°C for temperature above Ta = 25°C (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

○Recommended operating condition

Parameter	Symbol	Limits	Unit
Supply voltage	Vcc	5.0~14.0	V
CT oscillation frequency	fct	20~150	kHz
BCT oscillation frequency	fbct	0.05~0.50	kHz

○Electric Characteristics (Ta=25°C, VCC=7V)

Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
((WHOLE DEVICE))						
Operating current	Icc1	—	11.0	17.0	mA	CT=0.5V
Stand-by current	Icc2	—	2	10	μA	
((OVER VOLTAGE DETECT))						
FB over voltage detect voltage	Vovf	2.20	2.40	2.60	V	
((STAND BY CONTROL))						
Stand-by voltage H	VstH	1.6	—	VCC	V	System O N
Stand-by voltage L	VstL	-0.3	—	0.8	V	System O F F
Stand-by hysteresis	ΔVst	0.08	0.18	0.28	V	
((TIMER LATCH))						
Timer Latch voltage	Vcp	1.9	2.0	2.1	V	
Timer Latch current	Icp	0.5	1.0	1.5	μA	
((BURST MODE))						
BOSC Max voltage	VburH	1.94	2.0	2.06	V	f <sub>BCT</sub> =0.2kHz
BOSC Min Voltage	VburL	0.4	0.5	0.6	V	f <sub>BCT</sub> =0.2kHz
BOSC constant current	IBCT	1.35/BRT	1.5/BRT	1.65/BRT	A	
OSC constant current	fBCT	266	280	294	Hz	BRT=33kΩ, BCT=0.050μF
((OSC BLOCK))						
BOSC constant current	Ict	1.35/RT	1.5/RT	1.65/RT	A	
OSC Max voltage	Vosch	1.8	2.0	2.2	V	f <sub>ct</sub> =60kHz
OSC Min voltage	Voscl	0.3	0.5	0.7	V	f <sub>ct</sub> =60kHz
MAX DUTY	MAXDUTY	44	46.5	49	%	f <sub>ct</sub> =60kHz
Soft start current	I <sub>ss</sub>	1.0	2.0	3.0	μA	
IS COMP detect Voltage	V <sub>isc</sub>	0.45	0.50	0.55	V	
SS COMP detect voltage	V <sub>ss</sub>	2.0	2.2	2.4	V	
SRT ON resistance	RSRT	—	200	400	Ω	
((UVLO BLOCK))						
Operating voltage	V <sub>uvloH</sub>	4.100	4.300	4.500	V	
Shut down voltage	V <sub>uvloL</sub>	3.900	4.100	4.300	V	
Operating voltage (External UVLO)	V <sub>uvlo1</sub>	2.160	2.220	2.280	V	
Lock out voltage (External UVLO)	V <sub>uvlo2</sub>	2.242	2.315	2.388	V	
Hysteresis width	ΔV <sub>uvlo</sub>	0.068	0.095	0.122	V	
((REG BLOCK))						
REG output voltage	V <sub>REG</sub>	3.038	3.100	3.162	V	
REG source current	I <sub>REG</sub>	5.0	—	—	mA	
VREF voltage	V <sub>ref</sub>	1.225	1.250	1.275	V	V <sub>REF</sub> =Open
((FEED BACK BLOCK))						
IS threshold voltage	V <sub>is</sub>	1.225	1.250	1.275	V	V <sub>REF</sub> =Open
VS threshold voltage	V <sub>vs</sub>	1.220	1.250	1.280	V	
IS source current 1	I <sub>is1</sub>	—	—	1.5	μA	DUTY=2.0V
IS source current 2	I <sub>is2</sub>	13.0	20.0	27.0	μA	DUTY=0V, IS=0.5V
VS source current	I <sub>vs</sub>	—	—	1.0	μA	
((OUTPUT BLOCK))						
NAch output voltage H	V <sub>outNAH</sub>	VCC-0.3	VCC-0.1	—	V	
NBch output voltage H	V <sub>outNBH</sub>	VCC-0.3	VCC-0.1	—	V	
NAch output voltage L	V <sub>outNAL</sub>	—	0.1	0.3	V	
NBch output voltage L	V <sub>outNBL</sub>	—	0.1	0.3	V	
NAch output sink resistance	R <sub>sinkNA</sub>	—	5	10	Ω	
NAch output source resistance	R <sub>sourceNA</sub>	—	8	16	Ω	
NBch output sink resistance	R <sub>sinkNB</sub>	—	5	10	Ω	
NBch output source resistance	R <sub>sourceNB</sub>	—	8	16	Ω	
Drive output frequency	f <sub>out</sub>	58.5	60.0	61.5	KHz	RT=18kΩ, CT=400pF
((COMP BLOCK))						
Under voltage detect	V <sub>COMPL</sub>	0.620	0.640	0.660	V	
((PROTECT CLOCK))						
Normal output voltage	V <sub>PH</sub>	2.9	3.1	3.3	V	
Protect output voltage	V <sub>PL</sub>	—	—	0.5	V	

(This product is not designed for normal operation with in a radio active environment.)



○NOTE FOR USE

1. When designing the external circuit, including adequate margins for variation between external devices and the IC. Use adequate margins for steady state and transient characteristics.
2. Recommended Operating Range  
The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however, the variation will be small.
3. Mounting Failures  
Mounting failures, such as misdirection or miscounts, may harm the device.
4. Electromagnetic Fields  
A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within  $\pm 0.3V$  compared with the PGND pin
6. BD9886FV has the short circuit protection with Thermal Shut Down System. When STB or Vcc pin re-supplied, They enables to cancel the latch. If It rise the temperature of the chip more than 170°C (TYP). It make the external FET OFF
7. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
9. On operating Slow Start Control (SS is less than 2.2V), It does not operate Timer Latch.
10. By STB voltage, BD9886FV is changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state (0.8~1.6).
11. The pin connected a connector need to connect to the resistor for electrical surge destruction.
12. This IC is a monolithic IC which (as shown is Fig-1)has P<sup>+</sup> substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows.
  - (When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)
  - (When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND(P substrate)voltage to an input pin.

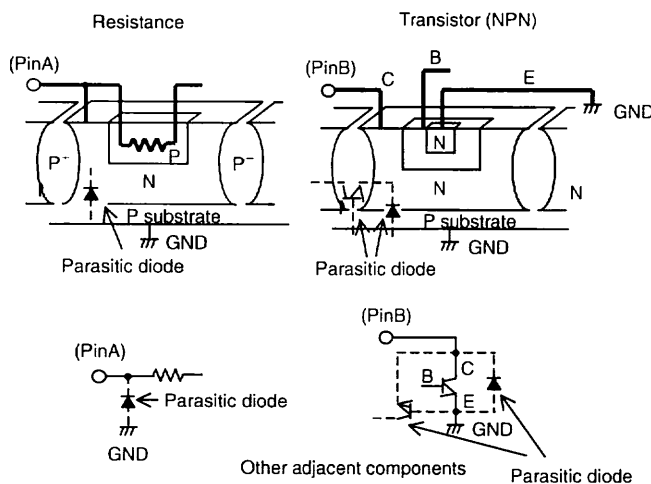


図-1 Simplified structure of a Bipolar IC

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