



## PRODUCT PREVIEW

**Product Part#: LPSF096064A00-T3**

**Product Name: 65K color OLED Module**

**Revision: 4.0**

**Date: Oct'2004**



## REVISION RECORD

Revision	Description of Revision	Revision date	Remark
0.0	Initial release	3-Jun-04	--
1.0	1) Changed "Dimensional outline" drawing	14-Jun-04	
2.0	1) Added the application circuit for using external DC/DC converter and its component list 2) Updated the component value of application circuit 3) Updated the "Quality Specification"	16-Aug-04	
3.0	1) Updated pin description of D0 and D1 for SPI mode 2) Changed SCLK (D6) to SCLK (D0) and SDIN (D7) to SDIN (D1) in SPI timing diagram	20-Aug-04	
4.0	1) Updated "Dot Size" in Mechanical specifications section 2) Updated the component value of application circuit	27-Oct-04	



---

## TABLE OF CONTENTS

<b>1. Functions &amp; features</b>	<b>1</b>
<b>2. Mechanical specifications</b>	<b>1</b>
<b>3. Block diagram</b>	<b>1</b>
<b>4. Dimensional outline</b>	<b>2</b>
<b>5. Pin description</b>	<b>3</b>
<b>6. Absolute maximum ratings</b>	<b>4</b>
<b>7. Optics &amp; electrical characteristics</b>	<b>4</b>
<b>8. Electrical characteristics</b>	<b>5</b>
<b>9. Control and display command</b>	<b>9</b>
<b>10. Reference application circuit</b>	<b>12</b>
<b>11. Quality specifications</b>	<b>16</b>

## 1. FUNCTIONS & FEATURES

1.1. Format	: 96(RGB)*64 dots
1.2. Display mode	: Passive Matrix
1.3. Display color	: 65k color
1.4. Duty	: 1/64

## 2. MECHANICAL SPECIFICATIONS

2.1. Module size	: 28.70mm(W)*32.99mm(H)
2.2. Panel size	: 28.70mm(W)*20.40mm(H)
2.3. Viewing area	: 23.312mm(W)*14.848mm(H)
2.4. Active area	: 21.286mm(W)*14.178mm(H)
2.5. Dot pitch	: 0.222mm(W)*0.222mm(H)
2.6. Dot size	: 0.196mm(W)*0.192mm(H)
2.7. Thickness(with polarizer)	: 1.70mm
2.8. Weight	: TBD

## 3. BLOCK DIAGRAM

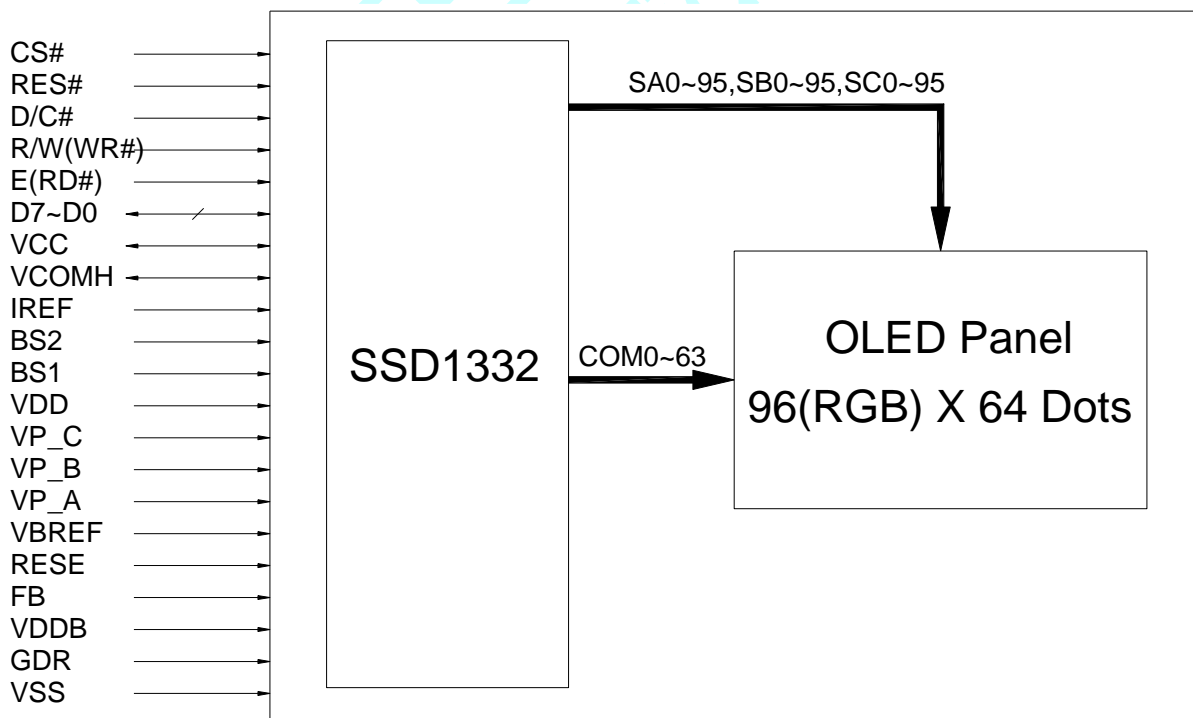


Figure 1. Block diagram

# 4. DIMENSIONAL OUTLINE

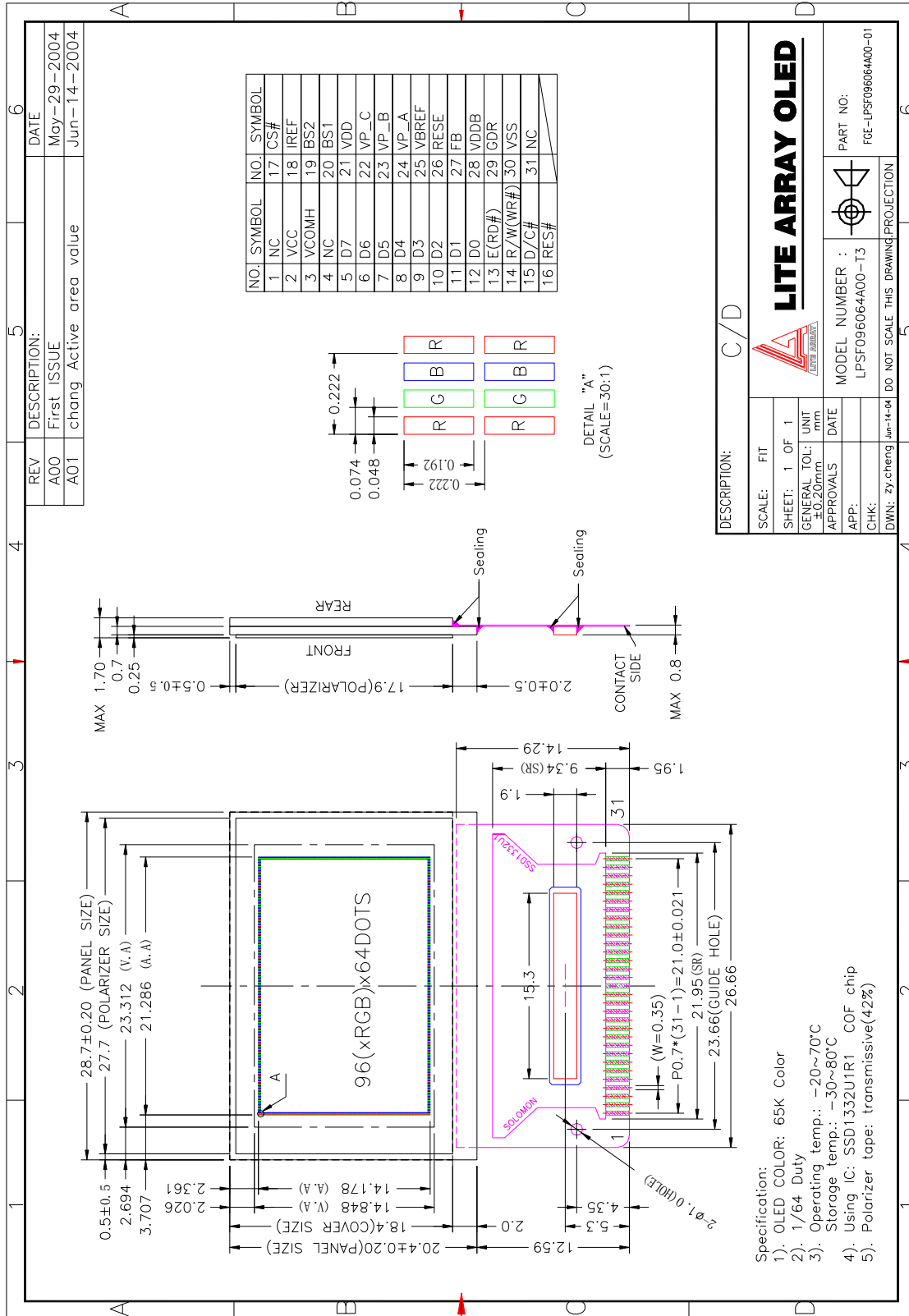


Figure 2. Dimensional outline



## 5. PIN DESCRIPTION

Pin no.	Symbol	Function												
1,4,31	NC	These are reserved pins and should not be connected. Do not group or short NC pins.												
2	VCC	Supply voltage for OLED This is the most positive voltage supply pin of the chip. It is supplied either by external high voltage source or internal booster.												
3	VCOMH	This pin is the input pin for the voltage output high level for COM signals. It can be supplied externally or internally. When VCOMH is generated internally, a capacitor should be connected between this pin and VSS.												
5~12	D7~D0	These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D1 will be the serial data input and D0 will be the serial clock input.												
13	E(RD#)	This pin is MCU interface input. <ul style="list-style-type: none"> <li>When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected.</li> <li>When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and the chip is selected.</li> <li>When serial interface is selected, this pin E(RD#) must be connected to VSS.</li> </ul>												
14	R/W(WR#)	This pin is MCU interface input. <ul style="list-style-type: none"> <li>When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.</li> <li>When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the chip is selected.</li> <li>When serial interface is selected, this pin RW#(WR#) must be connected to VSS.</li> </ul>												
15	D/C#	This pin is Data/Command control pin. <ul style="list-style-type: none"> <li>When the pin is pulled high, the data at D7-D0 is treated as display data.</li> <li>When the pin is pulled low, the data at D7-D0 will be transferred to the command register.</li> </ul>												
16	RES#	This pin is reset signal input. When the pin is low, initialization of the chip is executed.												
17	CS#	This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.												
18	IREF	This pin is the segment output current reference pin. A resistor should be connected between this pin and VSS.												
19,20	BS2,BS1	These input pins are used to configure MCU interface selection by appropriate logic setting, which is described in the following table: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th>6800-parallel interface (8 bit)</th> <th>8080-parallel interface (8 bit)</th> <th>Serial interface</th> </tr> </thead> <tbody> <tr> <td>BS1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>BS2</td> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>		6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	Serial interface	BS1	0	1	0	BS2	1	1	0
	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	Serial interface											
BS1	0	1	0											
BS2	1	1	0											

Pin no.	Symbol	Function
21	VDD	Power Supply pin for logic operation of the driver. It must be connected to external source.
22,23,24	VP_C VP_B VP_A	These pins are the pre-charge driving voltages for OLED driving segment pins SA0-SA95, SB0-SB95 and SC0-SC95 respectively. They can be supplied externally or internally generated by VP circuit. When internal VP is used, VP_A, VP_B, VP_C pins should be left open.
25	VBREF	This pin is the internal voltage reference of booster circuit. A stabilization capacitor should be connected between VBREF and VSS. When use external VCC, the pin should be left open.
26	RESE	This pin connects to the source current pin of the external NMOS of the booster circuit. When use external VCC, the pin should be left open.
27	FB	This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level (VCC). When use external VCC, the pin should be left open.
28	VDDDB	This is the power supply pin for the internal buffer of the DC-DC voltage converter. When use external VCC, the pin should be left open.
29	GDR	This output pin drives the gate of the external NMOS of the booster circuit. When use external VCC, the pin should be left open.
30	VSS	Ground pin. It must be connected to external ground.

**Table1: Pin Description**

## **6. ABSOLUTE MAXIMUM RATINGS**

### **6.1 Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage	V <sub>DD</sub>	-0.3	4.0	V	1,2
	V <sub>CC</sub>	0	18	V	1,2
	V <sub>REF</sub>	0	18	V	1,2
Supply Voltage/Output voltage	V <sub>COMH</sub>	0	16	V	1,2
SEG/COM output voltage	-	0	16	V	1,2
Input voltage	V <sub>in</sub>	V <sub>SS</sub> -0.3	V <sub>DD</sub> +0.3	V	1,2
Operating Temperature	T <sub>OP</sub>	-20	70	°C	--
Storage Temperature	T <sub>STG</sub>	-30	80	°C	--

**Table2: Absolute Maximum Ratings**

Note 1: All above voltages are on the basis of "V<sub>SS</sub> = 0.0V".

Note 2: When this module is used beyond above absolute maximum ratings, permanent damage of the module may occur. For normal operations, it should be restricted to the limits in the Electrical Characteristics Tables. If the module is used beyond these limits, malfunctioning will occur and the reliability of the module may deteriorate.

## 7. OPTICS & ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit	
Brightness(White)	L <sub>br</sub>	Display average (With polarizer)	30	50	70	Cd/m <sup>2</sup>	
CIE (Blue)	X	With polarizer	0.10	0.15	0.20	--	
	Y		0.12	0.17	0.22	--	
CIE (Green)	X		0.23	0.28	0.33	--	
	Y		0.58	0.63	0.68	--	
CIE (Red)	X		0.57	0.62	0.67	--	
	Y		0.32	0.37	0.42	--	
CIE (White)	X		0.24	0.29	0.34	--	
	Y		0.27	0.32	0.37	--	
Dark Room Contrast	CR			200	--	--	--
View Angle	A		--	>160	--	--	degree

Table 3: Optics & electrical characteristics

## 8. ELECTRICAL CHARACTERISTICS

### 8.1 DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub>	Operating Voltage		-	16	-	V
V <sub>DD</sub>	Logic Supply Voltage		2.4	2.7	3.5	V
V <sub>OH</sub>	High Logic Output Level	I <sub>out</sub> =100uA, 3.3MHz	0.9V <sub>DD</sub>	-	V <sub>DD</sub>	V
V <sub>OL</sub>	Low Logic Output Level	I <sub>out</sub> =100uA, 3.3MHz	0	-	0.1V <sub>D</sub> D	V
V <sub>IH</sub>	High Logic Input Level	I <sub>out</sub> =100uA, 3.3MHz	0.8V <sub>DD</sub>	-	V <sub>DD</sub>	V
V <sub>IL</sub>	Low Logic Input Level	I <sub>out</sub> =100uA, 3.3MHz	0	-	0.2V <sub>D</sub> D	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	V <sub>DD</sub> =2.7V, Display ON Contrast =FF, No panel attached	-	770	-	uA
I <sub>DD</sub>	V <sub>DD</sub> Supply Current	V <sub>DD</sub> =2.7V, Display ON Contrast =FF, No panel attached	-	170	-	uA
I <sub>fc</sub>	Forward current	All pixel on	-	12	-	mA
Pwr	Power consumption	30% ON, 50Cd/m <sup>2</sup>	-	100 (under)	-	mW

Table 4: DC characteristics



## 8.2 Characteristics

### 8.2.1 6800-Series MPU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Max	Unit
$t_{\text{cycle}}$	Clock cycle time	300	--	ns
$t_{\text{AS}}$	Address Setup Time	0	--	ns
$t_{\text{AH}}$	Address Hold Time	0	--	ns
$t_{\text{DSW}}$	Write Data Setup Time	40	--	ns
$t_{\text{DHW}}$	Write Data Hold Time	15	--	ns
$t_{\text{DHR}}$	Read Data Hold Time	20	--	ns
$t_{\text{OH}}$	Output Disable Time	--	70	ns
$t_{\text{ACC}}$	Access Time	--	140	ns
$PW_{\text{CSL}}$	Chip Select Low Pulse Width (read)	120	--	ns
	Chip Select Low Pulse Width (write)	60	--	ns
$PW_{\text{CSH}}$	Chip Select High Pulse Width (read)	60	--	ns
	Chip Select High Pulse Width (write)	60	--	ns
$t_{\text{R}}$	Rise time	--	15	ns
$t_{\text{F}}$	Fall time	--	15	ns

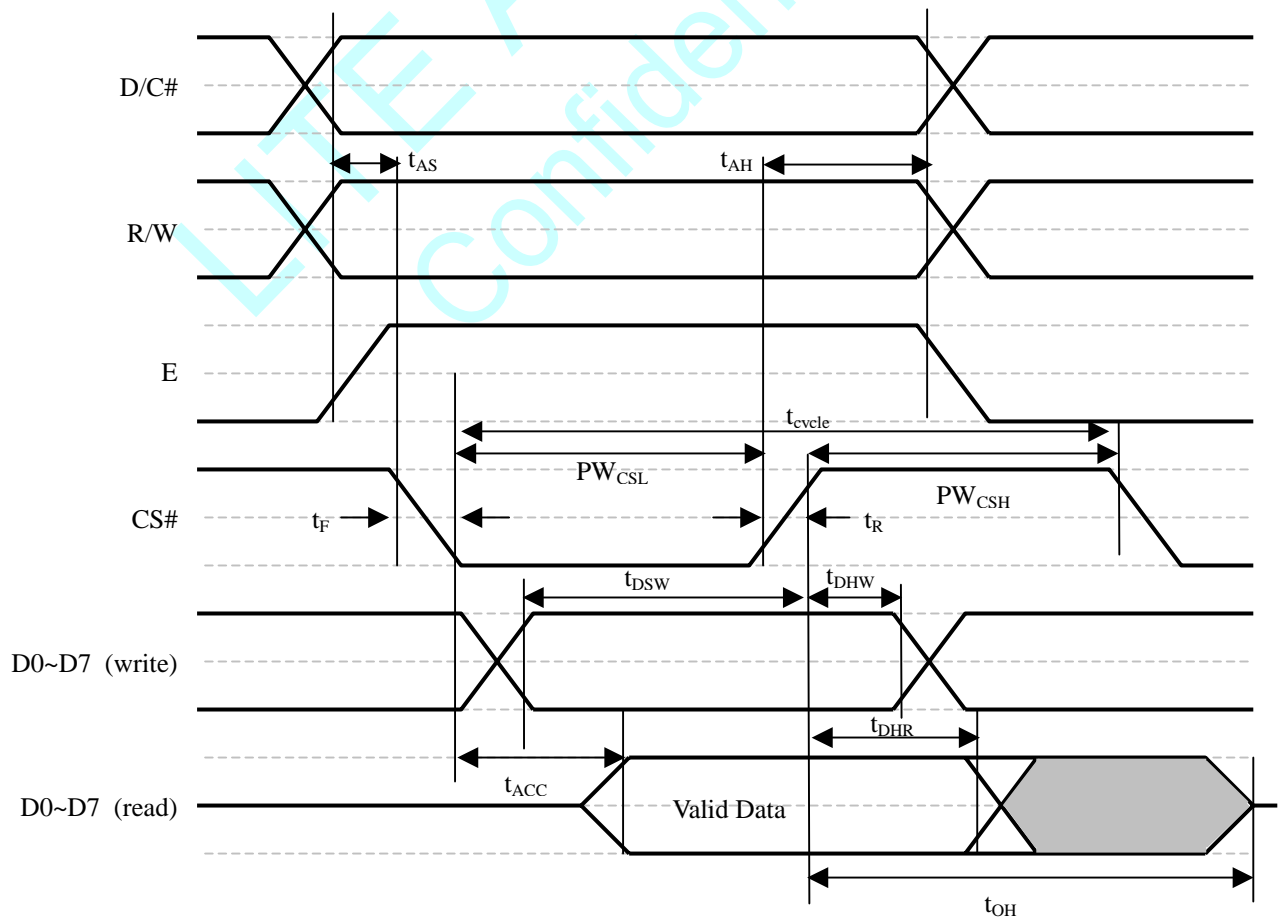


Figure 3: Timing diagram for 6800-series MPU parallel interface

### 8.2.2 8080-Series MPU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Max	Unit
$t_{\text{cycle}}$	Clock cycle time	300	--	ns
$t_{\text{AS}}$	Address Setup Time	0	--	ns
$t_{\text{AH}}$	Address Hold Time	0	--	ns
$t_{\text{DSW}}$	Write Data Setup Time	40	--	ns
$t_{\text{DHW}}$	Write Data Hold Time	15	--	ns
$t_{\text{DHR}}$	Read Data Hold Time	20	--	ns
$t_{\text{OH}}$	Output Disable Time	--	70	ns
$t_{\text{ACC}}$	Access Time	--	140	ns
$PW_{\text{CSL}}$	Chip Select Low Pulse Width (read)	120	--	ns
	Chip Select Low Pulse Width (write)	60	--	ns
$PW_{\text{CSH}}$	Chip Select High Pulse Width (read)	60	--	ns
	Chip Select High Pulse Width (write)	60	--	ns
$t_{\text{R}}$	Rise time	--	15	ns
$t_{\text{F}}$	Fall time	--	15	ns

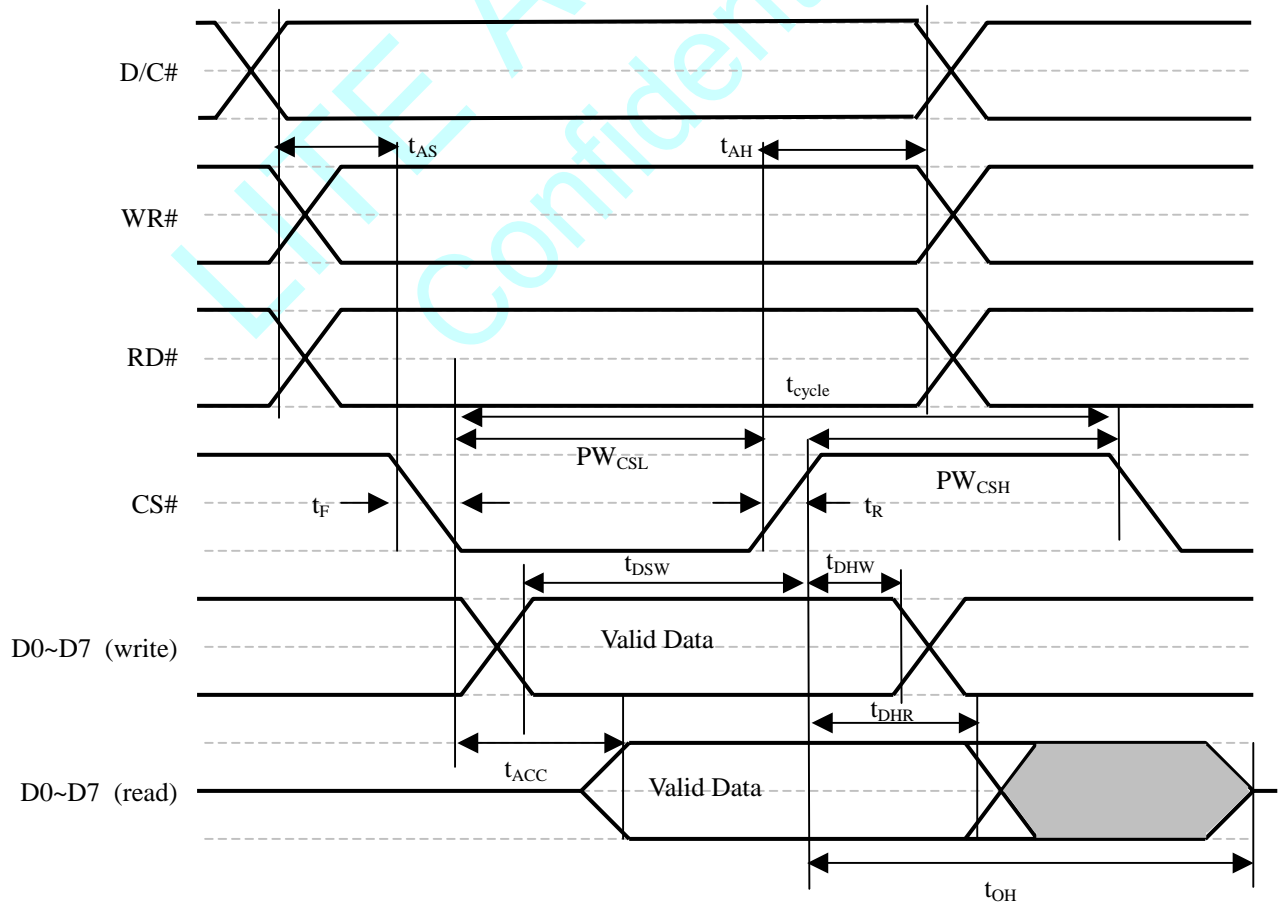


Figure4: Timing diagram for 8080-series MPU parallel interface

### 8.2.3 Serial Interface Timing Characteristics

Symbol	Parameter	Min	Max	Unit
$t_{cycle}$	Clock cycle time	250	--	ns
$t_{AS}$	Address Setup Time	150	--	ns
$t_{AH}$	Address Hold Time	150	--	ns
$t_{CSS}$	Chip Select Setup Time	120	--	ns
$t_{CSH}$	Chip Select Hold Time	60	--	ns
$t_{DSW}$	Write Data Setup Time	100	--	ns
$t_{DHW}$	Write Data Hold Time	100	--	ns
$t_{CLKL}$	Clock Low Time	100	--	ns
$t_{CLKH}$	Clock High Time	100	--	ns
$t_R$	Rise time	--	15	ns
$t_F$	Fall time	--	15	ns

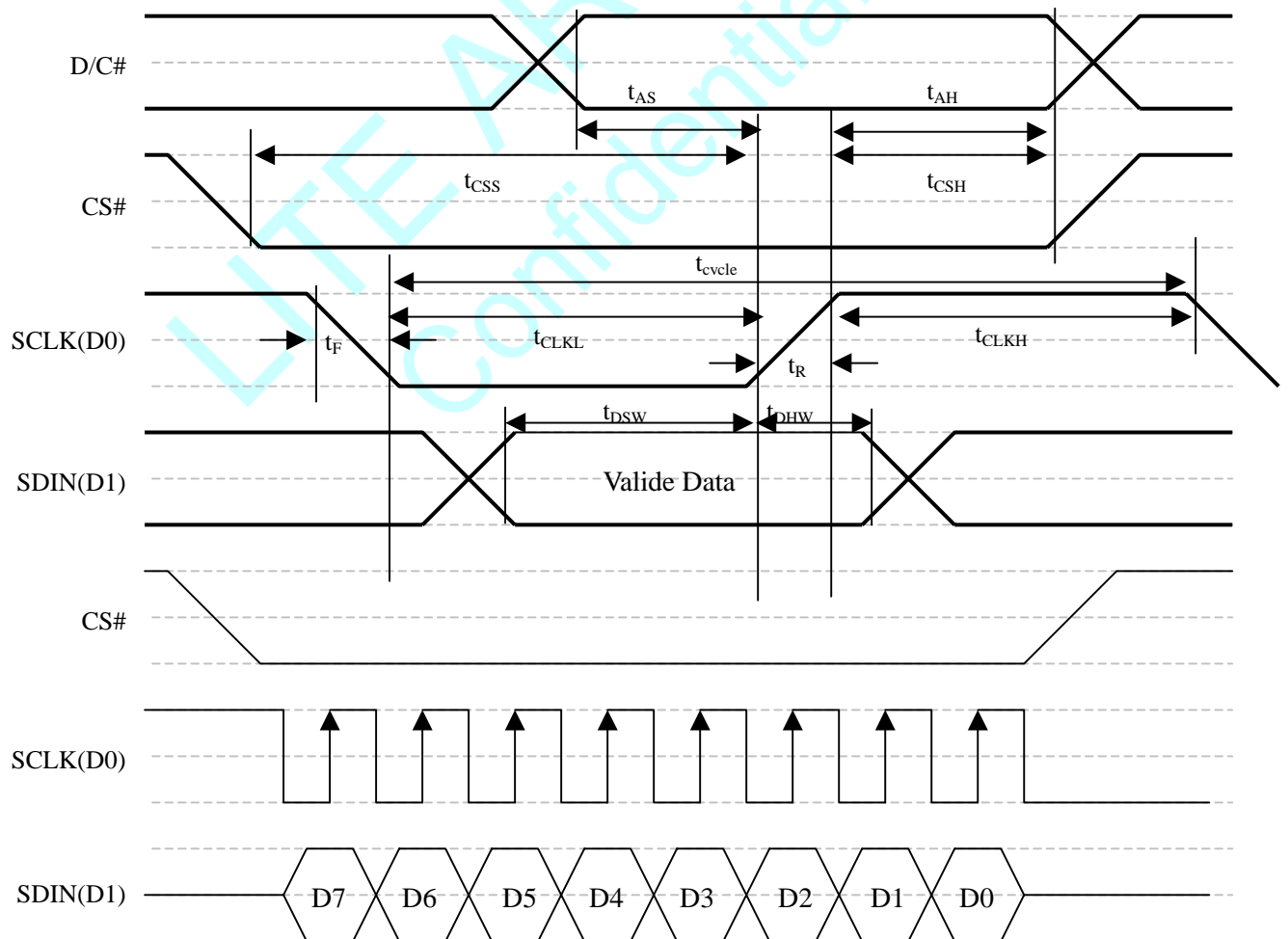


Figure 5: Timing diagram for serial interface



## 9. CONTROL AND DISPLAY COMMAND

### 9.1 Configuration Command Table

(To write commands to command registers, the MCU interface pins are set as: D/C = 0, R/W(WR#) = 0, E(RD#)=1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0	15 A[6:0] B[6:0]	0 * *	0 A <sub>6</sub> B <sub>6</sub>	0 A <sub>5</sub> B <sub>5</sub>	1 A <sub>4</sub> B <sub>4</sub>	0 A <sub>3</sub> B <sub>3</sub>	1 A <sub>2</sub> B <sub>2</sub>	0 A <sub>1</sub> B <sub>1</sub>	1 A <sub>0</sub> B <sub>0</sub>	Set Column Address	A[6:0] sets the column start address from 0-95, POR=00d. B[6:0] sets the column end address from 0-95 POR=95d.
0 0 0	75 A[5:0] B[5:0]	0 * *	1 * *	1 A <sub>5</sub> B <sub>5</sub>	1 A <sub>4</sub> B <sub>4</sub>	0 A <sub>3</sub> B <sub>3</sub>	1 A <sub>2</sub> B <sub>2</sub>	0 A <sub>1</sub> B <sub>1</sub>	1 A <sub>0</sub> B <sub>0</sub>	Set Row Address	A[5:0] sets the row start address from 0-63, POR=00d. B[5:0] sets the row end address from 0-63, POR=63d.
0 0	81 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	0 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Contrast for Color A (Segment Pins :SA0 – SA95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. POR = 80H
0 0	82 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	0 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	0 A <sub>0</sub>	Set Contrast for Color B (Segment Pins :SB0 – SB95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. POR = 80H
0 0	83 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	0 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	1 A <sub>0</sub>	Set Contrast for Color C (Segment Pins :SC0 – SC95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. POR = 80H
0 0	87 A[3:0]	1 *	0 *	0 *	0 *	0 A <sub>3</sub>	1 A <sub>2</sub>	1 A <sub>1</sub>	1 A <sub>0</sub>	Master Current Control	Set A[3:0] from 0000, 0001... to 1111 to adjust the master current attenuation factor from 1/16, 2/16... to 16/16. POR =1111b,for no attenuation.
0 0	A0 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	1 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	0 A <sub>0</sub>	Set Re-map & Data Format	A[0]=0, Horizontal address increment (POR) A[0]=1, Vertical address increment  A[1]=0, Column address 0 is mapped to SEG0 (POR) A[1]=1, Column address 95 is mapped to SEG0  A[4]=0, Scan from COM 0 to COM [N –1] A[4]=1, Scan from COM [N-1] to COM0. Where N is the Multiplex ratio.  A[5]=0, Disable COM Split Odd Even (POR) A[5]=1, Enable COM Split Odd Even  A[7:6]=00; 256 color format =01; 65k color format(POR)
0 0	A1 A[5:0]	1 *	0 *	1 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Display Start Line	Set display RAM display start line register from 0-63.  Display start line register is reset to 00H after POR.
0 0	A2 A[5:0]	1 *	0 *	1 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	0 A <sub>0</sub>	Set Display Offset	Set vertical scroll by COM from 0-63.  The value is reset to 00H after POR.
0	A4~A7	1	0	1	0	0	1	X <sub>1</sub>	X <sub>0</sub>	Set Display Mode	A4h=Normal Display (POR) A5h=Entire Display On, all pixels turn on at GS level 63 A6h=Entire Display Off, all pixels turn off A7h=Inverse Display
0 0	A8 A[5:0]	1 *	0 *	1 A <sub>5</sub>	0 A <sub>4</sub>	1 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	0 A <sub>0</sub>	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-64MUX, POR=63d (64MUX) A[5:0]=0-14d (invalid entry)
0 0	AD A[7:0]	1 1	0 0	1 0	0 0	1 0	1 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Master Configuration	A[0]=0, Select external VCC supply at Display ON A[0]=1, Select internal booster at Display ON (POR)  A[1]=0, Select external VCOMH voltage supply at Display ON A[1]=1, Select internal VCOMH regulator at Display ON (POR)  A[2]=0, Select External VP voltage supply A[2]=1, Select Internal VP (POR)
0	AE~AF	1	0	1	0	X <sub>3</sub>	1	1	1	Set Display On/Off	A Eh=Display off (POR) A Fh=Display on





## 9.2 Graphic Acceleration Command Set Table

(To write commands to command registers, the MCU interface pins are set as: D/C = 0, R/W(WR#)=0, E(RD#)=1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0 0 0 0 0 0	21 A[6:0] B[5:0] C[6:0] D[5:0] E[5:1] F[5:0] G[5:1]	0 * * * * * * *	0 A <sub>6</sub> * C <sub>6</sub> * * * *	1 A <sub>5</sub> B <sub>5</sub> C <sub>5</sub> D <sub>5</sub> E <sub>5</sub> F <sub>5</sub> G <sub>5</sub>	0 A <sub>4</sub> B <sub>4</sub> C <sub>4</sub> D <sub>4</sub> E <sub>4</sub> F <sub>4</sub> G <sub>4</sub>	0 A <sub>3</sub> B <sub>3</sub> C <sub>3</sub> D <sub>3</sub> E <sub>3</sub> F <sub>3</sub> G <sub>3</sub>	0 A <sub>2</sub> B <sub>2</sub> C <sub>2</sub> D <sub>2</sub> E <sub>2</sub> F <sub>2</sub> G <sub>2</sub>	0 A <sub>1</sub> B <sub>1</sub> C <sub>1</sub> D <sub>1</sub> E <sub>1</sub> F <sub>1</sub> G <sub>1</sub>	1 A <sub>0</sub> B <sub>0</sub> C <sub>0</sub> D <sub>0</sub> * F <sub>0</sub> *	Draw Line	A[6:0] : Column Address of Start B[5:0] : Row Address of Start C[6:0] : Column Address of End D[5:0] : Row Address of End E[5:1] : Color C of the line F[5:0] : Color B of the line G[5:1] : Color A of the line
0 0 0 0 0 0 0 0 0 0 0	22 A[6:0] B[5:0] C[6:0] D[5:0] E[5:1] F[5:0] G[5:1] H[5:1] I[5:0] J[5:1]	0 * * * * * * * * * *	0 A <sub>6</sub> * C <sub>6</sub> * * * * * * *	1 A <sub>5</sub> B <sub>5</sub> C <sub>5</sub> D <sub>5</sub> E <sub>5</sub> F <sub>5</sub> G <sub>5</sub> H <sub>5</sub> I <sub>5</sub> J <sub>5</sub>	0 A <sub>4</sub> B <sub>4</sub> C <sub>4</sub> D <sub>4</sub> E <sub>4</sub> F <sub>4</sub> G <sub>4</sub> H <sub>4</sub> I <sub>4</sub> J <sub>4</sub>	0 A <sub>3</sub> B <sub>3</sub> C <sub>3</sub> D <sub>3</sub> E <sub>3</sub> F <sub>3</sub> G <sub>3</sub> H <sub>3</sub> I <sub>3</sub> J <sub>3</sub>	0 A <sub>2</sub> B <sub>2</sub> C <sub>2</sub> D <sub>2</sub> E <sub>2</sub> F <sub>2</sub> G <sub>2</sub> H <sub>2</sub> I <sub>2</sub> J <sub>2</sub>	1 A <sub>1</sub> B <sub>1</sub> C <sub>1</sub> D <sub>1</sub> E <sub>1</sub> F <sub>1</sub> G <sub>1</sub> H <sub>1</sub> I <sub>1</sub> J <sub>1</sub>	0 A <sub>0</sub> B <sub>0</sub> C <sub>0</sub> D <sub>0</sub> * F <sub>0</sub> * * * *	Drawing Rectangle	A[6:0] : Column Address of Start B[5:0] : Row Address of Start C[6:0] : Column Address of End D[5:0] : Row Address of End E[5:1] : Color C of the line F[5:0] : Color B of the line G[5:1] : Color A of the line H[5:1] : Color C of the fill area I[5:0] : Color B of the fill area J[5:1] : Color A of the fill area
0 0 0 0 0 0 0	23 A[6:0] B[5:0] C[6:0] D[5:0] E[6:0] F[5:0]	0 * * * * * *	0 A <sub>6</sub> * C <sub>6</sub> * * *	1 A <sub>5</sub> B <sub>5</sub> C <sub>5</sub> D <sub>5</sub> E <sub>5</sub> F <sub>5</sub>	0 A <sub>4</sub> B <sub>4</sub> C <sub>4</sub> D <sub>4</sub> E <sub>4</sub> F <sub>4</sub>	0 A <sub>3</sub> B <sub>3</sub> C <sub>3</sub> D <sub>3</sub> E <sub>3</sub> F <sub>3</sub>	0 A <sub>2</sub> B <sub>2</sub> C <sub>2</sub> D <sub>2</sub> E <sub>2</sub> F <sub>2</sub>	1 A <sub>1</sub> B <sub>1</sub> C <sub>1</sub> D <sub>1</sub> E <sub>1</sub> F <sub>1</sub>	1 A <sub>0</sub> B <sub>0</sub> C <sub>0</sub> D <sub>0</sub> E <sub>0</sub> F <sub>0</sub>	Copy	A[6:0] : Column Address of Start B[5:0] : Row Address of Start C[6:0] : Column Address of End D[5:0] : Row Address of End E[6:0] : Column Address of New Start F[5:0] : Row Address of New Start
0 0 0 0	24 A[6:0] B[5:0] C[6:0] D[5:0]	0 * * *	0 A <sub>6</sub> * C <sub>6</sub> *	1 A <sub>5</sub> B <sub>5</sub> C <sub>5</sub> D <sub>5</sub>	0 A <sub>4</sub> B <sub>4</sub> C <sub>4</sub> D <sub>4</sub>	0 A <sub>3</sub> B <sub>3</sub> C <sub>3</sub> D <sub>3</sub>	1 A <sub>2</sub> B <sub>2</sub> C <sub>2</sub> D <sub>2</sub>	0 A <sub>1</sub> B <sub>1</sub> C <sub>1</sub> D <sub>1</sub>	0 A <sub>0</sub> B <sub>0</sub> C <sub>0</sub> D <sub>0</sub>	Dim Window	A[6:0] : Column Address of Start B[5:0] : Row Address of Start C[6:0] : Column Address of End D[5:0] : Row Address of End The effect of dim window: GS15~GS0 no change GS19~GS16 become GS4 GS23~GS20 become GS5 ... GS63~GS60 become GS15
0 0 0 0	25 A[6:0] B[5:0] C[6:0] D[5:0]	0 * * *	0 A <sub>6</sub> * C <sub>6</sub> *	1 A <sub>5</sub> B <sub>5</sub> C <sub>5</sub> D <sub>5</sub>	0 A <sub>4</sub> B <sub>4</sub> C <sub>4</sub> D <sub>4</sub>	0 A <sub>3</sub> B <sub>3</sub> C <sub>3</sub> D <sub>3</sub>	1 A <sub>2</sub> B <sub>2</sub> C <sub>2</sub> D <sub>2</sub>	0 A <sub>1</sub> B <sub>1</sub> C <sub>1</sub> D <sub>1</sub>	1 A <sub>0</sub> B <sub>0</sub> C <sub>0</sub> D <sub>0</sub>	Clear Window	A[6:0] : Column Address of Start B[5:0] : Row Address of Start C[6:0] : Column Address of End D[5:0] : Row Address of End
0 0	26 A[4:0]	0 *	0 *	1 *	0 A <sub>4</sub>	0 0	1 0	1 0	0 A <sub>0</sub>	Fill Enable / Disable	A0 0 : Disable Fill for Draw Rectangle Command (POR) 1 : Enable Fill for Draw Rectangle Command A[3:1] 000 : Reserved values A4 0 : Disable reverse copy (POR) 1 : Enable reverse during copy command.

Table 6: Graphic Acceleration Command Set Table

### 9.3 Read Command Table

(D/C=0, R/W (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

Bit Pattern	Command	Description
D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub> D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>	Status Register Read *	D <sub>7</sub> : "1" for Command lock D <sub>6</sub> : "1" for display OFF / "0" for display ON D <sub>5</sub> : Reserve D <sub>4</sub> : Reserve D <sub>3</sub> : Reserve D <sub>2</sub> : Reserve D <sub>1</sub> : Reserve D <sub>0</sub> : Reserve

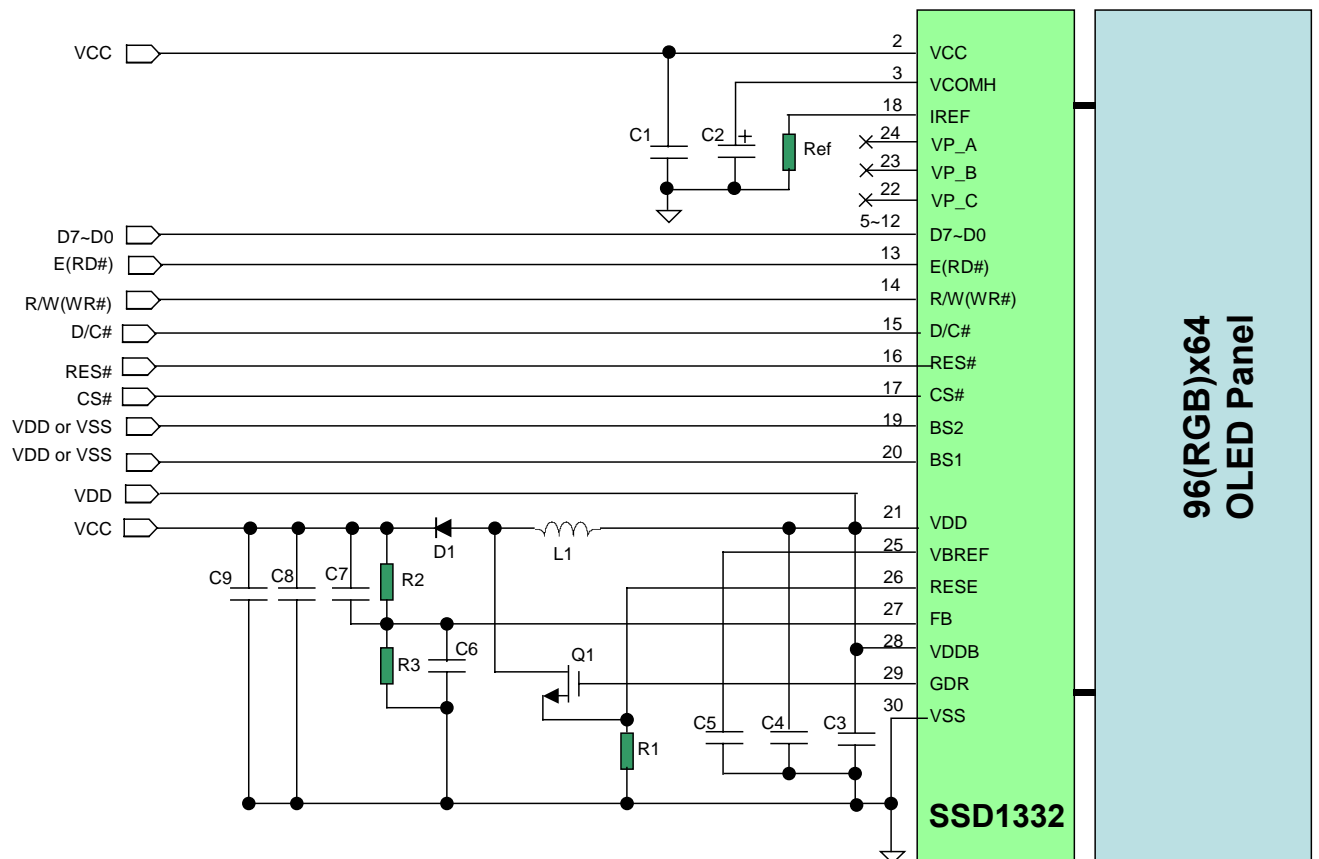
**Table 7: Read Command Table**

Note:

1.Remark "\*" stands for "Don't Care"

2.Patterns other than that given in Command Table are prohibited to enter to the chip as a command; otherwise, unexpected result will occur.

## 10. REFERENCE APPLICATION CIRCUIT



**Figure 6: Reference Application Circuit (using internal DC/DC voltage converter)**

Notes:

- MPU interface: 8-bit 6800-series/8080-series parallel interface or Serial interface. It is pin selectable by BS1 and BS2.

	6800-series parallel interface	8080-series parallel interface	Serial interface
BS1	0	1	0
BS2	1	1	0

- L1, D1, Q1 and C4 should be grouped closed together on PCB layout
- R2, R3, C5 and C6 should be grouped closed together on PCB layout
- The VCC output voltage level is adjusted by R2 and R3, the formula is:

$$VCC = 1.2 \times (R2+R3)/R3$$

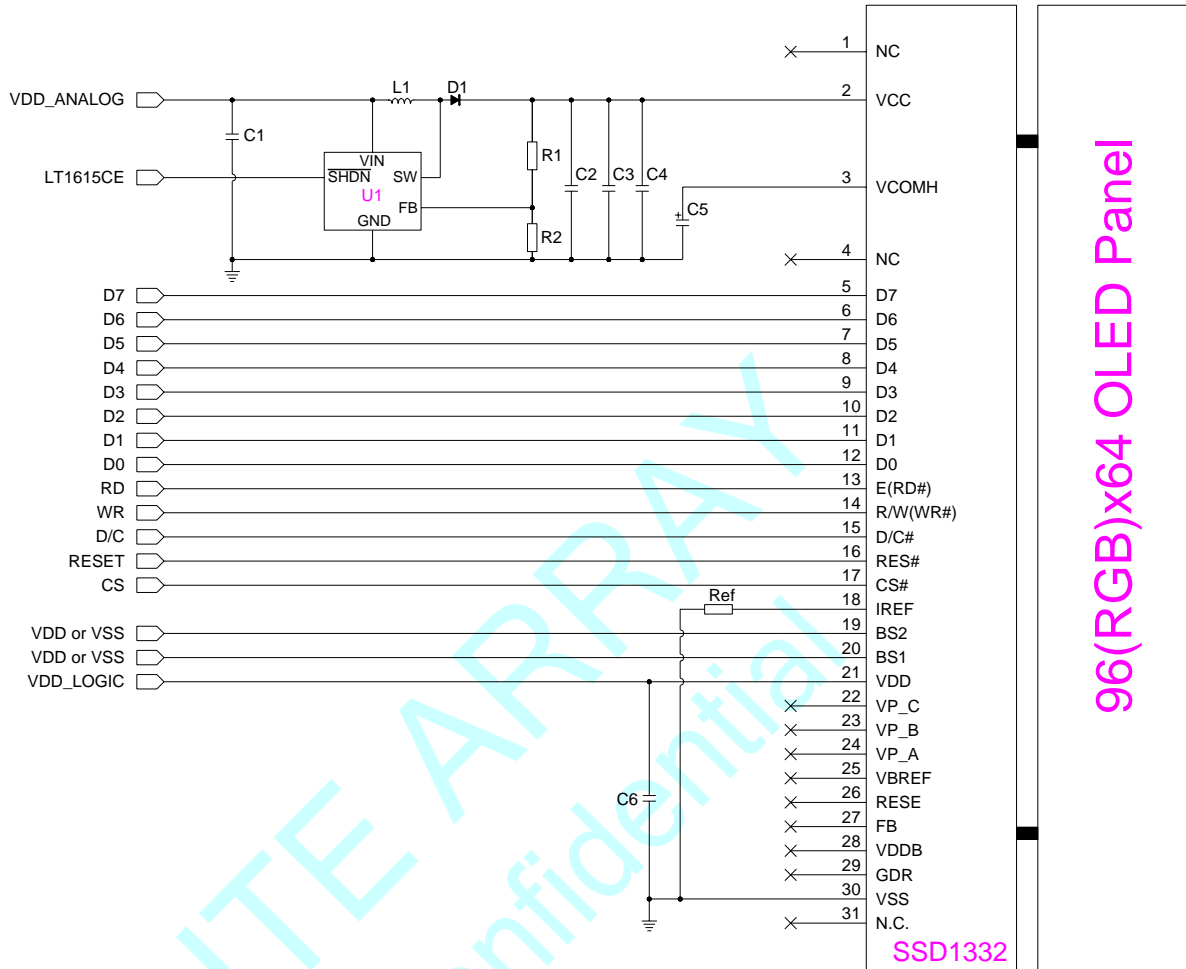
The value of (R2+R3) should be between 500k to 1M ohm.

Below table is the component list for the application circuit.

Item	Description
SSD1332	OLED Driver IC ( <i>Solomon</i> )
Q1	MOSFET – N-FET with low $R_{DS(on)}$ and low $V_{th}$ voltage, eg, MGSF1N02Lt1 ( <i>On Semi</i> )
L1	Inductor – 22 $\mu$ H, 2A
D1	Schottky diode – 2A, 25V, eg, 1N5822
Ref	Resistor – 1%, 1/2W (see remark)
R1	Resistor – 1.2 $\Omega$ , 1%, 1/2W
R2, R3	Resistor – 1%, 1/10W
C1	Capacitor – 1 $\mu$ F~2.2 $\mu$ F, 16V
C2	Tantalum Capacitor – 1 $\mu$ F~2.2 $\mu$ F, 16V
C3	Capacitor – 0.1 ~ 1 $\mu$ F, 16V
C4	Capacitor – 1 ~ 10 $\mu$ F, 16V
C5	Capacitor – 1 $\mu$ F, 16V
C6	Capacitor – 10nF, 16V
C7	Capacitor – 15nF, 16V
C8	Capacitor – 22 $\mu$ F, 25V, Low ESR
C9	Capacitor – 1 $\mu$ F, 16V

**Table 8: Component list for the internal DC-DC voltage converter application**





**Figure 7: Reference Application Circuit (using external DC/DC voltage converter)**

**Notes:**

- MPU interface: 8-bit 6800-series/8080-series parallel interface or Serial interface. It is pin selectable by BS1 and BS2.

	<b>6800-series parallel interface</b>	<b>8080-series parallel interface</b>	<b>Serial interface</b>
<b>BS1</b>	0	1	0
<b>BS2</b>	1	1	0

- U1: LT1615 DC/DC Converter
- LT1615CE can be connected to MCU or VDD for alternative solution.
- $VCC = 1.23 \times (R1 + R2)/R2$

Below table is the component list for the application circuit.

Item	Description
SSD1332	OLED Driver IC ( <i>Solomon</i> )
U1	DC/DC Converter – LT1615 Step-up( <i>Linear</i> )
L1	Inductor – 10 $\mu$ H, 2A
D1	Schottky Diode – 20V, 1A, eg. MBR5120T3
R1	Resistor – 1M $\Omega$ , 1%, 1/4W
R2	Resistor – 150k $\Omega$ , 1%, 1/4W
Ref	Resistor – 910k $\Omega$ , 1% (see remark)
C1,C6	Capacitor – 4.7 $\mu$ F, 6.3V, Low ESR
C2,C3	Capacitor – 4.7 $\mu$ F, 16V, Low ESR
C4	Capacitor – 0.1 $\mu$ F, 16V, Low ESR
C5	Tantalum Capacitor – 1 $\mu$ F ~2.2 $\mu$ F, 16V, Low ESR

**Table 9: Component list for the external DC-DC voltage converter application circuit**

Remark:

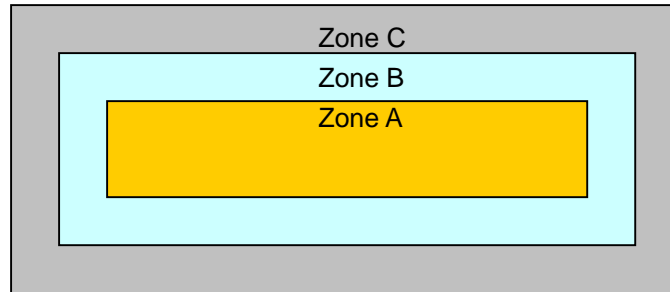
Ref = (Voltage at IREF pin – VSS)/I<sub>REF</sub>; Voltage at I<sub>REF</sub> pin = VCC - VDD

For example, VDD = 3.0V, VCC = 12V, I<sub>REF</sub> = 10 $\mu$ A

Ref = (12-3)/10<sup>-6</sup> = about 910k $\Omega$

# 11. QUALITY SPECIFICATIONS

## 11.1 Quality guaranty of Zone



Zone A: Active Area

Zone B: Viewing Area

Zone C: Appearance or other module organization of Zone B

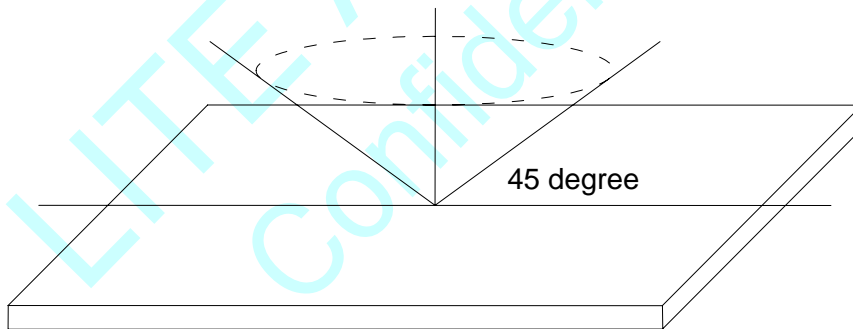
## 11.2 Inspection Condition

Temperature: 20~30°C

Humidity: 40~70%RH

Pressure: 86~106kPa

Functional and Appearance tests shall be performed when the module is turned ON and OFF respectively, allowing a distance of 30cm or more. The viewing angle for a visual check shall not exceed 45 degrees from the vertical in each direction: forward, backward, right and left (See the sketch below). A sample shall be subject to visual observations under the fluorescent lamp of 40watts.



## 11.3 AQL

Defect type	Sampling procedures	AQL
Major	MIL-STD-105D Inspection level I normal inspection single sample inspection	0.65
Minor	MIL-STD-105D Inspection level I normal inspection single sample inspection	1.5

### \*Major defect

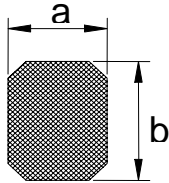
A major defect refers to the defect, which is considered to substantial degradation to the usability for product application.

### \*Minor defect

A minor defect refers to the defect, which is not considered to be substantial degradation for product application, or the defect, which deviate from the existing standards, and it is almost unrelated to the effective use of the product or its operation.

### 11.4 Inspection standards

The size of foreign object or black spot shall be defined as follows



$$D \text{ (mm)} = (a + b) / 2 \text{ [When changing square, length of a side]}$$

#### 1) Major

Zone	Item	Judgment
A. B (turn on)	Non display	No non display is allowed
	Irregular operating	No irregular operation is allowed
	Short	No shorts are allowed
	Open	Any segments or common patterns that don't active are rejectable

#### 2) Minor

##### 2-1) Alien substance, Blemish

Zone	D size (mm)	Judgment
A.B (turn on)	$D \leq 0.10$	Pass
	$0.10 < D \leq 0.15$	2
	$0.15 < D \leq 0.20$	1
	$0.20 < D$	0

##### 2-2) Scratch on Polarizer

Zone	Width (W, mm)	Length (L, mm)	Judgment
A.B (turn on)	$W \leq 0.03$	Pass	Pass
	$0.03 < W \leq 0.05$	$L \leq 2.0$	Pass
		$L > 2.0$	1
	$0.05 < W \leq 0.08$	$L > 1.0$	1
		$L \leq 1.0$	Pass
$0.08 < W$	(*)	(*)	

##### 2-3) Polarizer Bubble

Zone	D size (diameter, mm)	Judgment
A.B (turn on)	$D \leq 0.20$	PASS
	$0.20 < D \leq 0.50$	3
	$0.50 < D \leq 0.80$	2
	$0.80 < D$	FAIL

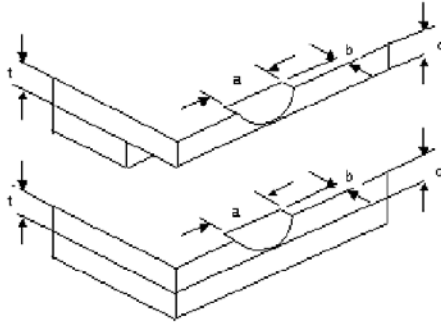
##### 2-4) White/Dark Spot(Spot/Line type)

Zone	D size (mm)	Judgment
A.B (turn on)	$D \leq 0.15$	PASS
	$0.15 < D \leq 0.20$	3
	$0.20 < D \leq 0.30$	2
	$0.30 < D$	FAIL

Zone	Width (W, mm)	Length (L, mm)	Judgment
A.B (turn on)	$0.03 < W \leq 0.04$	$10 < L$	5
	$0.04 < W \leq 0.06$	$5.0 < L \leq 10$	3
	$0.06 < W \leq 0.07$	$1.0 < L \leq 5.0$	2
	$0.07 < W \leq 0.09$	$L \leq 1.0$	1

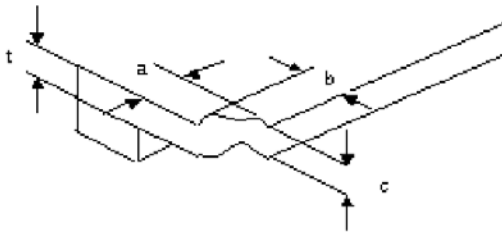
### 3) CRACKS

#### ① General crack(unit : mm)

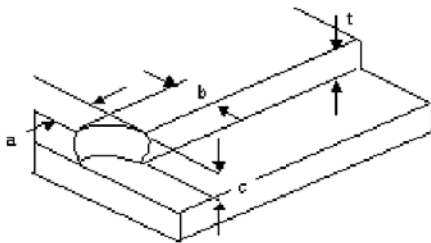


$a \leq 1/6$ panel length
$b \leq 1$
$c \leq t$

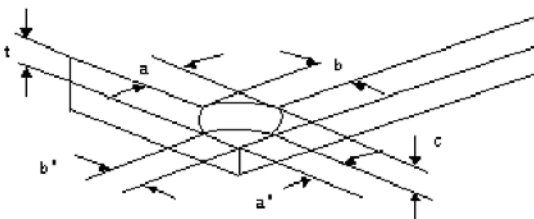
#### ② Corner crack(unit :mm)



$a \leq 2.5$	NO EXPOSURE ANY CONDUCTIVE MATERIAL
$b \leq 2.5$	
$c \leq t$	

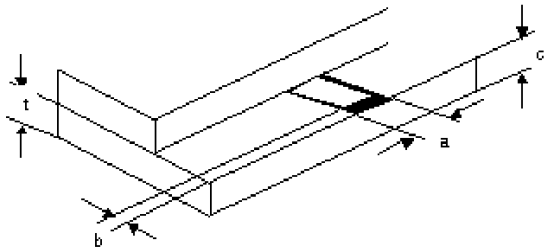


$a \leq 0.7$	NO EXPOSURE ANY CONDUCTIVE MATERIAL
$b \leq 0.7$	
$c \leq t$	



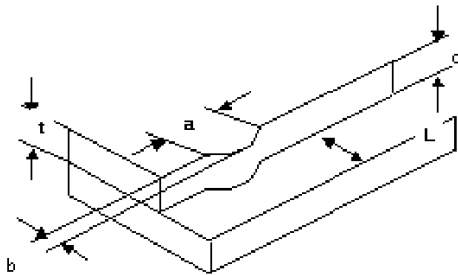
$a \leq 1.3$	$a' \leq a$
$b \leq 1.3$	$b' \leq b$
$c \leq t$	

③ Electrode pad crack (unit : mm )



$a \leq 1/6$ panel length
$b \leq 1/6$ pad length
$c \leq t$

④ Glass chip remain (unit : mm)



$a \leq 1/6$ panel length
$b \leq 1/10$ pad length
$c \leq t$

⑤ Future crack (unit: mm)



NO TOLERATION ANY PROGRESSING CRACK
-------------------------------------



### 11.5 Reliability test condition

Operating life time(30% ON, 50cd/ m<sup>2</sup>) : Longer than 10,000 hours  
 Reliability characteristics shall meet following requirements

No.	ITEM	CONDITION	TEST TIME	CRITERION
1	High Humidity Storage	60±2°C,95±5%RH	96 Hrs	Brightness: over 50% of initial value Color coordination: within ±0.05 of initial value
2	High Humidity Operation	60±2°C,95±5%RH	96 Hrs	
3	High Temperature Storage	80±2°C	96 Hrs	
4	High Temperature Operation	60±2°C	96 Hrs	
5	Low Temperature Storage	-30±2°C	96 Hrs	
6	Low Temperature Operation	-20±2°C	96Hrs	
7	Thermal shock	-30°C(30min) →80°C(30min) 5Cycles, Transient time = 10 min (Turn off) -30°C(30min) → 80°C(30min) 5 Cycles Transient time = 10 min (Turn on)		Appearance or E/T inspection: follows working specification
8	Vibration test (Packaging state)	1.Operating time: 2hrs exposure in each direction (X, Y, Z) 2. Frequency (1min): 10 to 55Hz 3. Amplitude: 2mm		There isn't crack and broken on soldering part
9	Drop test (Packaging state)	1.Direction: 1 corner, 3 edges, 6 faces, drop once for each direction 2. 3 times height 1.8m or 5 times height 1.5m from concrete surface		There isn't crack and broken on soldering part
10	ESD	150Pf, 330 ,±8kV 10times, air discharge		After testing, cosmetic and electrical defects should not happen. Total current consumption should be double of initial value



LITE ARRAY  
Confidential

Lite Array reserves the right to make changes without further notice to any products described herein. Unless specifically agreed to by Lite Array in writing in a particular instance, Lite Array makes no warranty, representation or guarantee, express or implied, regarding the suitability of its products for any particular purpose, nor does Lite Array assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Unless specifically agreed to by Lite Array in writing in a particular instance, Lite Array does not convey any license under its patent rights nor the rights of others. Lite Array products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Lite Array product could create a situation where personal injury or death may occur. Should Buyer purchase or use Lite Array products for any such unintended or unauthorized application, Buyer shall indemnify and hold Lite Array and its offices, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Lite Array was negligent regarding the design or manufacture of the part. The purchase of a Lite Array product by a buyer shall, for such product, be deemed an acceptance by the buyer of the terms set forth above.