Power supply and ground design for WiFi transceiver

A solid RF layout requires careful planning of board stack-up, power supply routing, supply bypassing and grounding. These techniques, along with correct placement of filter components, can address PLL spurs as demonstrated by an IEEE-802.11a/g transceiver reference design.

By Roger Bremer, Tracey Chavers, Zhongmin Yu

A solid RF layout requires careful planning of board stack-up, power supply routing, supply bypassing, and grounding. These techniques along with correct placement of filter components can address PLL spurs as demonstrated by an IEEE-802.11a/g transceiver reference design.

Fundamentals of supply routing and bypassing

When designing RF circuits, the implementation and layout of the power supply section is often treated as an afterthought when compared with the high-frequency signal path. Without careful consideration, it is easy for the supply voltages around the circuit to become corrupted and noisy, adversely affecting the system performance of the RF circuitry. Proper planning of the PCB layer stack-up, V_{CC} routing via a star topology, and proper decoupling of the V_{CC} pins will help in achieving the best RF performance possible.

Starting with a sensible PCB layer definition will ease the rest of the layout process. Given a four-layer board, as is commonly used in WLAN routing, a typical stack-up would be to use the top layer for component placement and RF routing, a ground plane on the second layer, power routing on the third layer and whatever signal routing remains on the fourth layer.

Placing an uninterrupted ground plane on the second layer is imperative for establishing well-controlled impedances for the RF signal paths. It also allows for ground returns to be as short as possible and isolates the first and third layers so that coupling is minimized. While it is possible to effectively use other stack-up approaches (required if a different number of layers is used), the aforementioned approach has been proven to successfully work.

While it may be tempting to use a large power plane to simplify the routing of the V_{CC} signals, this approach will most definitely lead to degraded system performance. By tying all of the supply voltages together at a large plane, it is impossible to prevent noise transfer from one pin to another.

Instead, using a star topology reduces coupling between the various supply pins in a system. An example of distributing V_{CC} through a star topology is shown in Figure 1. This figure is taken from the layout of the MAX2826 IEEE 802.11a/g transceiver evaluation board. A main VCC node is established, from which individual traces branch out to feed each of the RF IC supply pins. Using independent traces for each supply pin presents spatial separation between the pins, thus minimizing the amount of coupling that is seen. Each line will also have a finite amount of parasitic inductance associated with it, and that inductance works in our favor to help filter high-frequency noise from line.

When using a star topology for V_{CC} routing, it is necessary to properly decouple the supply lines. Decoupling is complicated by the fact that capacitors have parasitic inductance. In practice, a capacitor is represented as a series RLC circuit as shown in Figure 2. The capacitance will dominate at low frequencies, but after the self-resonant frequency (SRF) at

$$f_S = \frac{1}{2p\sqrt{LC}},$$

the impedance of the capacitor will begin to look inductive. Thus, a capacitor is only useful for decoupling purposes over a frequency range that is near or below its SRF, where the capacitor presents a low impedance at the frequency of interest.

Figure 3 shows typical S11 performance for various capacitor values. From these plots, the SRFs can be seen by the dip in the graph. It can also be seen that the higher capacitances provide better decoupling (apparent lower impedance) at lower frequencies than the lower-valued capacitors.

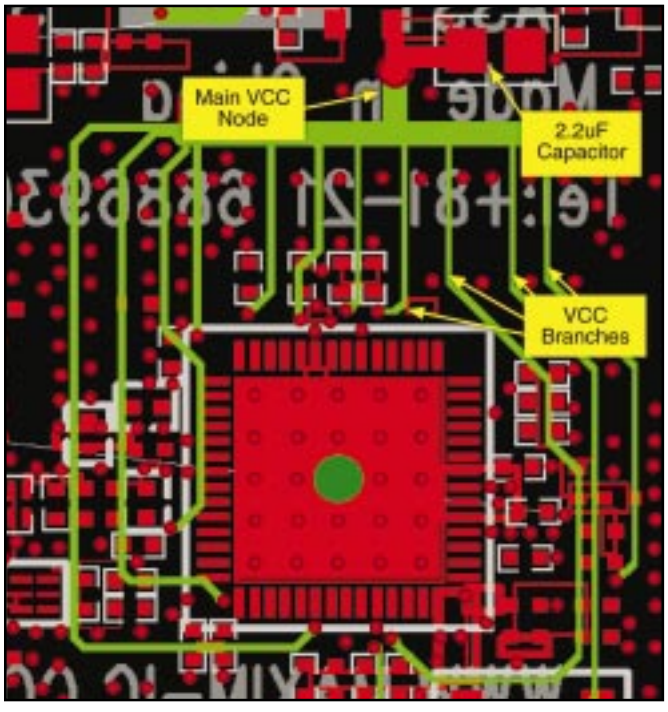

Figure 1. Star topology V_{CC} routing.

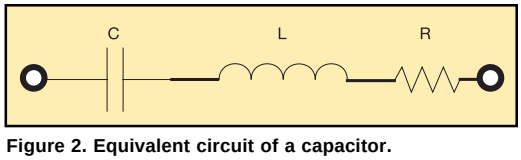

Figure 2. Equivalent circuit of a capacitor.

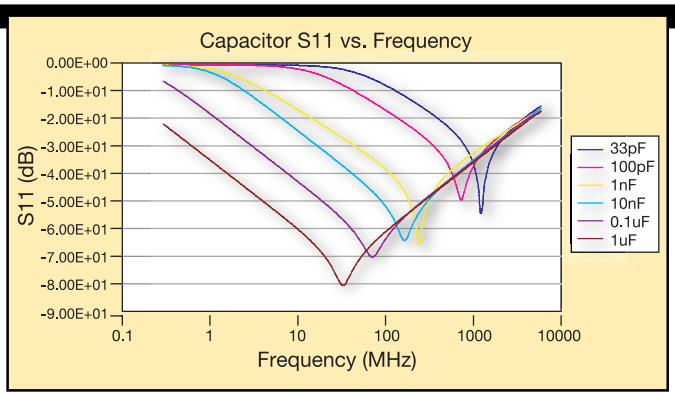

Figure 3. Capacitor impedance variations over frequency.

At the main node of the VCC star, it is desirable to place a large valued capacitor, such as 2.2 µF. This capacitor has a low SRF but is effective at removing low-frequency noise and creating a stable dc voltage. At each supply pin of the IC, a lower-valued capacitor such as 10 nF, should be used to remove any higher-frequency noise that may couple onto the V_{CC} line.

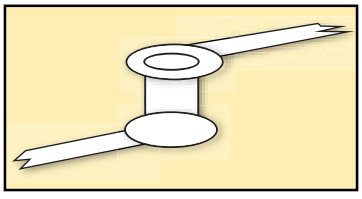

Figure 4. Physical model of a via.

If the part of the circuit that the supply pin is powering is sensitive to noise (i.e., a VCO supply) it may be necessary to place two capacitors close to the IC. For example, using a 100 pF cap in parallel with a 10 nF capacitor will provide a wider frequency range of decoupling and will make the supply less susceptible to noise. Each supply pin should be carefully examined to determine how much decoupling is necessary and at what frequencies the particular circuitry is most vulnerable to noise.

Combining good power supply decoupling techniques with a well thought-out PCB layer stack-up and careful V_{CC} routing (implementing a star-topology) will provide a solid foundation for any RF system design. While there are other factors that can degrade system performance, having a supply as noise free as possible is essential in achieving optimal performance.

In a good board design, drop as many vias to ground as possible in the RF circuitry section—especially for the exposed grounding paddle of popular IC packages.

Fundamentals of RF grounding, using ground vias

Grounding and routing are critical steps in WLAN board layout and fabrication. These steps will directly impact board parasitic parameters that sometimes result in undesirable system performance.

There are no unique solutions to ground distribution in RF board design; several approaches may achieve satisfactory system performance. Split ground planes or split traces can be used to separate analog and digital signals, or isolate high-current or high heat-generating sections. However, based on previous experience with WLAN EV board design, a single solid ground plane in a four-layer stack-up board works well. The rule of thumb is to avoid cross interference by using a ground plane to shield the RF section from other circuitry in the board. As described earlier, layer 2 is usually designated as ground plane while layer 1 is used for components and RF routing.

After grounding arrangements are settled, it is important to route all signal ground returns to the solid ground plane in the shortest path possible. Dropping vias from the top layer ground to the ground plane is a common solution for this task, but vias are quite inductive. The physical model of a via is shown in Figure 4. An accurate electrical model is given in Figure 5 where L_{via} is via inductance and C_{via} is parasitic capacitance of the PCB pad of a via.

In the grounding technique discussed, the parasitic capacitance can be neglected. A 1.6 mm deep via with a diameter of 0.2 mm offers about 0.75 nH of inductance. The equivalent reactance in the 2.5 GHz and 5.0 GHz WLAN bands is about 12 Ω and 24 Ω, respectively. Therefore, a single via to ground does not provide real grounding for RF signals.

In a good board design, drop as many vias to ground as possible in the RF circuitry section—especially for the exposed grounding paddle of popular IC packages. Otherwise, as an example, undesirable emitter degeneration will occur in receive front-end or power amplifier circuitry. The emitter degeneration leads to diminished gain and degraded noise-figure performance. It should be noted that a poorly soldered ground paddle will cause similar problematic effects. In addition, heat dissipation for power amplifiers requires many vias to a solid ground plane.

Filtering noise from other stages, and constraining locally generated noise to avoid cross-interference between stages through V_{CC} lines are a few of the benefits of using V_{CC} decoupling. However, if the decoupling capacitors share the same ground vias, these vias at the joint end will carry all RF interference from both supplies due to the via inductance to ground. This not only makes decoupling capacitors lose their function, but also provides another path for noise coupling between stages in the system.

As will be discussed later, PLL implementation presents a challenge in system design. Satisfactory spur-level performance may not be achieved without good grounding separation. In current IC designs, all PLLs and VCOs are integrated into the chip; most PLLs use digital current-charge-pump outputs to control the VCO through a loop filter. Usually, a second- or third-order RC loop filter is required to filter the charge pump's digital pulse current to an analog control voltage.

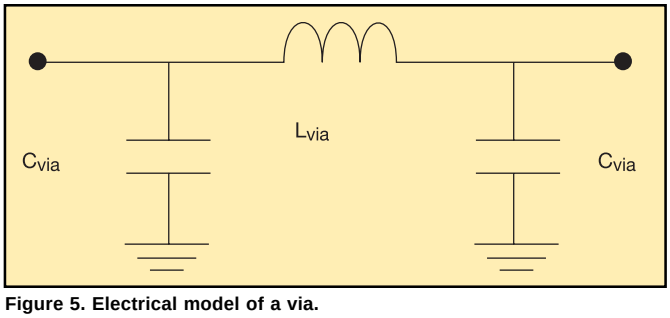

Figure 5. Electrical model of a via.

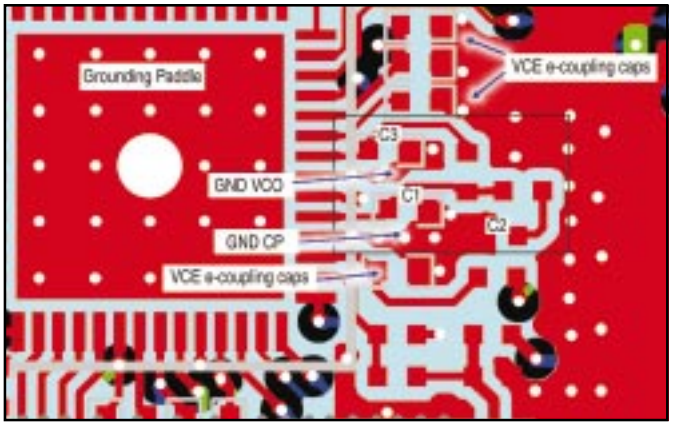

Figure 6. An example of PLL filter component placement and grounding is shown using the MAX2827 reference design board.

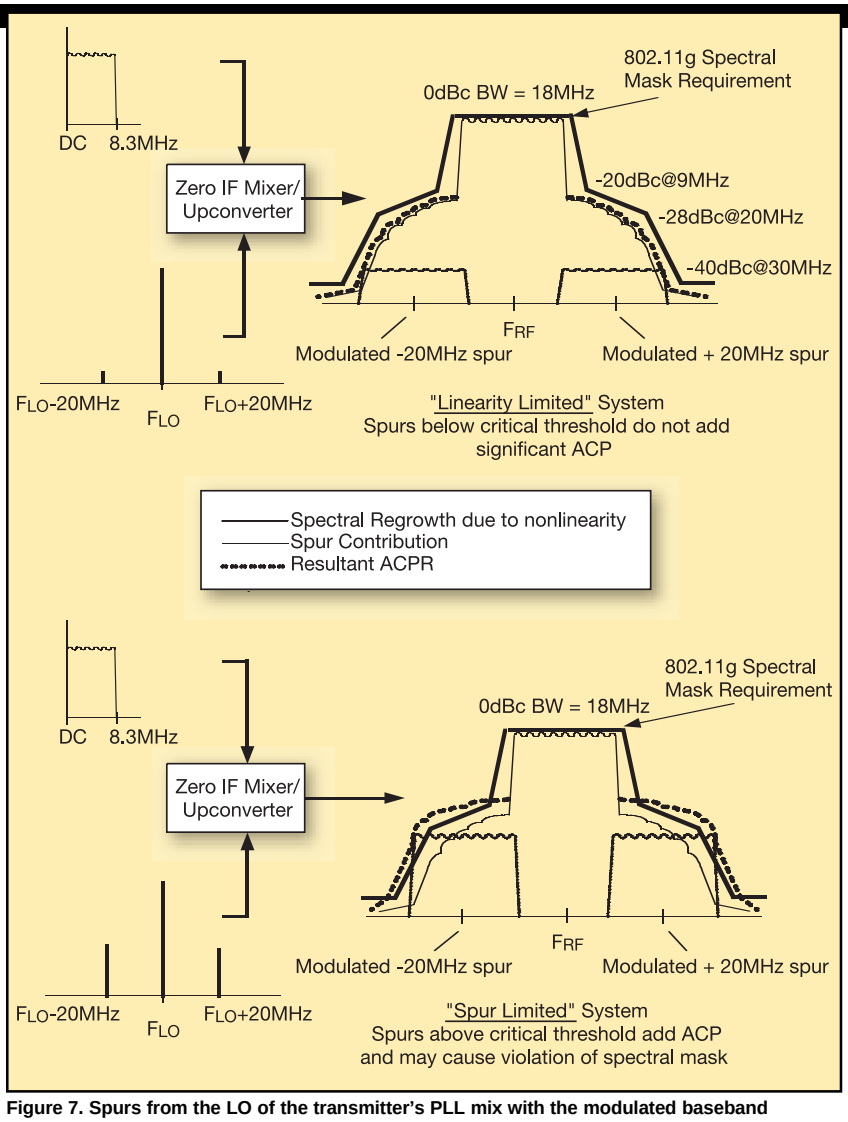

Figure 7. Spurs from the LO of the transmitter's PLL mix with the modulated baseband signal and may degrade adjacent-channel performance if the spurs are above a certain threshold.

filter) should directly connect to the VCO ground to prevent control voltages from floating with the digital current. Straying from these principals increases the risk of high comparison spurs.

An example of a PCB layout for grounding is shown in Figure 6. There are many ground vias in the grounding paddle, allowing each V_{CC} decoupling capacitor to have its own ground via. The circuitry within the box is the PLL loop filter. The first capacitor directly connects to GND_CP while the second capacitor (in series with an R) turns 180° and returns at the same GND_CP. However, the third capacitor connects to GND_VCO. This ground distribution yields superior system performance.

Managing PLL spurious with proper supply bypassing and grounding

Meeting transmit spectral mask requirements in an 802.11a/b/g system can be a challenging component of the design process. Linearity and power consumption must be balanced with enough margin to fall within IEEE and FCC specifications while maintaining adequate transmit output power.

A typical target for an IEEE 802.11g system is +15 dBm at the antenna and –28 dBr at a 20 MHz offset. In-band adjacent channel power ratio (ACPR) is considered largely a function of a device's linearity, which can be adapted (within reason) to a particular application. The arduous task of optimizing ACPR in transmit line-ups is often accomplished empirically through bias adjustments, in both IC and power amplifier (PA), coupled with fine-tuning of PA input, output and interstage matching networks.

However, not all apparent ACPR issues are due to device linearity. In a prime example, a WLAN transmitter can exhibit less than desirable adjacent-channel performance even after extensive tuning and optimization of the power amplifier and PA driver (two of the main contributors to ACPR). Spurs on the local oscillator (LO) from the transmitter's phase-locked loop (PLL) can also cause poor ACPR performance.

The LO spurs will mix with the modulated baseband signal and the product will be amplified along with the desired channel (Figure 7). This

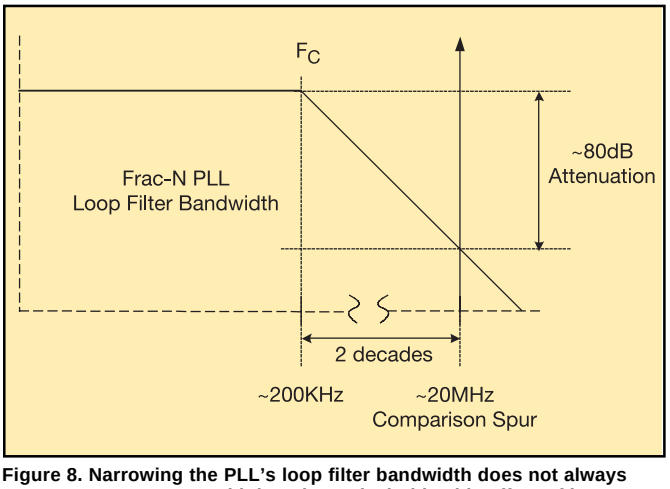

Figure 8. Narrowing the PLL's loop filter bandwidth does not always attenuate PLL spurs, and it has the undesirable side effect of increasing PLL lock time.

The two capacitors nearest the charge pump output must be grounded directly to the charge pump circuitry ground. This isolates the ground-return pulse current path from the VCO ground, minimizing the comparison frequency spurs on the LO. The third capacitor (for a third-order

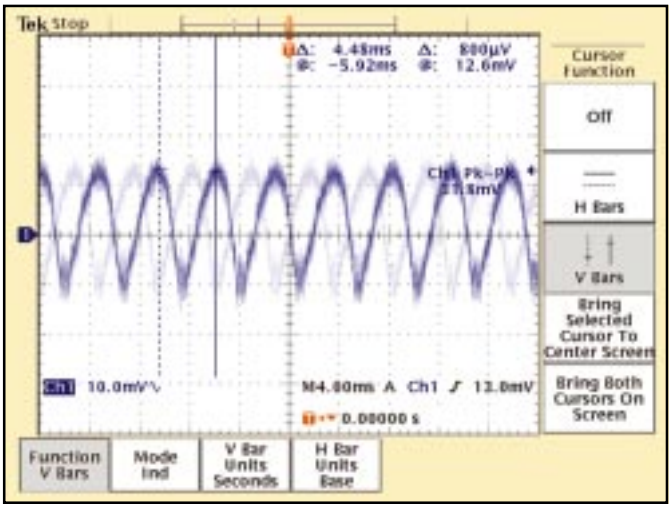

Figure 9. An inadequately decoupled VCO power supply yields the noise measurements shown here.

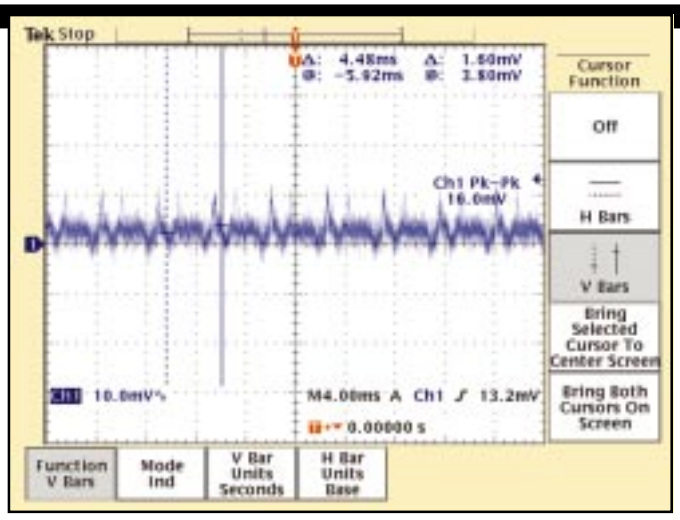

Figure 10. Increased bypass capacitance at the VCO supply quiets the noise.

mixing action is only an issue when the PLL spurs are above a certain threshold. When they are below this threshold the ACPR will be dominated by PA non-linearities.

When the transmit output power and spectral mask performance is "linearity limited," we are in a position to trade-off current for linearity and output power, which is the desired scenario. If LO spurs dominate the ACPR performance, then we are "spur limited" and are required to bias the PA higher to keep its ACPR contribution down for a given P_{OUT}—this costs more current and offers less flexibility in the design.

This leads to the question of how to limit PLL spurs to an amplitude that does not influence the transmit spectrum. A few techniques can be used once the offending spur has been identified. The first and most tempting solution may be to narrow the PLL's loop-filter bandwidth in an attempt to attenuate the spur. This can work in a select cases; however, an example will expose the possible folly in this line of reasoning.

Take the hypothetical situation in Figure 8. Suppose a fractional-N synthesizer with a 20 MHz comparison frequency is used. If the loop filter is second order, with a cut-off frequency of 200 kHz, a roll-off of roughly 40 dB/decade is nominal, yielding 80 dB of attenuation at 20 MHz.

If the reference spur is measured at –40 dBc, a level that is likely to cause undesired modulation, the mechanism causing the spur probably occurs beyond the influence of the loop filter. (If it were generated prior to the filter, it would have been extremely strong to begin with). Narrowing the filter bandwidth is not likely to improve this spur but will increase PLL lock-time—an undesirable effect.

The most effective way to combat PLL spurs is by using appropriate grounding, power supply routing, and decoupling techniques. The items discussed at the beginning of this article are a good starting point to mitigate PLL spur issues. A star-topology is imperative due to the relatively large current changes that occur in the charge-pump.

The noise generated by current pulses can couple to the power supply of the VCO if isolation is not adequate, and will effectively modulate the VCO at the comparison frequency. This is known as "VCO pushing." Isolation can be improved through physical separation of the power supply lines, decoupling at each V_{CC} pin, judicious placement of ground vias, and the introduction of series ferrite elements (consider this as a last resort). While not all of these measures may be necessary in every design, each can be used as part of a larger spur-mitigation strategy.

Figure 9 demonstrates the effect of an inadequately decoupled VCO power supply. The supply ripple shown directly relates to charge-pump activity that is corrupting the supply line. Fortunately, in this case, the corruption could be reduced significantly by increasing the local by-pass capacitance. Figure 10 was measured at the same point after the change.

In another example, similar noise was observed on the VCO supply. The resultant spurs were strong enough to influence ACPR and no amount of decoupling improved the situation. In this case, a review of the PCB layout revealed that the VCO supply trace was run directly beneath the charge-pump supply. Re-routing the trace reduced the spur to a spec-compliant level.

Conclusion

An understanding of potential issues, coupled with careful planning and layout techniques are the cornerstones of a successful radio design. We have exlored these issues, and presented solutions and strategies to avoid them. In summary, start with a PCB stack-up emphasizing short ground return paths. Rout V_{cc} lines in a star pattern, decoupling them globally and locally with appropriate capacitor values. Ground RF sections liberally, keep return inductances to a minimum, and thoughtfully arrange ground pad locations. Using a combination of these techniques can help keep supply noise and VCO pushing to a minimum and increase the likelihood of a successful design. **RFD**

ABOUT THE AUTHORS

Roger Bremer has a BSEE from the University of Illinois, Urbana-Champaign. He is a wireless systems engineer at Maxim Integrated Products.

Tracey Chavers is an associate RF applications engineer with Maxim Integrated Products. He holds an A.S. in Avionics Technology and is pursuing a BSEE part time. He has written several application notes and other content for Maxim's web site: www.maxim-ic.com.

Zhongmin Yu is a senior RF engineer with Maxim Integrated Products. He holds an MSEE and has contributed to many of Maxim's RF circuit board and system level designs. Zhongmin is regarded by peers and customers as a leading applications engineer.