

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4060B**

### **MSI**

14-stage ripple-carry binary counter/divider and oscillator

Product specification  
File under Integrated Circuits, IC04

January 1995

# 14-stage ripple-carry binary counter/divider and oscillator

# HEF4060B MSI

**DESCRIPTION**

The HEF4060B is a 14-stage ripple-carry binary counter/divider and oscillator with three oscillator terminals (RS, R<sub>TC</sub> and C<sub>TC</sub>), ten buffered outputs (O<sub>3</sub> to O<sub>9</sub> and O<sub>11</sub> to O<sub>13</sub>) and an overriding asynchronous master reset input (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may

be replaced by an external clock signal at input RS. The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (O<sub>3</sub> to O<sub>9</sub> and O<sub>11</sub> to O<sub>13</sub> = LOW), independent of other input conditions. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

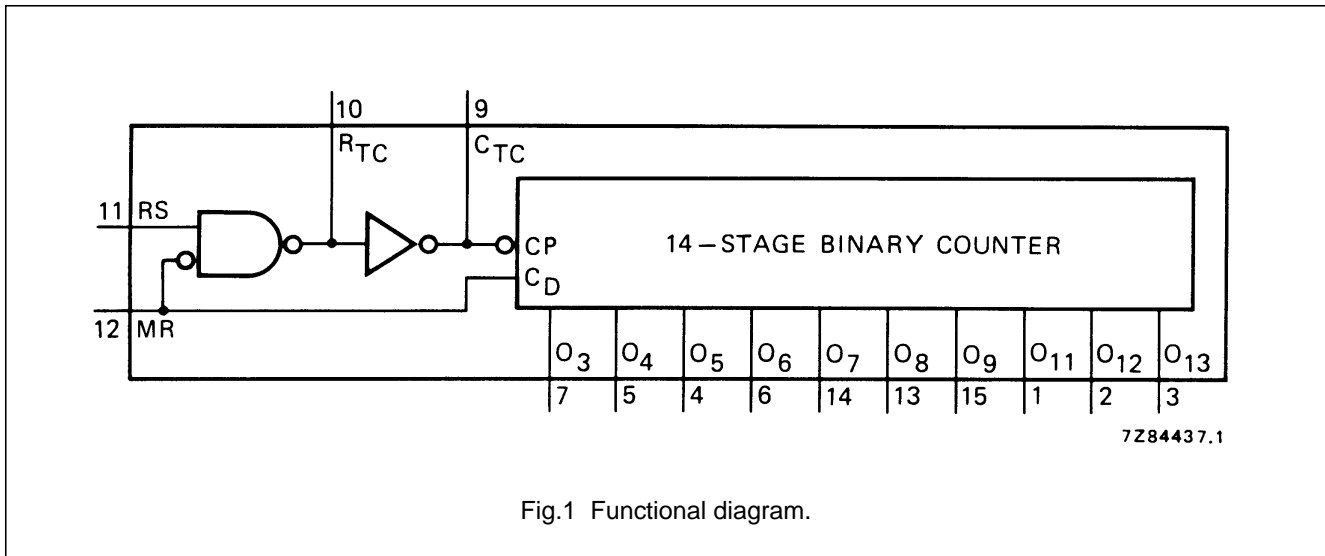


Fig.1 Functional diagram.

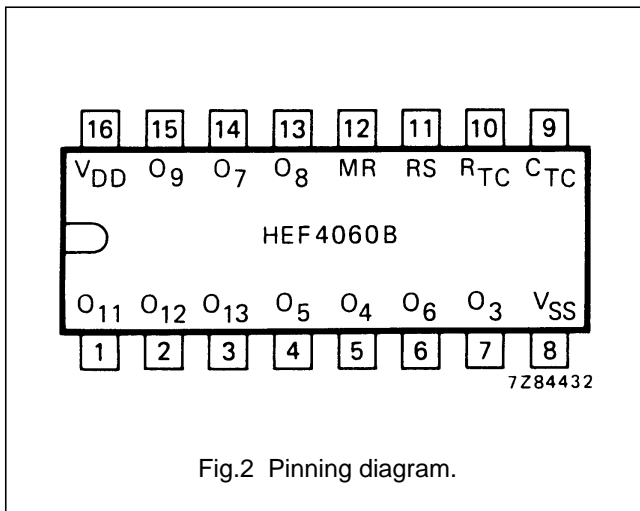


Fig.2 Pinning diagram.

**PINNING**

- MR master reset
- RS clock input/oscillator pin
- R<sub>TC</sub> oscillator pin
- C<sub>TC</sub> external capacitor connection
- O<sub>3</sub> to O<sub>9</sub> counter outputs
- O<sub>11</sub> to O<sub>13</sub> counter outputs

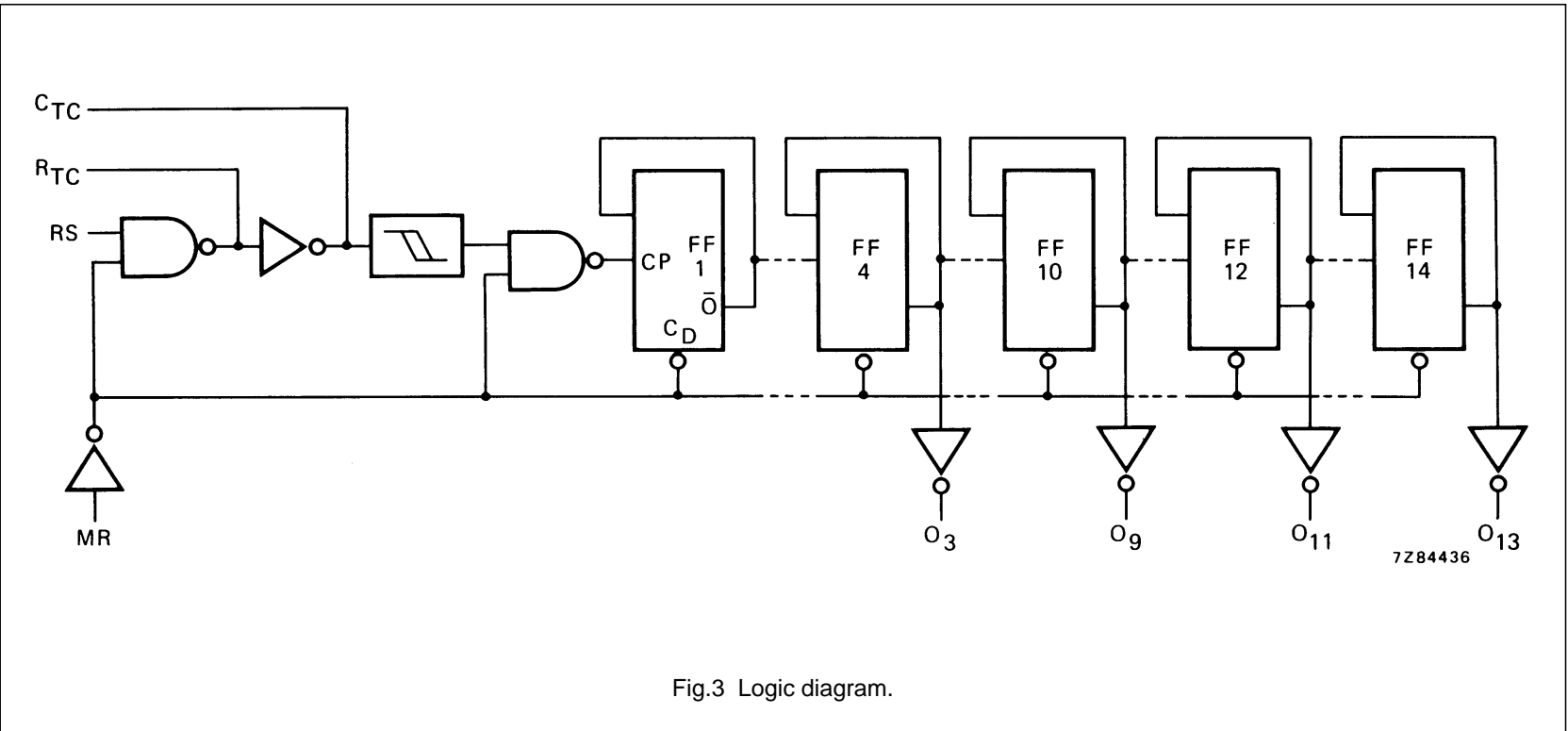
- HEF4060BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4060BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4060BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

**FAMILY DATA, I<sub>DD</sub> LIMITS category MSI**

See Family Specifications

# 14-stage ripple-carry binary counter/divider and oscillator

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MSI



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### AC CHARACTERISTICS

$V_{SS} = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF; input transition times  $\leq 20$  ns

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA				
Propagation delays	5	$t_{PHL}$		210	420	ns	$183 \text{ ns} + (0,55 \text{ ns/pF}) C_L$			
				RS $\rightarrow$ O <sub>3</sub>	80	160		ns	$69 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
				HIGH to LOW	50	100		ns	$42 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
	5	$t_{PLH}$			210	420	ns	$183 \text{ ns} + (0,55 \text{ ns/pF}) C_L$		
					LOW to HIGH	80	160		ns	$69 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
						50	100		ns	$42 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	O <sub>n</sub> $\rightarrow$ O <sub>n+1</sub>	5	$t_{PHL}$		25	50	ns			
					HIGH to LOW	10	20		ns	
						6	12		ns	
		5	$t_{PLH}$			25	50		ns	
						LOW to HIGH	10		20	ns
							6		12	ns
MR $\rightarrow$ O <sub>n</sub>	5	$t_{PHL}$		100	200	ns	$73 \text{ ns} + (0,55 \text{ ns/pF}) C_L$			
				HIGH to LOW	40	80		ns	$29 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
					30	60		ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
Output transition times	5	$t_{THL}$		60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$			
				HIGH to LOW	30	60		ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$	
					20	40		ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$	
	5	$t_{TLH}$			60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$		
					LOW to HIGH	30	60		ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
						20	40		ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
Minimum clock pulse width input RS	5	$t_{WRSH}$		120	60	ns				
				HIGH	50	25		ns		
					30	15		ns		
Minimum MR pulse width; HIGH	5	$t_{WMRH}$		50	25	ns				
					30	15		ns		
					20	10		ns		
Recovery time for MR	5	$t_{RMR}$		160	80	ns				
					80	40		ns		
					60	30		ns		
Maximum clock pulse frequency input RS	5	$f_{max}$		4	8	MHz				
					10	20		MHz		
					15	30		MHz		

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**AC CHARACTERISTICS**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; input transition times  $\leq 20\text{ ns}$

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ ) <sup>(1)</sup>
Dynamic power dissipation per package (P)	5	$700 f_i + f_o C_L V_{DD}^2$
	10	$3\,300 f_i + f_o C_L V_{DD}^2$
	15	$8\,900 f_i + f_o C_L V_{DD}^2$
Total power dissipation when using the on-chip oscillator (P)	5	$700 f_{osc} + f_o C_L V_{DD}^2 + 2C_t V_{DD}^2 f_{osc} + 690 V_{DD}$
	10	$3\,300 f_{osc} + f_o C_L V_{DD}^2 + 2C_t V_{DD}^2 f_{osc} + 6\,900 V_{DD}$
	15	$8\,900 f_{osc} + f_o C_L V_{DD}^2 + 2C_t V_{DD}^2 f_{osc} + 22\,000 V_{DD}$

**Notes**

1. where:

$f_i$  = input frequency (MHz)

$f_o$  = output frequency (MHz)

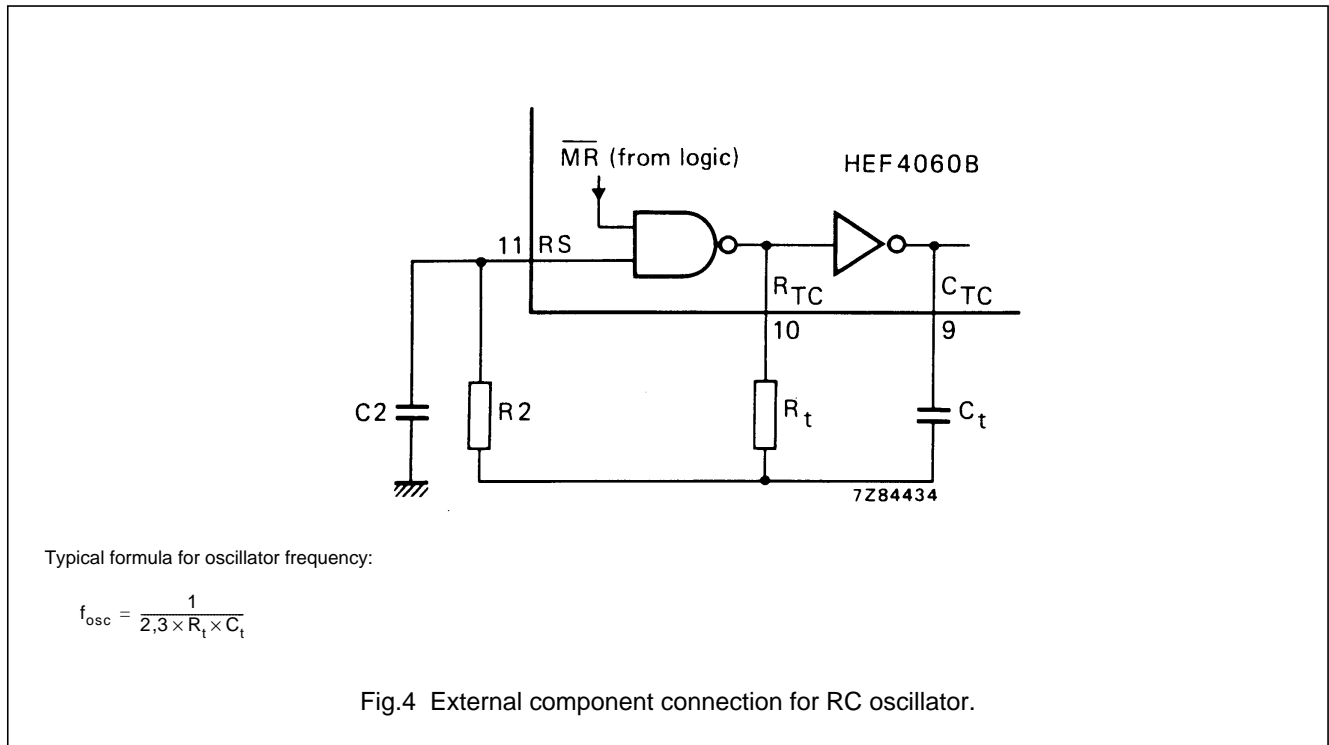
$C_L$  = load capacitance (pF)

$V_{DD}$  = supply voltage (V)

$C_t$  = timing capacitance (pF)

$f_{osc}$  = oscillator frequency (MHz)

**RC oscillator**



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**Timing component limitations**

The oscillator frequency is mainly determined by  $R_t C_t$ , provided  $R_t \ll R_2$  and  $R_2 C_2 \ll R_t C_t$ . The function of  $R_2$  is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance  $C_2$  should be kept as small as possible. In consideration of accuracy,  $C_t$  must be larger than the inherent stray capacitance.  $R_t$  must be larger than the LOCMOS 'ON' resistance in series with it, which typically is 500  $\Omega$  at  $V_{DD} = 5$  V, 300  $\Omega$  at  $V_{DD} = 10$  V and 200  $\Omega$  at  $V_{DD} = 15$  V.

The recommended values for these components to maintain agreement with the typical oscillation formula are:

$C_t \geq 100$  pF, up to any practical value,  
 $10$  k $\Omega \leq R_t \leq 1$  M $\Omega$ .

**Typical crystal oscillator circuit**

In Fig.5,  $R_2$  is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary.

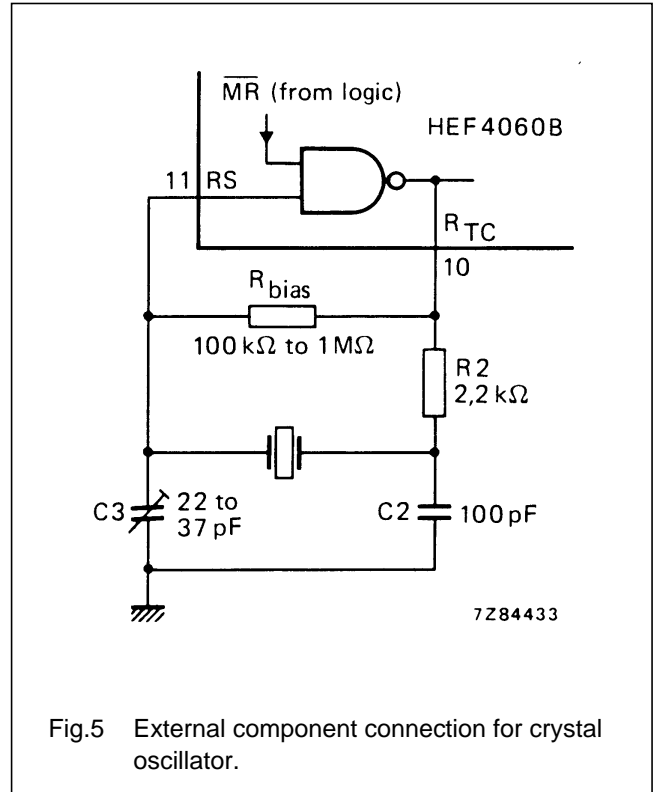


Fig.5 External component connection for crystal oscillator.

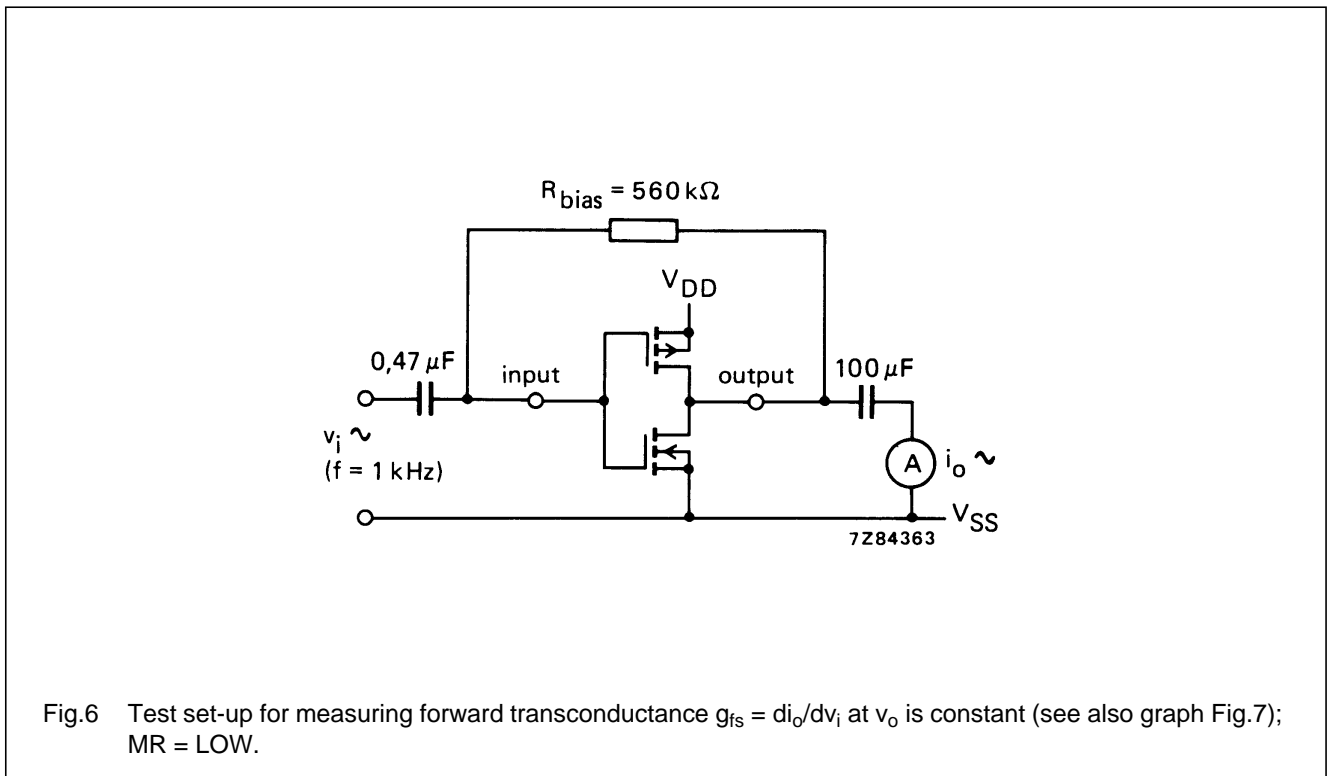


Fig.6 Test set-up for measuring forward transconductance  $g_{fs} = di_o/dv_i$  at  $v_o$  is constant (see also graph Fig.7);  $MR = LOW$ .

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