

D

D

C

C

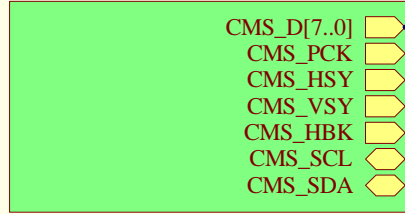
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B

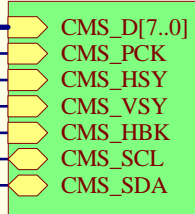
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A

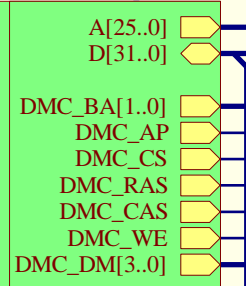
CMOS
CMOS.sch



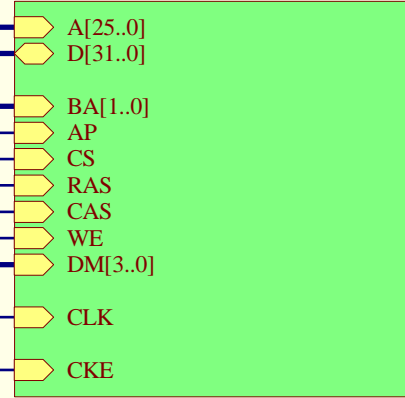
TMPA910Ports
TMPA910Ports.sch



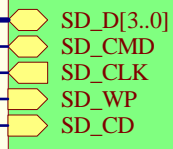
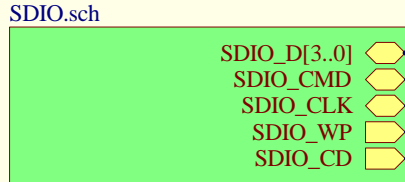
TMPA910Expansion
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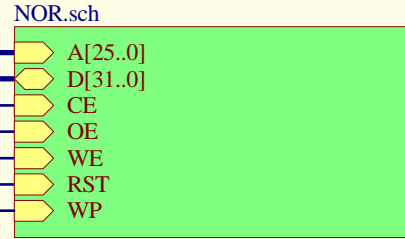
SDRAM
SDRAM.sch



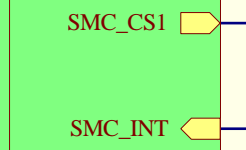
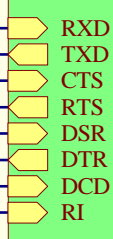
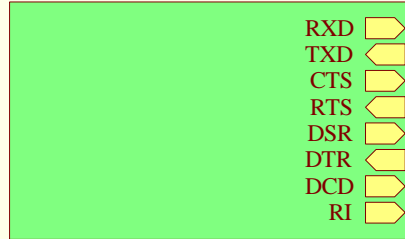
SDIO
SDIO.sch



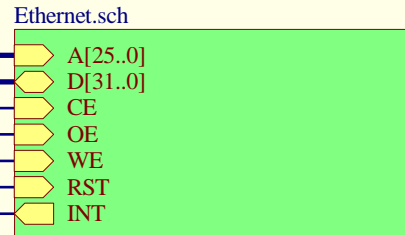
NOR
NOR.sch



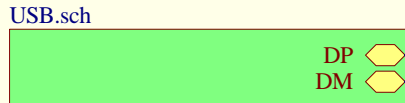
RS232
RS232.sch



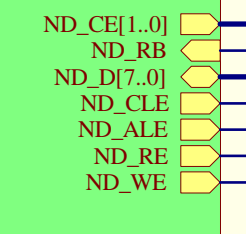
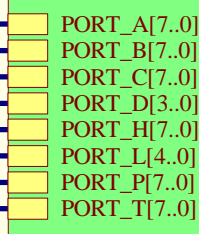
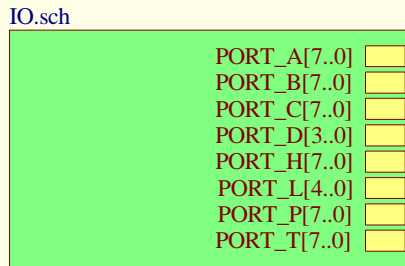
Ethernet
Ethernet.sch



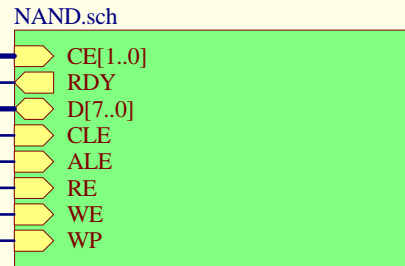
USB
USB.sch



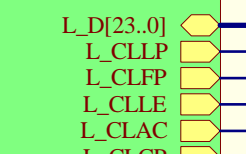
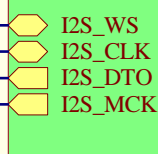
IO
IO.sch



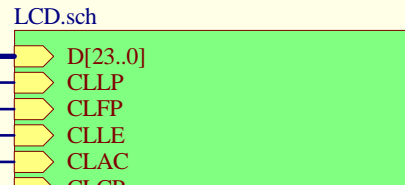
NAND
NAND.sch



I2S
I2S.sch



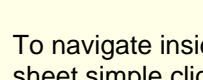
LCD
LCD.sch



Supply
Supply.sch



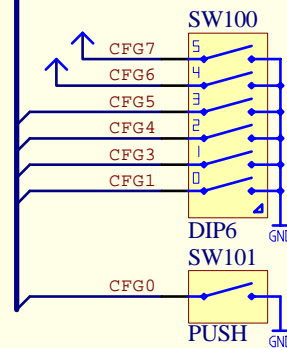
TMPA910Power
TMPA910Power.sch



- FID100 FIDUCAL
- FID101 FIDUCAL
- FID102 FIDUCAL
- FID103 FIDUCAL
- FID104 FIDUCAL
- FID105 FIDUCAL

To navigate inside the TopLevel sheet simple click on the subsheets.

To go back by one level please use the TOSHIBA logo.



SYSTEM CONFIG BUS

- CFG[7] = NOR WP
- CFG[6] = NAND WP
- CFG[5..4] = AM[1..0]
- CFG[3] = SELJTAG
- CFG[1] = ON/OFF SW
- CFG[0] = RESET SW



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TMPA910 - Starterkit Toplevel Schematic

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Size
A4

FCSM No.

DWG No.

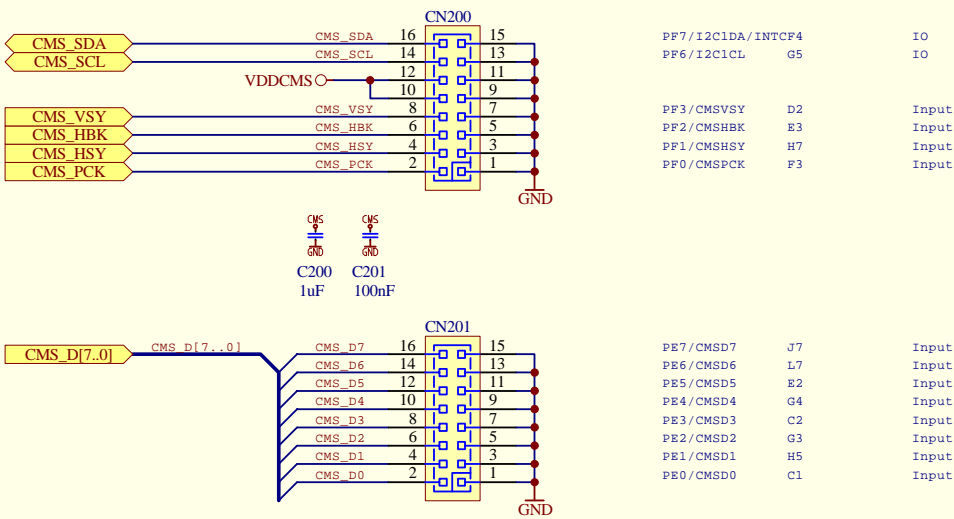
Rev
1.0

Scale

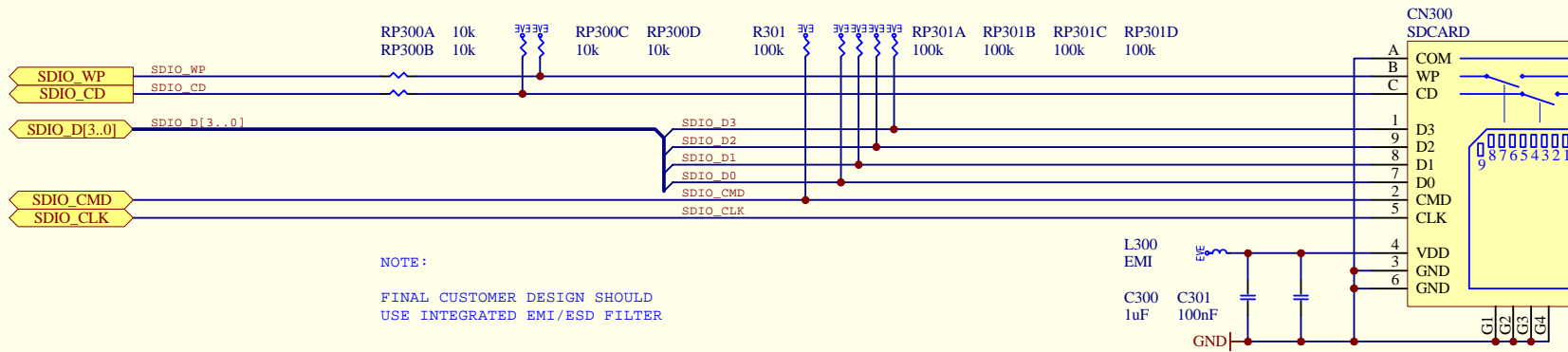
Sheet

1 of 16

NOTE:
EXTERNAL SENSOR CIRCUIT
MUST PROVIDE I2C PULLUP



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	CMOS - external camera sensor connector		
CONFIDENTIAL	Size	FCSM No.	Rev
	A4		1.0
design by www.bplan-gmbh.de	Scale	Sheet	2 of 16



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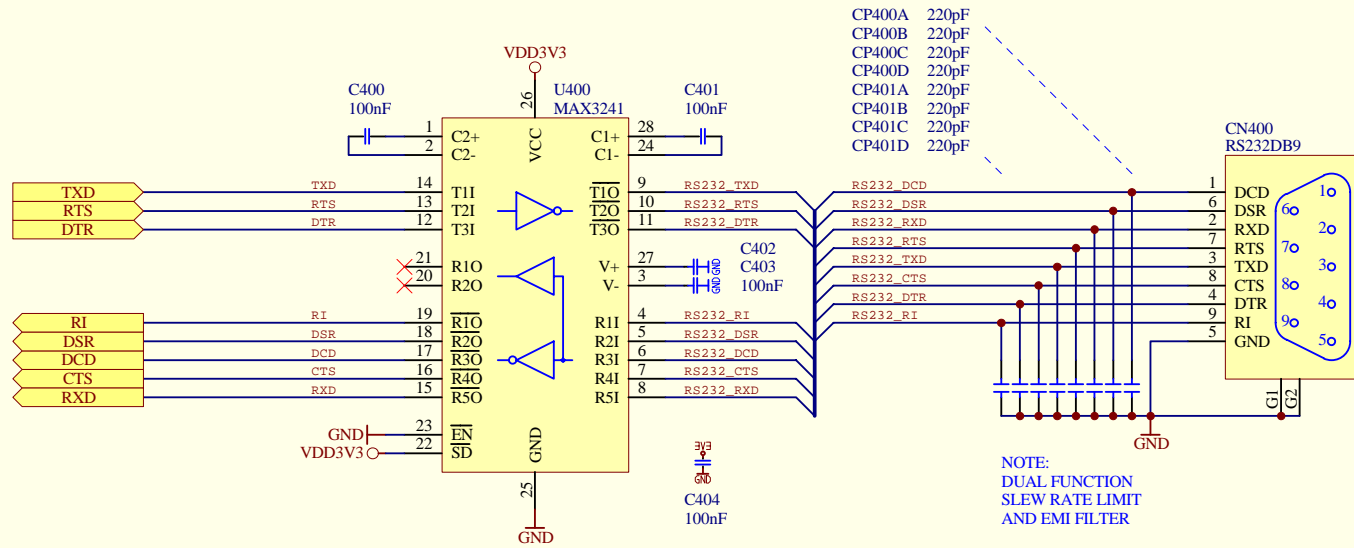
SDIO - Standard SDIO Card Holder

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Size A4	FCSM No.	DWG No.	Rev 1.0
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Scale	Sheet 3 of 16
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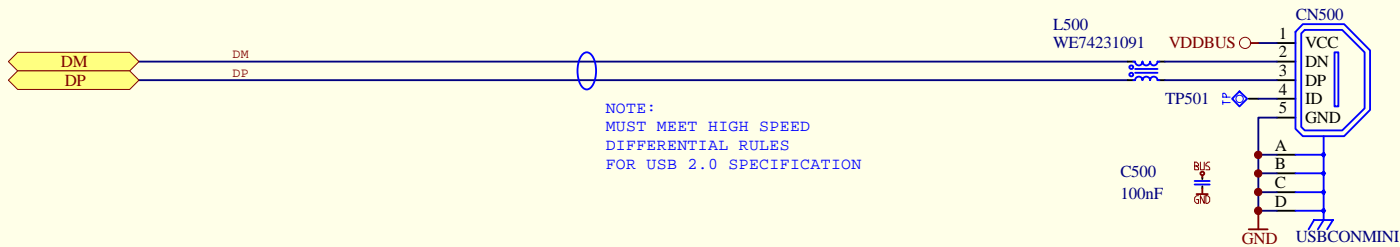
RS232

CONFIDENTIAL

Size A4	FCSM No.	DWG No.	Rev 1.0
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Scale	Sheet 4 of 16
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USB

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Size
A4

FCSM No.

DWG No.

Rev
1.0

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Scale

Sheet
5 of 16

1

2

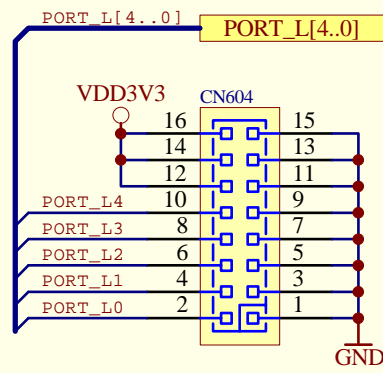
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4

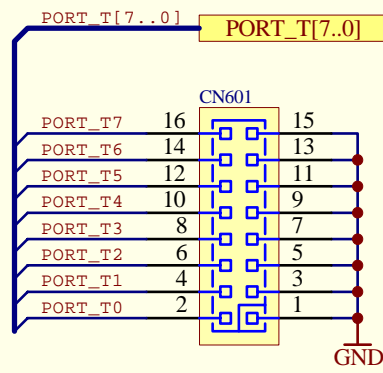
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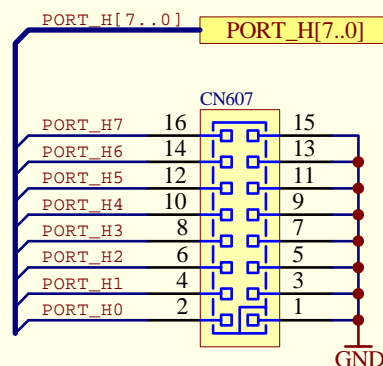
PL4/I2SSCLK	W14	IO
PL3/I2S0MCLK/SP1DIN11		IO
PL2/I2S0DATI/SP1DOR11		IO
PL1/I2S0CLK/SP1CLKU13		IO
PL0/I2S0WS/SP1FSSR12		IO



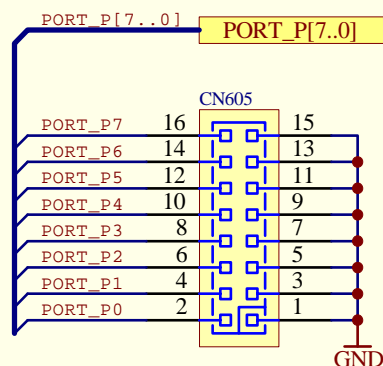
PT7/X1USB/SELNANDU9		IO
PT6/U1CTS _n	K5	IO
PT5/U1RXD	L4	IO
PT4/U1TXD	N7	IO
PT3/SP0DI	J5	IO
PT2/SP0DO	D1	IO
PT1/SP0CLK	H3	IO
PT0/SP0FSS	H4	IO



PH7/SDC1CLK	N1	IO
PH6/SDC1CD	P6	IO
PH5/SDC1WP	M4	IO
PH4/SDC1CMD	R1	IO
PH3/SDC1DAT3	N4	IO
PH2/SDC1DAT2	R6	IO
PH1/SDC1DAT1	P2	IO
PH0/SDC1DAT0	N3	IO



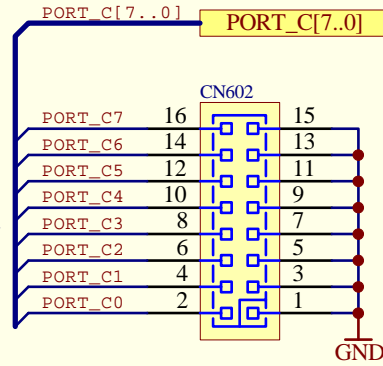
PP7/INT7	L14	IO
PP6/INT6	R19	IO
PP5/INT5	L13	IO
PP4/INT4	M17	IO
PP3/INT3	L12	IO
PP2/INT2	R8	IO
PP1/INT1	P9	IO
PP0/INT0	R9	IO



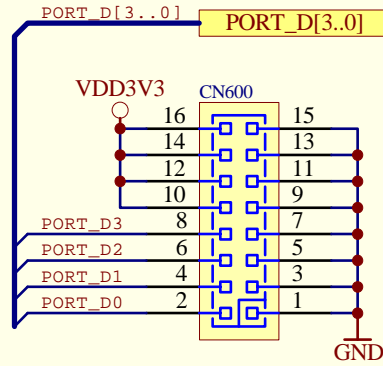
C

C

PC7/I2C0DA/INT9M1		Output
PC6/I2C0CL	L5	Output
PC5/MLDALMn/INT8L6		Output
PC4/FSOUT/PWM2OUTJ3		Output
PC3/MLDALM/PWM0OUTJ2		Output
PC2/PWE	L1	Output
PC1/KO9	J16	Output
PC0/KO8	H19	Output



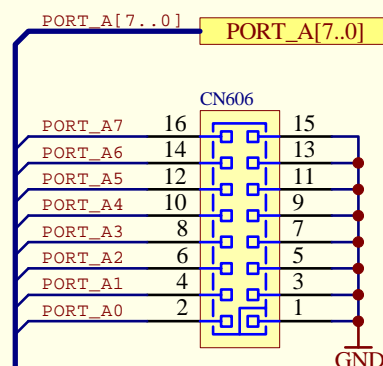
PD3/AN3	R5	Input
PD2/AN2	R4	Input
PD1/AN1	T5	Input
PD0/AN0	T3	Input



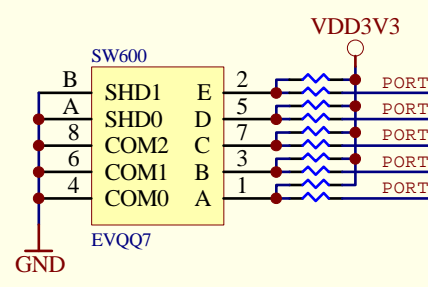
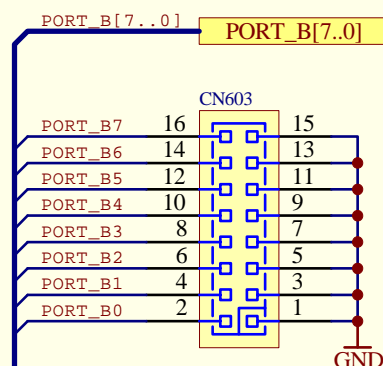
B

B

PA7/KI7	K16	Input
PA6/KI6	M19	Input
PA5/KI5	M18	Input
PA4/KI4	L16	Input
PA3/KI3	L17	Input
PA2/KI2	L15	Input
PA1/KI1	N19	Input
PA0/KI0	N18	Input

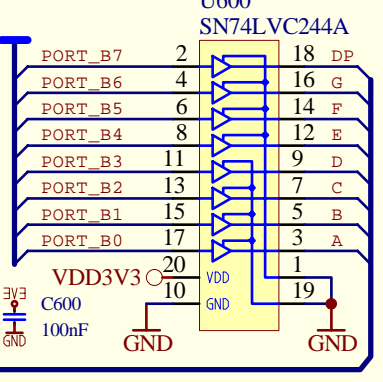
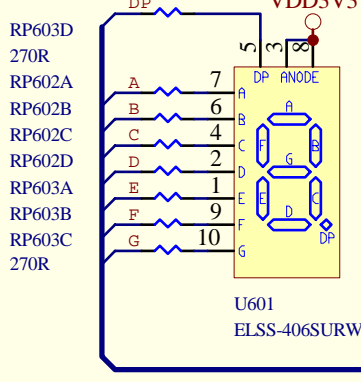


PB7/KO7	J15	Output
PB6/KO6	J18	Output
PB5/KO5	J19	Output
PB4/KO4	K14	Output
PB3/KO3	K18	Output
PB2/KO2	K13	Output
PB1/KO1	L18	Output
PB0/KO0	K15	Output



R601	10k
R600	10k
RP600A	10k
RP601D	10k
RP600B	10k
RP601C	10k
RP600C	10k
RP601B	10k
RP600D	10k
RP601A	10k

NOTE:
 PROVIDE 4 WAY JOYSTICK WITH CENTER PUSH AS CN606 OVERRIDE
 E = CENTER PUSH BOTTON
 D = RIGHT
 C = UP
 A = LEFT
 B = DOWN
 PROVIDE PORT B VISUALIZATION WITH 7 SEGMENT DISPLAY



A

A



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IO Patch Panel - Custom Usage Only

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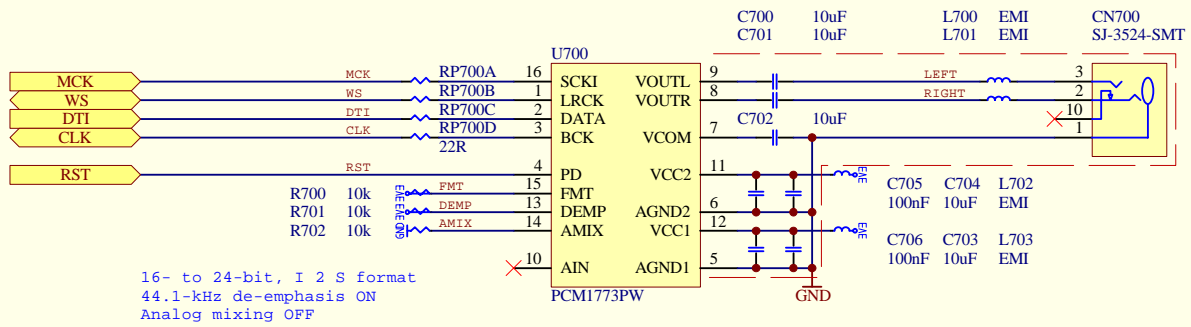
Size A4	FCSM No.	DWG No.	Rev 1.0
Scale	Sheet 6 of 16		

1

2

3

4



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I2S - Audio DAC

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Size
A4

FCSM No.

DWG No.

Rev
1.0

design by www.bplan-gmbh.de

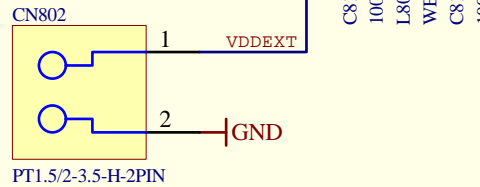
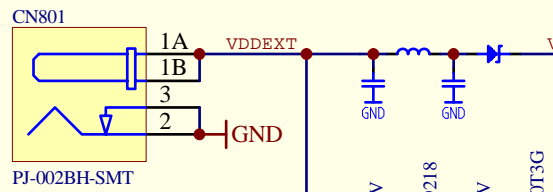
Scale

Sheet
7 of 16

NOTE:

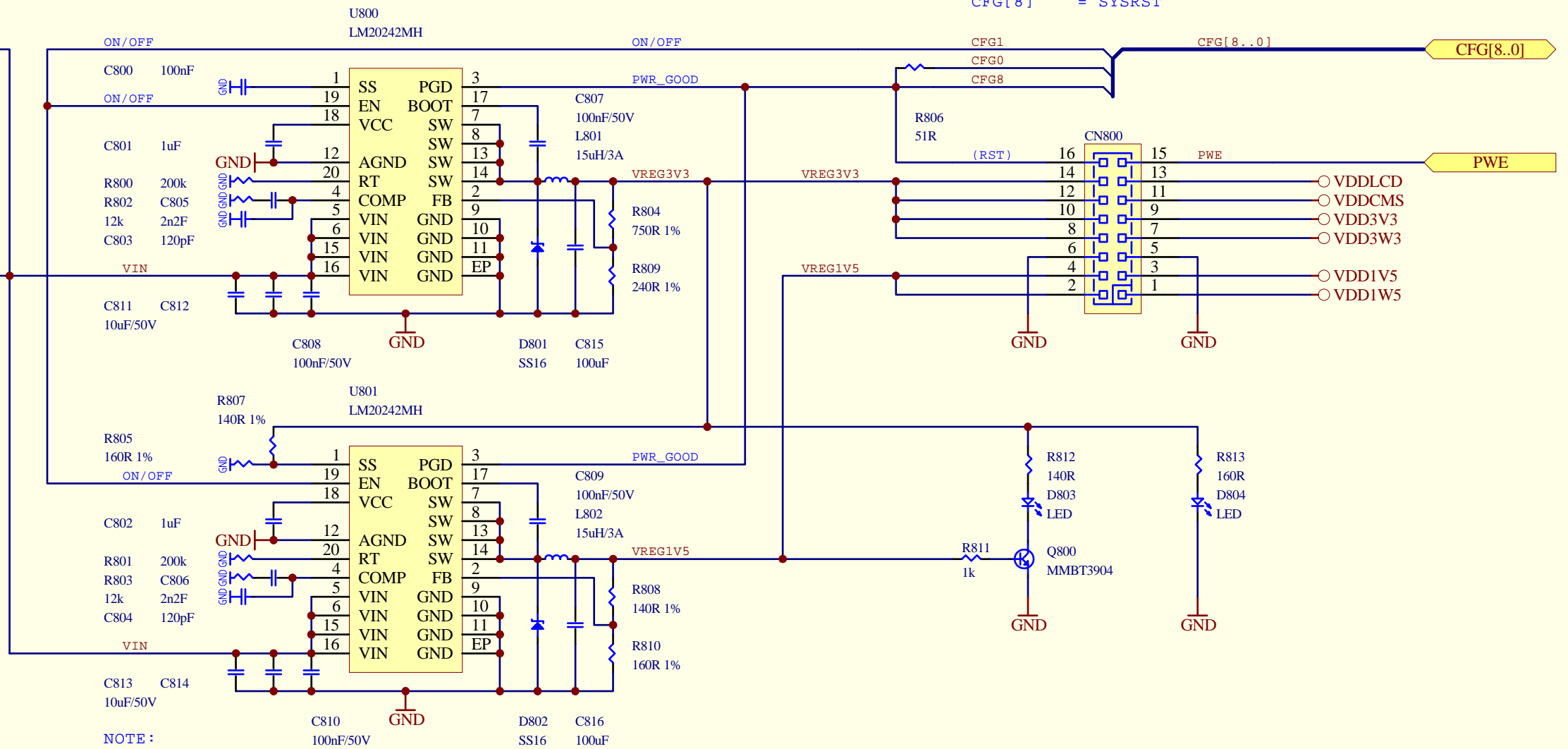
USB BUS SUPPLY

EXTERNAL SUPPLY INPUT 5-35 VOLT DC
INNER CONTACT POSITIVE



ALTERNATE SOLDER PAD CONNECTION

CFG[1] = ON/OFF SW
CFG[0] = RESET SW
CFG[8] = SYSRST



NOTE:
VREG3V3 AND REG1V5 ARE SET FOR
SIMULTANEOUS START UP
(USING SS/TRK FEATURE OF 2ND REGULATOR)

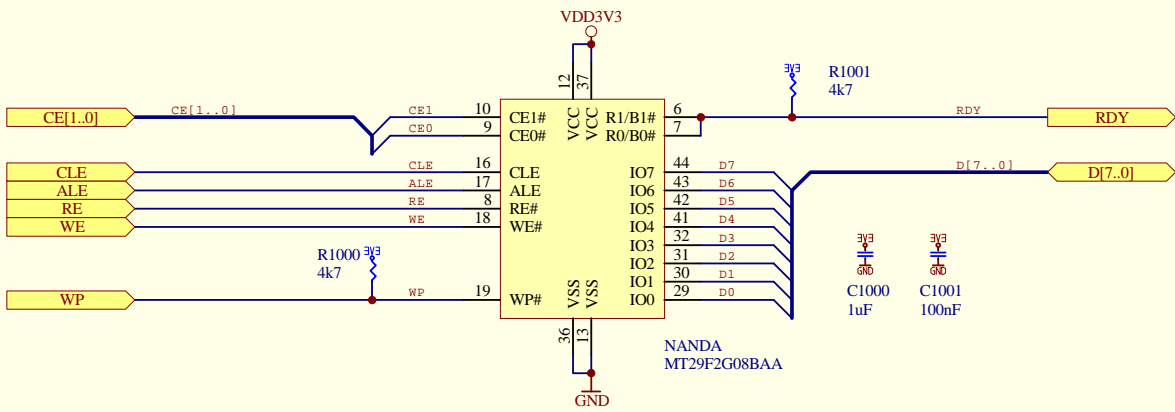
POWER DOMAIN ASSIGNMENT		
SUPPLY	DOMAIN	NOTE
VDDLCD	DVCC3LCD	3.3 V LCD IO AND PANEL
VDDCMS	DVCC3CMS	3.3 V CMOS IO AND SENSOR
VDD3V3	DVCC3IO DVCCM DVCC12S AVCC3AD	3.3 V IO PORTS 3.3 V RAM/NOR/ETHERNET 3.3 V I2S INTERFACE 3.3 V ADC
VDD3W3	AVDD3T AVDD3C	3.3 V PWE DOMAIN USB 3.3 V PWE DOMAIN USB
VDD1V5	DVCC1B	1.5 V RTC AND PMC
VDD1W5	DVCC1A DVCC1C	1.5 V PWE DOMAIN CORE 1.5 V PWE DOMAIN PLL

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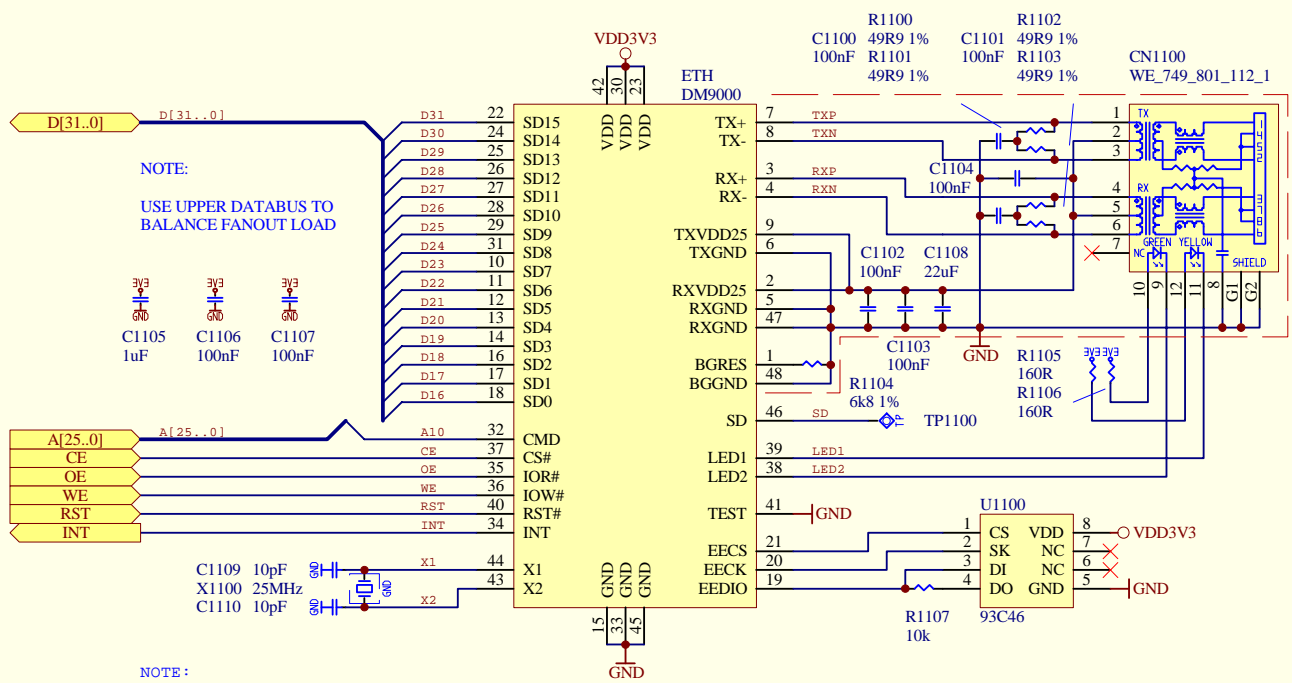
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Supply - TMPA910 Starterkit Power Supply

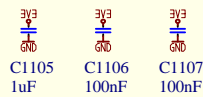
CONFIDENTIAL	Size A4	FCSM No.	DWG No.	Rev 1.0
design by www.bplan-gmbh.de	Scale	Sheet 8 of 16		



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	NAND Flash		
CONFIDENTIAL	Size	FCSM No.	DWG No.
	A4		
design by www.bplan-gmbh.de	Scale	Sheet	Rev
		10 of 16	1.0



NOTE:
USE UPPER DATABUS TO
BALANCE FANOUT LOAD



NOTE:
TMPA910 USES INTERNAL ADDRESS
SHIFT ACCORDING TO SELECTED
BUS WIDTH

ETHERNET CS MUST BE PROGRAMMED TO
32 BIT BUS WIDTH (TO ACCESS UPPER 16 BIT DATABUS)
ACCESS CHIP AT [CS+\$0002] AND [CS+\$1002]



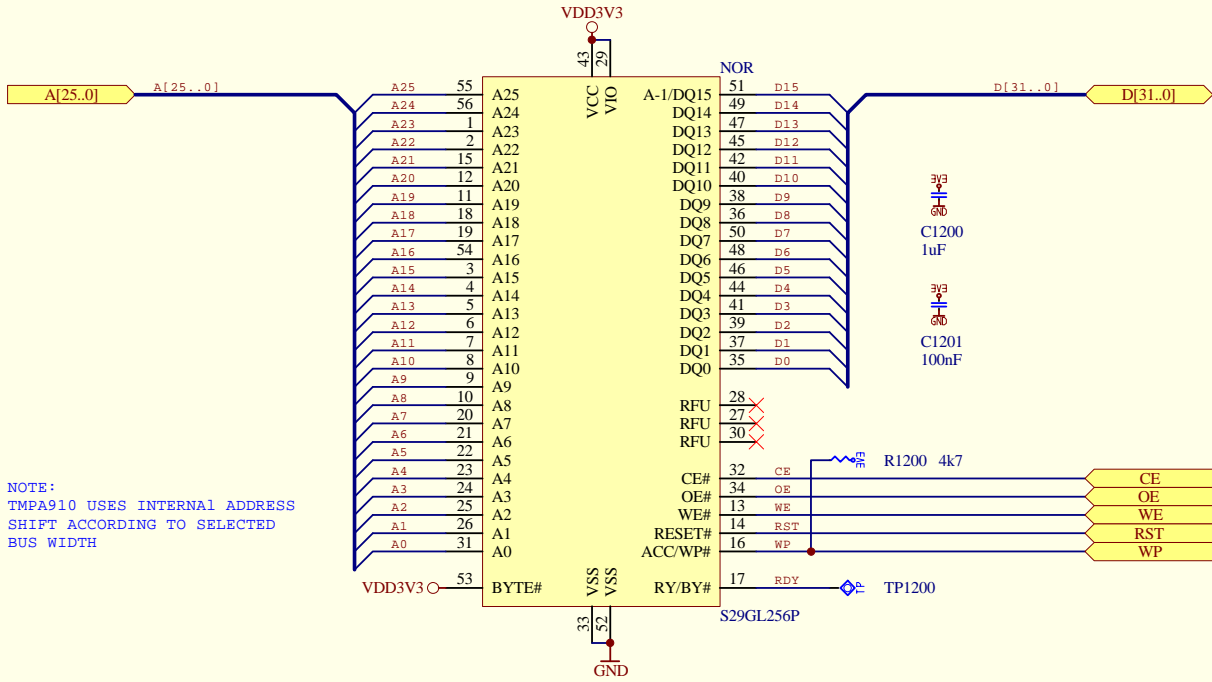
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Ethernet

CONFIDENTIAL

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Size A4	FCSM No.	DWG No.	Rev 1.0
Scale	Sheet 11 of 16		



NOTE:
 TMPA910 USES INTERNAL ADDRESS
 SHIFT ACCORDING TO SELECTED
 BUS WIDTH

NOTE:
 DON'T USE RDY FOR WAITSTATE GENERATION
 IT MAY BE ACTIVE FOR MORE THAN 0.5 SEC
 DURING ERASE
 SOFTWARE SHOULD USE DQ POLLING TO CHECK
 READ STATE

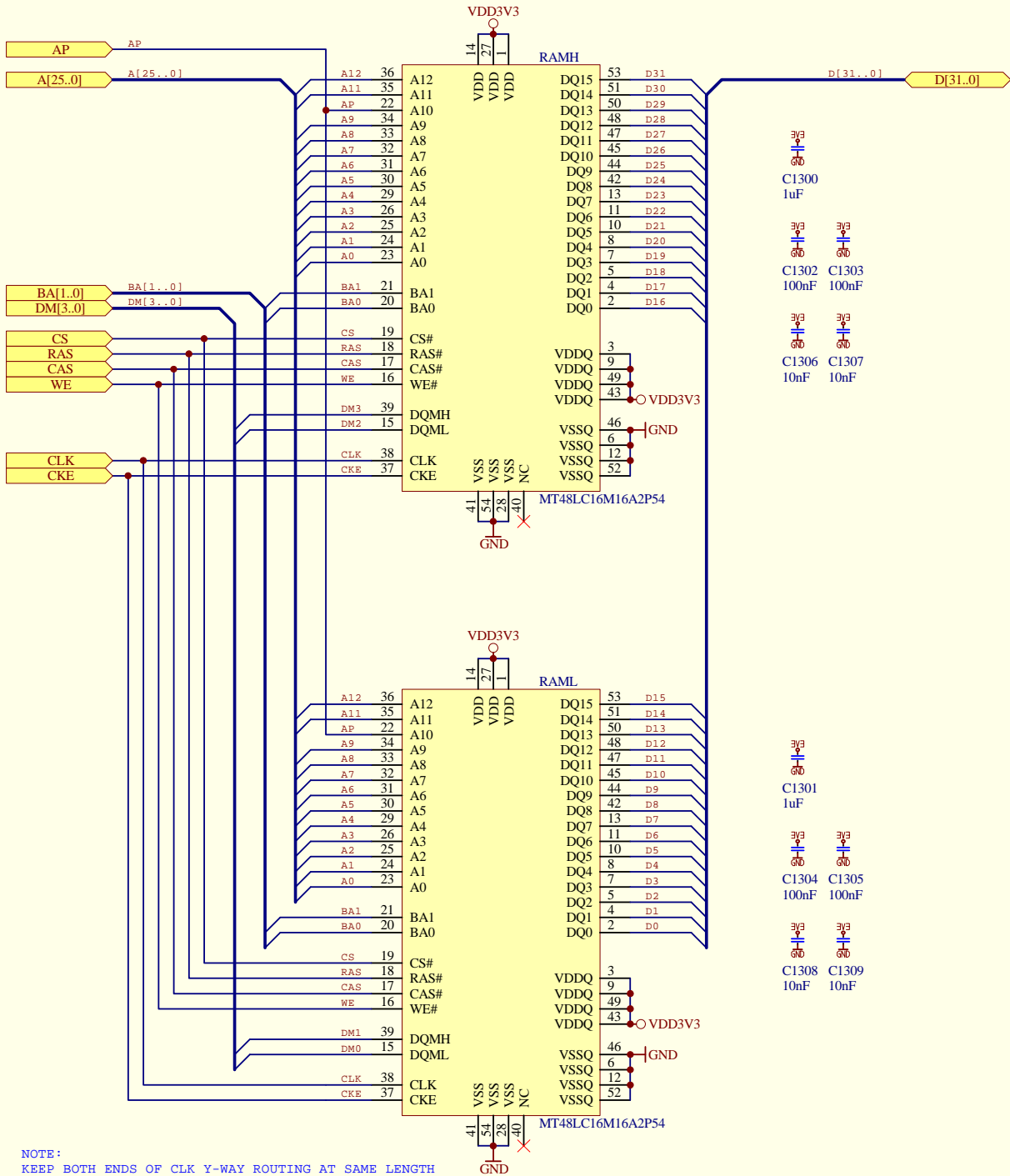


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NOR Flash

CONFIDENTIAL

Size A4	FCSM No.	DWG No.	Rev 1.0
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NOTE:
KEEP BOTH ENDS OF CLK Y-WAY ROUTING AT SAME LENGTH

	TOSHIBA Electronics Europa GmbH Hansaallee 181 40549 Düsseldorf Deutschland/Germany		
	SDRAM		
CONFIDENTIAL design by www.bplan-gmbh.de	Size	FCSM No.	Rev
	A4		1.0
Scale	Sheet		
	13 of 16		

D

D

C

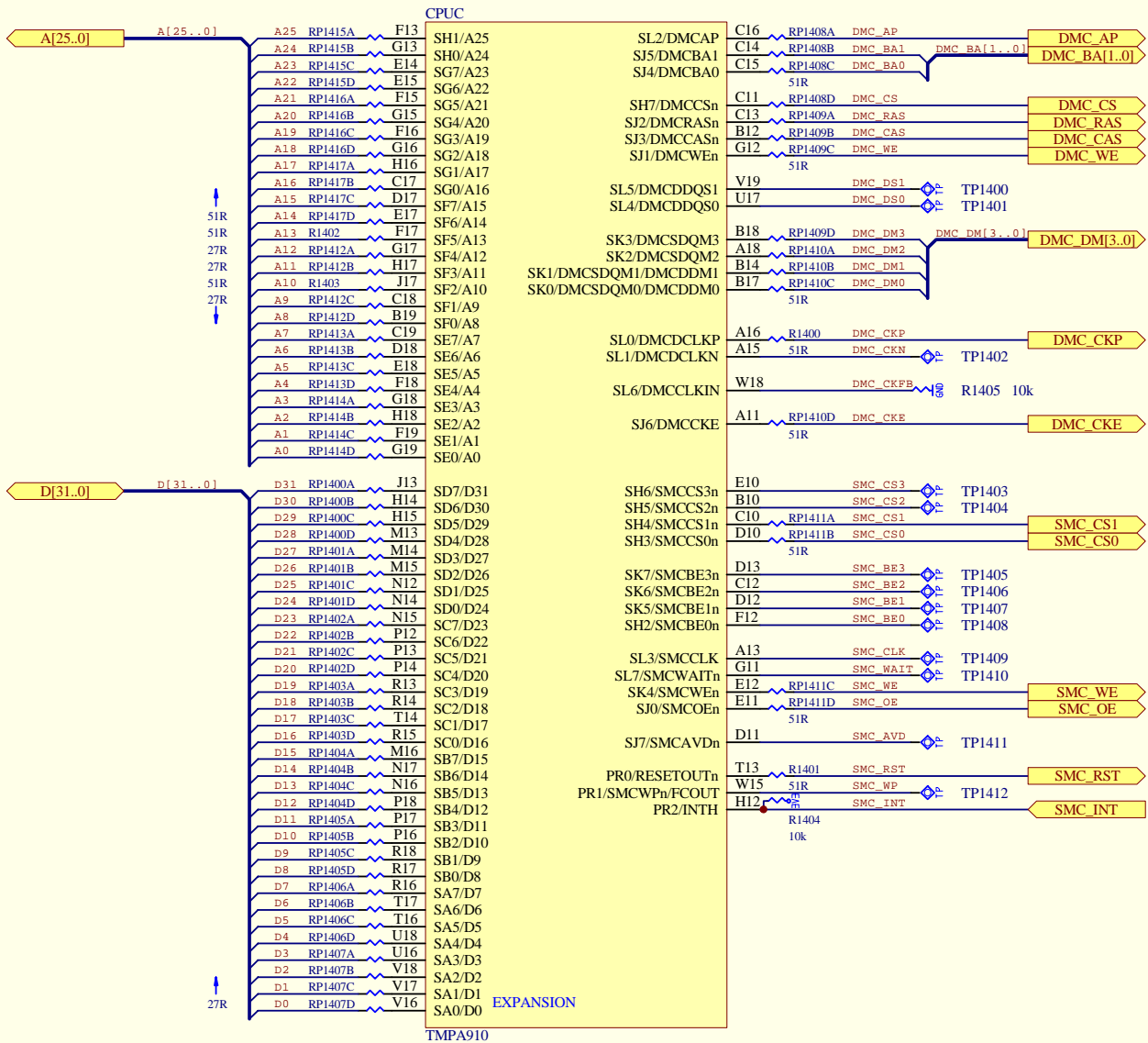
C

B

B

A

A

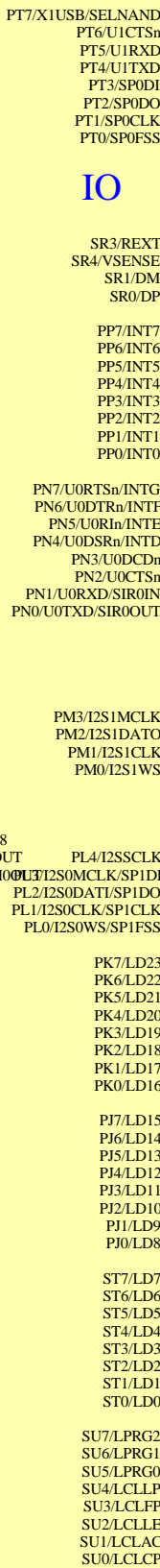
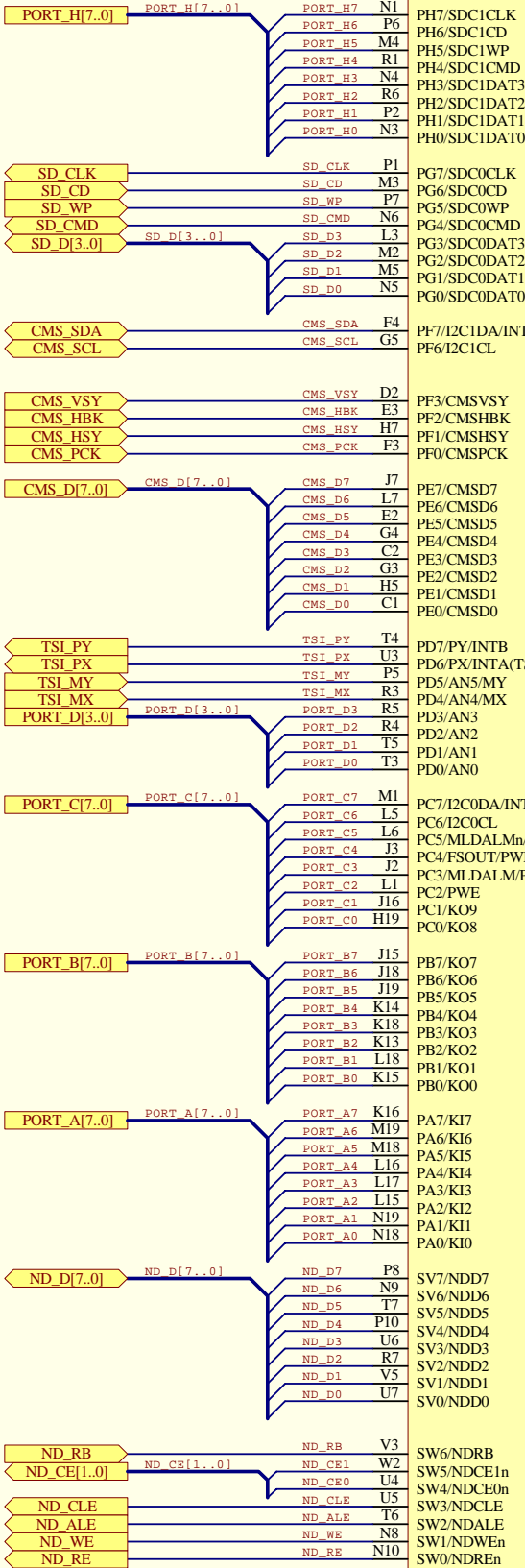


NOTE :

OUTPUT DRIVER OF TMPA910 NEED MATCHING RESISTORS (WITH PROTOTYPE SILICON)
 ANY THREE LOAD SIGNAL (D31-D0,A0-A9,A11,A12) USE 27R
 ANY OTHER (TWO OR ONE LOAD) USE 51R
 FINAL VALUES DEPEND ON LAYOUT AND SILICON VERSION
 SIMULATION OF CUSTOMER PCB IS HIGHLY RECOMMENDED

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	TMPA910 - Expansion Bus		
CONFIDENTIAL	Size	FCSM No.	DWG No.
	A4		
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			Rev 1.0

CPUA



IO

TMPA910

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TMPA910 - IO Ports

CONFIDENTIAL	Size A4	FCSM No.	DWG No.	Rev 1.0
design by www.bplan-gmbh.de	Scale		Sheet 15 of 16	

NOTE:

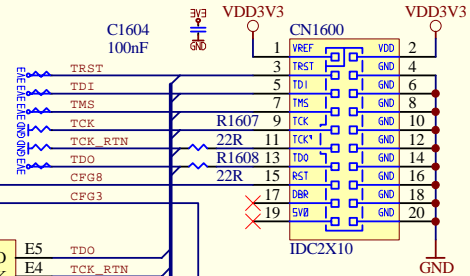
SYSTEM CONFIG BUS

CFG[8] = SYSRST
CFG[5..4] = AM[1..0]
CFG[3] = SELJTAG

CFG[8..0]

RP1600A 10k
RP1600B 10k
RP1600C 10k
RP1600D 10k

R1601 10k
R1602 10k
R1603 10k
R1605 10k
R1606 10k
R1604 10k



NOTE:

STRAPPING ACCORDING TO MANUAL CHAPTER 3.10

R1609 4k7
R1610 4k7

V6 PLL_FILTER
V8 GND
V7 GND

V1 ADC_FILTER
U1 GND

T2 VREFPH
U2 VREFL

V9 USB_FILTER
W10 GND

V13 PLL_FILTER
W13 GND

U10 GND
U12 GND

U11 GND
V11 GND

K8 PLL_FILTER
J8 GND

L8 GND
M9 GND

K3 GND
M8 GND

P4 GND
M10 GND

M10 GND
K9 GND

J10 GND
L10 GND

M11 GND
N13 GND

M12 GND
K10 GND

L11 GND
J12 GND

J11 GND
G14 GND

H13 GND
D16 GND

D14 GND
F14 GND

A17 GND
B13 GND

A14 GND
A14 GND

A12 GND
A12 GND

A10 GND
H11 GND

H10 GND
J9 GND

C6 GND
H9 GND

C6 GND
H9 GND

C6 GND
H9 GND

C6 GND
H9 GND

C6 GND
H9 GND

C6 GND
H9 GND

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C6 GND
H9 GND

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D

C

B

A

D


C

B

A

NOTE:

VDD3V3 AND VDDI5 DOMAINS MUST USE POWER PLANE
KEEP PWR PLANE TO GND PLANE GAP < 0.1MM (4MIL)
PLANE CAPACITANCE IS PART OF SUPPLY DECOUPLING
CHECK NUMBER OF DISCRETE CAPACITORS NEEDED WHEN
CHANGING LAYER STACKUP

 <p>TOSHIBA Leading Innovation >>></p>	TOSHIBA Electronics Europe GmbH Hansaallee 181 40549 Düsseldorf Deutschland/Germany		
	TMPA910 - Supply		
<p>CONFIDENTIAL</p>	Size	FCSM No.	DWG No.
	Scale		
design by www.bplan-gmbh.de			Sheet 16 of 16