PLL PhaseLink Corporation

Analog Frequency Multiplier

(VCXO)

Technical Document

PRODUCT DESCRIPTION

PhaseLink's Analog Frequency Multiplier™ (AFM™) are the industry's first 'Balanced Oscillator' utilizing analog multiplication of the fundamental frequency (at double or quadruple frequency), combined with an attenuation of the fundamental of the reference crystal, without the use of a phase locked loop, in CMOS technology.

PhaseLink's patent pending PL56X family of AFM products can achieve up to 800 MHz output frequency with practically no jitter or phase noise deterioration.

The PL56X AFM products are specifically designed for low-cost high performance VCXO applications. Designed to accept a low frequency input, these devices allow the usage of a low-cost fundamental crystal to reduce the overall system cost, while PhaseLink's non phase locked loop AFM function allows x2 or x4 multiplication of the input frequency for high performance outputs, ranging from 60 MHz -800 MHz. This feature permits significant crystal cost reduction while offering higher performance unattainable with other technologies, at comparable cost.

PL560-XX family of products are specifically designed for low-cost high performance applications. They utilize a low-power CMOS technology and are housed in a 16-pin TSSOP, and 16-pin 3x3 QFN. Additionally, the AFM products are capable of producing a differential PECL, LVDS, or single-ended CMOS output.

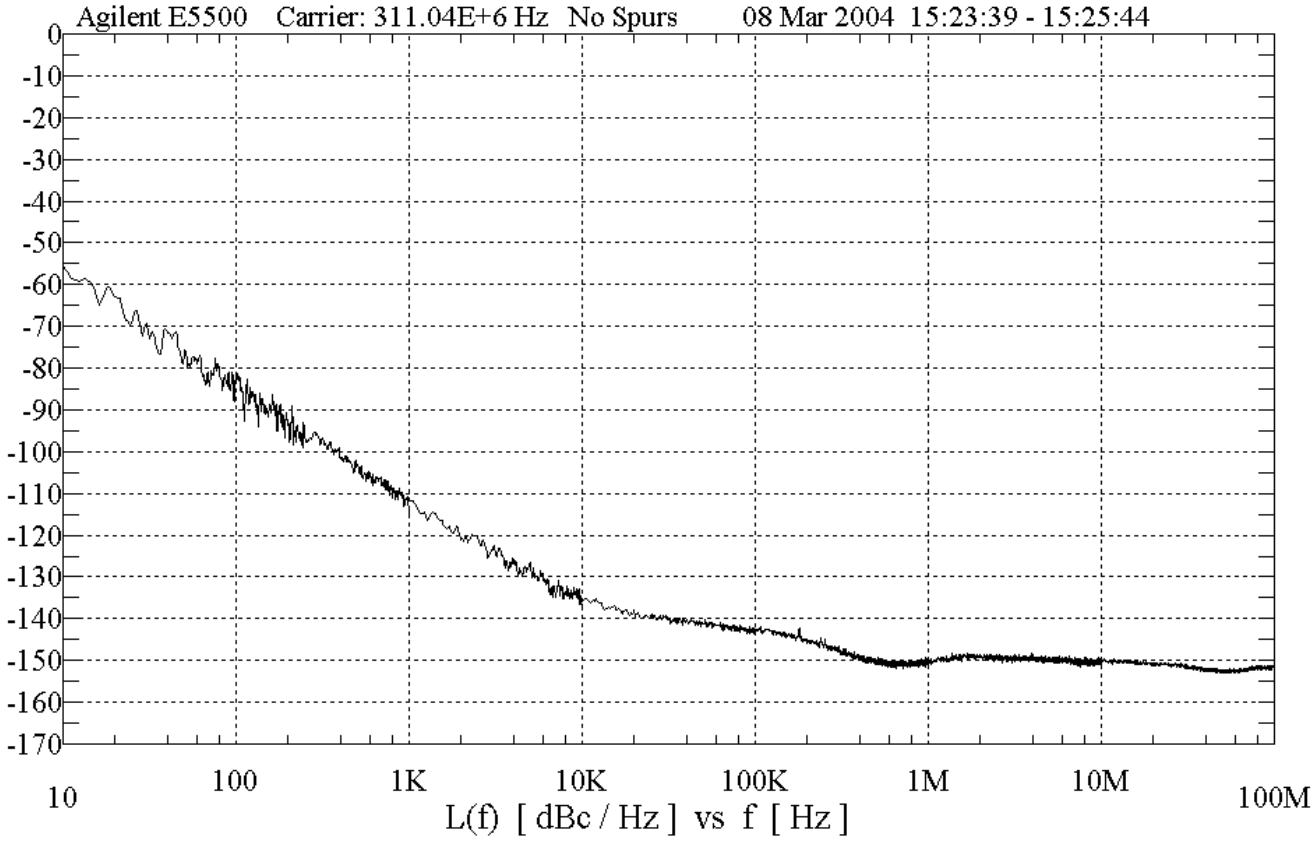


Figure 1: 2x AFM Phase Noise at 311.04MHz

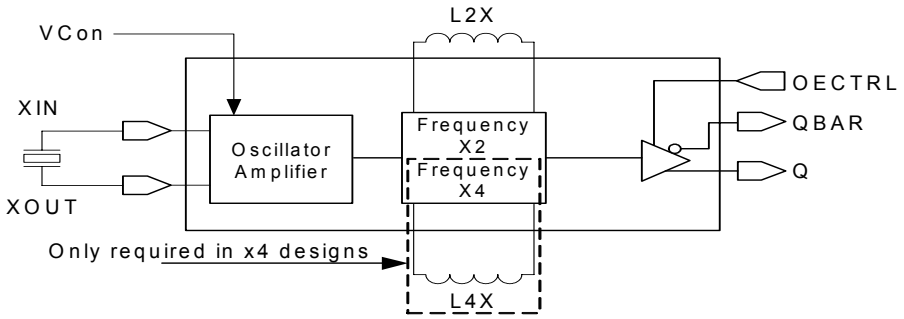


Figure 2: Overall VCXO AFM Block Diagram

FEATURES

- Non Phase Locked Loop frequency multiplication
- Input frequency from 30-200 MHz
- Output frequency from 60-800-MHz
- Low Phase noise and jitter (equivalent to fundamental crystal at the output frequency)
- Unbeatably low jitter
  - RMS phase jitter < 0.25ps (12kHz to 20MHz)
  - RMS period jitter < 2.5 ps
- Low Phase Noise
  - -142 dBc/Hz @ 100kHz Offset from 155.52MHz
  - -150 dBc/Hz @ 10MHz Offset from 155.52MHz
- High linearity pull range (typ. 5%)
- +/- 120 PPM pullability VCXO
- Low cost crystal input eliminates expensive crystals
- Differential output levels (PECL, LVDS), or single-ended CMOS
- Single 2.5V or 3.3V +/- 10% power supply
- Optional industrial temperature range (-40°C to +85°C)
- Available in 16-pin SSOP, and 3x3 QFN

Figure 3 shows the jitter histogram of the 2x Analog Frequency Multiplier at 155.52MHz, while figure 4 shows the very low rejection levels of sub-harmonics that correspond to the exceptionally low jitter performance.

Figure 3: Jitter Histogram at 311.04 MHz
Analog Frequency Multiplier (2x)
with 155.52MHz crystal

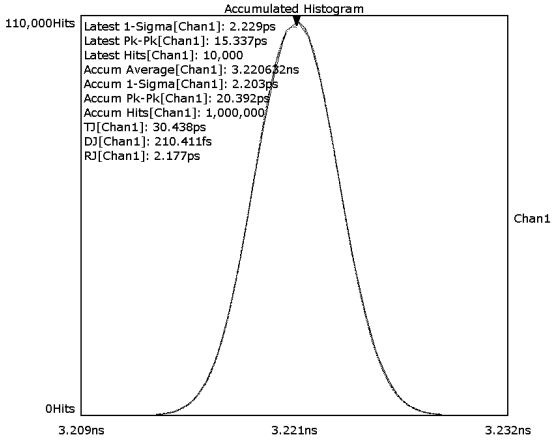
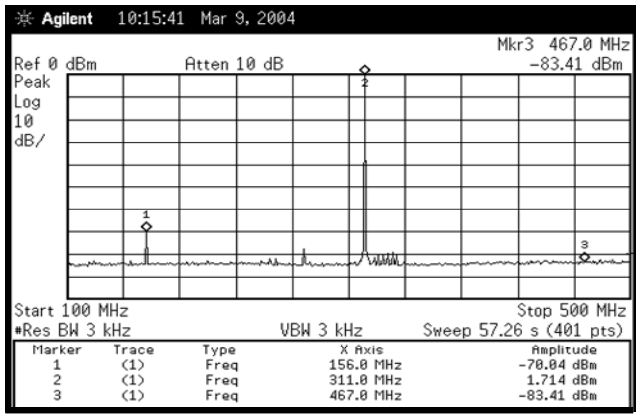


Figure 4: Spectrum Analysis at 311.04 MHz
Analog Frequency Multiplier (2x)
with sub-harmonic below –72 dBc



PRODUCT SELECTION GUIDE

FREQUENCY VERSUS PHASE NOISE PERFORMANCE

Part Number	Input Frequency Range (MHz)	Analog Frequency Multiplication Factor	Output Frequency Range (MHz)	Output Type	Phase Noise AT Frequency Offset From Carrier (dBc/Hz)							
					Carrier Freq. (MHz)	10 Hz	100 Hz	1 KHz	10 KHz	100 KHz	1 MHz	10 MHz
PL560-08	75 - 200	4	300 - 800	PECL	622.08	-55	-85	-110	-130	-137	-148	-150
PL560-09	75 - 200	4	300 - 800	LVDS	622.08	-55	-85	-110	-130	-137	-148	-150
PL560-37	30 - 80	4	120 - 320	CMOS	155.52	-50	-82	-110	-128	-142	-148	-150
PL560-38	30 - 80	4	120 - 320	PECL	155.52	-50	-82	-110	-128	-142	-148	-150
PL560-39	30 - 80	4	120 - 320	LVDS	155.52	-50	-82	-110	-128	-142	-148	-150
PL560-47	30 - 80	2	60 - 160	CMOS	155.52	-65	-95	-122	-138	-142	-148	-149
PL560-48	30 - 80	2	60 - 160	PECL	155.52	-65	-95	-122	-138	-142	-148	-149
PL560-49	30 - 80	2	60 - 160	LVDS	155.52	-65	-95	-122	-138	-142	-148	-149
PL560-68	75 - 200	2	150 - 400	PECL	311.04	-60	-85	-112	-135	-142	-150	-151
PL560-69	75 - 200	2	150 - 400	LVDS	311.04	-60	-85	-112	-135	-142	-150	-151

Phase Noise numbers were obtained using Agilent 5500.

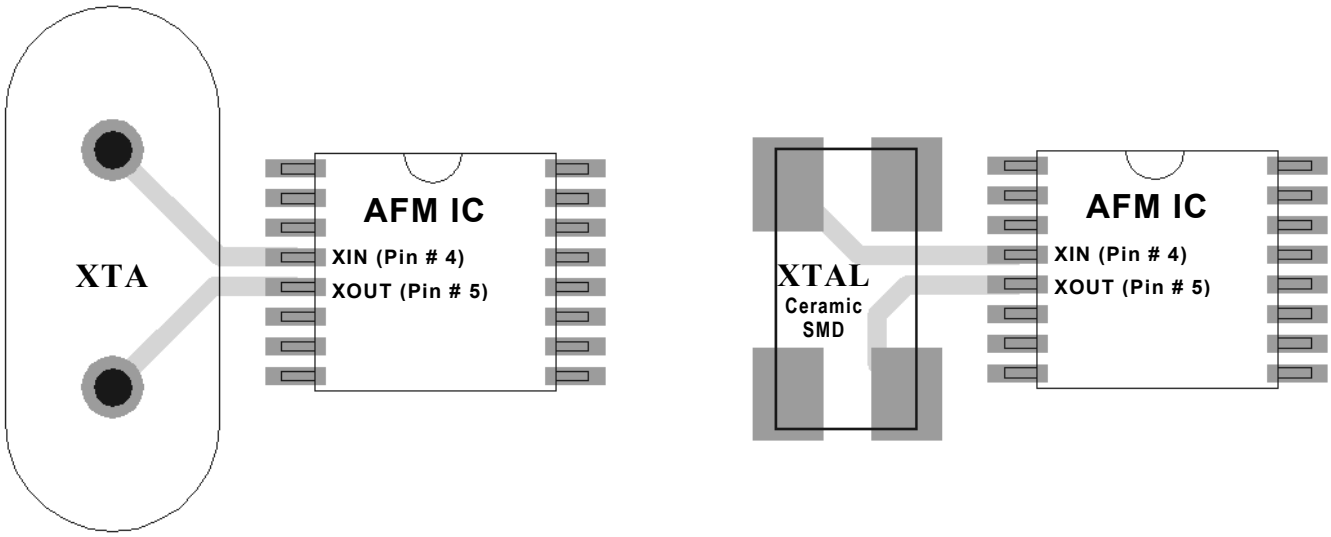
FREQUENCY VERSUS JITTER, AND SUB-HARMONIC PERFORMANCE

Part Number	Jitter Calc. Freq. (MHz)	RMS Period Jitter (Ps)			Peak to Peak Period Jitter (Ps)			RMS Accumulated (L.T.) Jitter (Ps)			Phase Jitter (12 KHz-20MHz) (Ps)			Spectral Specifications / Sub-harmonic Content (dB), Frequency (MHz)						
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Carrier Freq. (Fc)	@ -75% (Fc)	@ -50% (Fc)	@ -25% (Fc)	@ +25% (Fc)	@ +50% (Fc)	@ +75% (Fc)
PL560-08	622		4	6		25	30			6		0.09		622	-50	-50	-45	-47	-47	-55
PL560-09	622		4	6		25	30			6		0.09		622	-50	-50	-45	-47	-47	-55
PL560-37	155		4	6		18	20			6		0.25		155.52	-75	-62			-65	-75
PL560-38	155		4	6		18	20			6		0.25		155.52	-75	-62			-65	-75
PL560-39	155		4	6		18	20			6		0.25		155.52	-75	-62			-65	-75
PL 560-47	155		2.5	3		18	20			3		0.25		155.52		-68			-68	
PL 560-48	155		2.5	3		18	20			3		0.25		155.52		-68			-68	
PL 560-49	155		2.5	3		18	20			3		0.27		155.52		-68			-68	
PL 560-68	311		2.5	3		18	20			3		0.18		311.04		-72			-85	
PL 560-69	311		2.5	3		18	20			3		0.18		311.04		-72			-85	

Note: Wavecrest Data 10,000 hits. No Filtering was used in Jitter Calculations. Agilent 5500 was used for Phase Jitter Calculations. Spectral Specifications were obtained using Agilent E7401A.

CRYSTAL SPECIFICATIONS AND BOARD LAYOUT CONSIDERATIONS

BOARD LAYOUT CONSIDERATIONS



To minimize parasitic effects, and improve performance:

- Place the crystal as close as possible to the IC.
- Make the board traces that are connected to the crystal pins symmetrical.
- The board trace symmetry is important, as it reduces the negative parasitic effects, for a clean frequency multiplication with low jitter. Parasitic have negative effect on frequency pulling of a VCXO and jitter.

CRYSTAL SPECIFICATIONS & TUNING PERFORMANCE

CRYSTAL SPECIFICATIONS						TUNING PERFORMANCE					
PART NUMBER	CRYSTAL RESONATOR FREQUENCY (FXIN)	MODE	CL (xtal)		ESR (RE)	CRYSTAL				TUNING (Typical)	
			CONDI-TIONS	TYP.	Max.	CRYSTAL FREQ (MHz)	C0	C1	C0/C1	VC: 1.65V→ 0V	VC: 1.65V→ 3.4V
PL560-08/09 PL560-68/69	75~200MHz	Funda-mental	At Vcon = 1.65V	5pF	30 Ω	155.52	3.0pF	12.2fF	245	-145 ppm	+108 ppm
						155.52	1.8pF	5.7fF	316	-134 ppm	+87 ppm
PL560-37/38/39 PL560-47/48/49	30~80MHz	Funda-mental	At Vcon = 1.65V	5pF	30 Ω	30.72	2.8pF	12.4fF	228	-167ppm	+176ppm
						30.72	4.5pF	19.1fF	236	-163ppm	+167ppm
						38.88	5.1pF	20.9fF	242	-131ppm	+98ppm
						38.88	5.3pF	25.6fF	207	-157ppm	+141ppm
						77.76	2.0pF	6.7fF	305	-92ppm	+110ppm

Note: Non specified parameters can be chosen as standard values from crystal suppliers.

CL ratings larger than 5pF require a crystal frequency adjustment. Request detailed crystal specifications from PhaseLink.

VOLTAGE CONTROL SPECIFICATION

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time	$T_{VCXOSTB}$	From power valid		10		ms
Linearity				5	10	%
VCXO Tuning Characteristic				70		ppm/V
VCON input impedance			130			kΩ
VCON modulation BW		0V ≤ VCON ≤ 3.3V, -3dB	25			kHz

EXTERNAL COMPONENT VALUES AND DESIGN CONSIDERATIONS

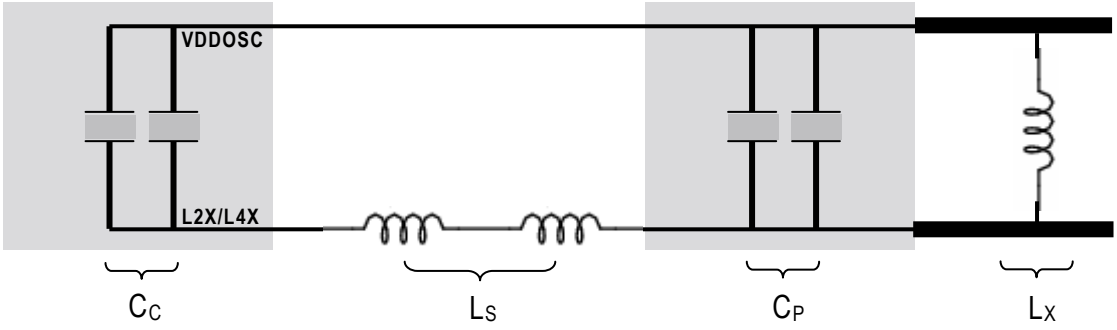


Figure 5: Diagram Representation Of The Related System Inductance And Capacitance

- C_C is the effective capacitance of the bond pad and the capacitor inside the IC.
- L_S is the effective parasitic inductance of the bond wire and the package lead frame/pins.
- C_P is the effective parasitic capacitance of the lead frame, and the board traces.
- L_X is the inductor value that needs to be determined for optimum performance.

INDUCTOR VALUE OPTIMIZATION

The required inductor value(s) for the best performance depends on the operating frequency, and the board layout specifications. The listed values in this datasheet are based on the calculated parasitic values from PhaseLink's evaluation board design (Gerber file available upon request). These inductor values provide the user with a starting point to determine the optimum inductor values. Additional fine-tuning may be required to determine the optimal solution. A method of determining the optimum inductor value(s) required in the system is described below to assist you in fine-tuning your system performance.

DETERMINING THE OPTIMUM INDUCTOR VALUE(S)

STEP 1

Refer to the 'Inductor Value vs. Output Frequency' table (below) to choose a starting value for the L2X inductor. Measure the signal's AC voltage swing on the L2X inductor. This can be accomplished by utilizing an oscilloscope, and a FET probe with

<0.5pF capacitance. The voltage swing can be as high as 3.5Vpp. You can achieve good performance at signal levels above 2.0Vpp, however best performance is achieved with signal levels approaching 3.0Vpp or higher. 1.5Vpp is required to observe an output signal. For the L4X inductor the signal levels should be at least 50% of the L2X signal levels mentioned above.

If at first you do not achieve the required voltage swing, try changing the inductor value to the next closest value and observe for performance improvement. A larger signal swing on the inductor indicates performance improvement, while smaller signal swing on the inductor indicates performance degradation. Try to find the inductor value where the signal levels are the largest.

Important note: The signal level on L4X depends on the value of L2X inductor. You must set the L2X value first.

STEP 2

To fine-tune the inductor value(s) for the optimum performance, use a spectrum analyzer to observe the sub-harmonics. Measure the strength of all the sub-harmonics. Try changing the inductor value(s) to the next closest value and observe for performance improvement. You want to find the inductor value(s) where the harmonics are the lowest. Highest priorities are the 0.5xFc and 1.5xFc harmonics, since the jitter is most sensitive at these values.

Important Note: If your board design is significantly different than PhaseLink's evaluation board design, new parasitic values must be used to calculate the correct inductor value(s) that result in optimum performance. For additional information about determining the parasitic and optimum inductor value(s), please contact PhaseLink or visit us at [www.phaselink.com].

INDUCTOR VALUE VERSUS OUTPUT FREQUENCY
SSOP PACKAGE, BASED ON PHASELINK'S EVALUATION PCB

560-08/09				560-37/38/39				560-47/48/49		560-68/69	
L2X		L4X		L2X		L4X		L2X		L2X	
MHz	nH	MHz	nH	MHz	nH	MHz	nH	MHz	nH	MHz	nH
150	58.76	300	30.20	60	159.15	120	64.73	60	181.30	150	88.29
155	54.89	310	28.00	62	148.63	124	60.32	62	169.38	155	82.31
160	51.37	320	26.00	64	139.09	128	56.32	64	158.56	160	76.89
165	48.17	330	24.18	66	130.39	132	52.67	66	148.71	165	71.95
170	45.24	340	22.52	68	122.45	136	49.34	68	139.71	170	67.44
175	42.57	350	21.00	70	115.19	140	46.29	70	131.48	175	63.31
180	40.11	360	19.60	72	108.52	144	43.49	72	123.92	180	59.52
185	37.85	370	18.31	74	102.38	148	40.92	74	116.97	185	56.03
190	35.76	380	17.13	76	96.72	152	38.54	76	110.56	190	52.81
195	33.83	390	16.03	78	91.49	156	36.34	78	104.63	195	49.84
200	32.04	400	15.02	80	86.64	160	34.30	80	99.15	200	47.08
205	30.38	410	14.07	82	82.15	164	32.41	82	94.06	205	44.53
210	28.84	420	13.20	84	77.97	168	30.65	84	89.33	210	42.15
215	27.40	430	12.38	86	74.08	172	29.01	86	84.92	215	39.94
220	26.06	440	11.62	88	70.45	176	27.48	88	80.81	220	37.87
225	24.81	450	10.91	90	67.06	180	26.05	90	76.98	225	35.94
230	23.64	460	10.24	92	63.89	184	24.72	92	73.39	230	34.13
235	22.54	470	9.62	94	60.92	188	23.46	94	70.02	235	32.44
240	21.51	480	9.03	96	58.13	192	22.28	96	66.87	240	30.85
245	20.54	490	8.48	98	55.51	196	21.17	98	63.90	245	29.36
250	19.62	500	7.96	100	53.05	200	20.13	100	61.12	250	27.95
255	18.76	510	7.47	102	50.73	204	19.14	102	58.49	255	26.63
260	17.95	520	7.01	104	48.54	208	18.21	104	56.01	260	25.38
265	17.18	530	6.58	106	46.47	212	17.33	106	53.68	265	24.19
270	16.45	540	6.17	108	44.52	216	16.50	108	51.47	270	23.08
275	15.76	550	5.78	110	42.67	220	15.71	110	49.38	275	22.02
280	15.11	560	5.41	112	40.92	224	14.96	112	47.40	280	21.02
285	14.49	570	5.06	114	39.26	228	14.25	114	45.53	285	20.07
290	13.90	580	4.72	116	37.69	232	13.58	116	43.75	290	19.16
295	13.34	590	4.41	118	36.19	236	12.94	118	42.06	295	18.30
300	12.81	600	4.10	120	34.77	240	12.32	120	40.45	300	17.49
305	12.30	610	3.82	122	33.42	244	11.74	122	38.92	305	16.71
310	11.82	620	3.54	124	32.13	248	11.18	124	37.47	310	15.97
315	11.36	630	3.28	126	30.90	252	10.65	126	36.08	315	15.26
320	10.92	640	3.03	128	29.73	256	10.14	128	34.76	320	14.59
325	10.49	650	2.80	130	28.61	260	9.65	130	33.50	325	13.94
330	10.09	660	2.57	132	27.54	264	9.18	132	32.30	330	13.32
335	9.70	670	2.35	134	26.52	268	8.74	134	31.15	335	12.73
340	9.33	680	2.14	136	25.54	272	8.31	136	30.05	340	12.17
345	8.97	690	1.94	138	24.61	276	7.89	138	28.99	345	11.62
350	8.63	700	1.75	140	23.71	280	7.50	140	27.98	350	11.10
355	8.30	710	1.57	142	22.85	284	7.11	142	27.02	355	10.60
360	7.98	720	1.39	144	22.03	288	6.75	144	26.09	360	10.12
365	7.68	730	1.22	146	21.24	292	6.39	146	25.20	365	9.66
370	7.39	740	1.05	148	20.48	296	6.05	148	24.35	370	9.22
375	7.10	750	0.90	150	19.75	300	5.72	150	23.53	375	8.79
380	6.83	760	0.75	152	19.05	304	5.40	152	22.75	380	8.38
385	6.57	770	0.60	154	18.38	308	5.09	154	21.99	385	7.98
390	6.31	780	0.46	156	17.73	312	4.79	156	21.26	390	7.60
395	6.06	790	0.32	158	17.10	316	4.50	158	20.56	395	7.23
400	5.82	800	0.19	160	16.50	320	4.22	160	19.89	400	6.87

Note: The industry standard inductor values may be different than the stated inductor values in the above table. Please select the closest industry standard inductor value and 'fine tune' the system performance, as stated earlier. The listed inductor values, in the above table, are based on the calculated parasitic values from PhaseLink's evaluation board design. We recommend using high Q, small size 0402 or 0603 SMD inductors. Place this inductor between L2X and VDD. For additional information about determining the parasitic and optimum inductor values, please contact PhaseLink or visit us at [www.phaselink.com].

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

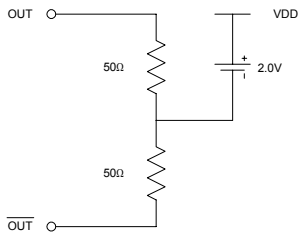
PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	-40	+85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

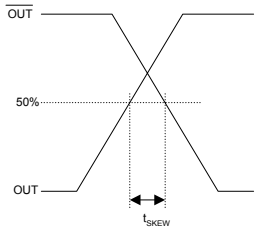
PECL ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (with loaded outputs)	I_{DD}	Fout = 622.08		75*	80*	mA
Operating Voltage	V_{DD}		2.97		3.63	V
Output Clock Duty Cycle		@ Vdd – 1.3V	45	50	55	%
Short Circuit Current				±50		mA
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V)	V_{DD} – 1.025			V
Output Low Voltage	V_{OL}				V_{DD} – 1.620	V
Clock Rise Time	t_r	@20/80%		0.4	0.7	ns
Clock Fall Time	t_f	@80/20%		0.4	0.7	ns

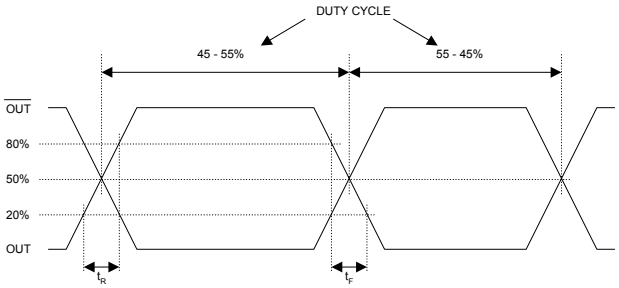
PECL Levels Test Circuit



PECL Output Skew



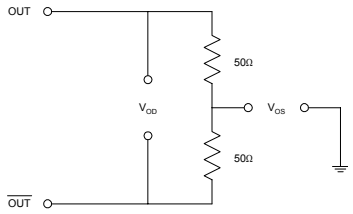
PECL Transistion Time Waveform



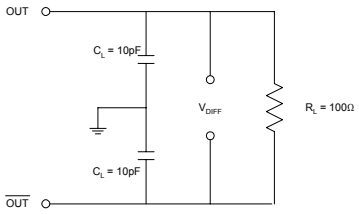
LVDS ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (with loaded outputs)	I_{DD}	Fout = 622.08, LVDS		55*	60*	mA
Operating Voltage	V_{DD}		2.97		3.63	V
Output Clock Duty Cycle		@ 1.25V (LVDS)	45	50	55	%
Short Circuit Current				±50		mA
Output Differential Voltage	V_{OD}	R_L = 100 W (see figure)	247	355	454	mV
VDD Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND VDD = 0V		±1	±10	µA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA
Differential Clock Rise Time	t_r	R_L = 100 W CL = 10 pF (see figure)	0.2	0.5	0.7	ns
Differential Clock Fall Time	t_f		0.2	0.5	0.7	ns

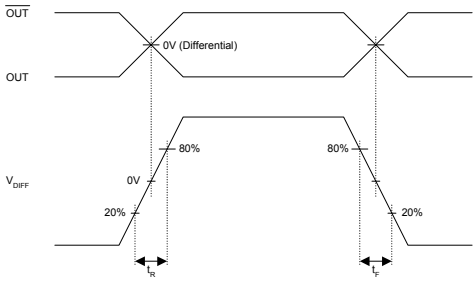
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform

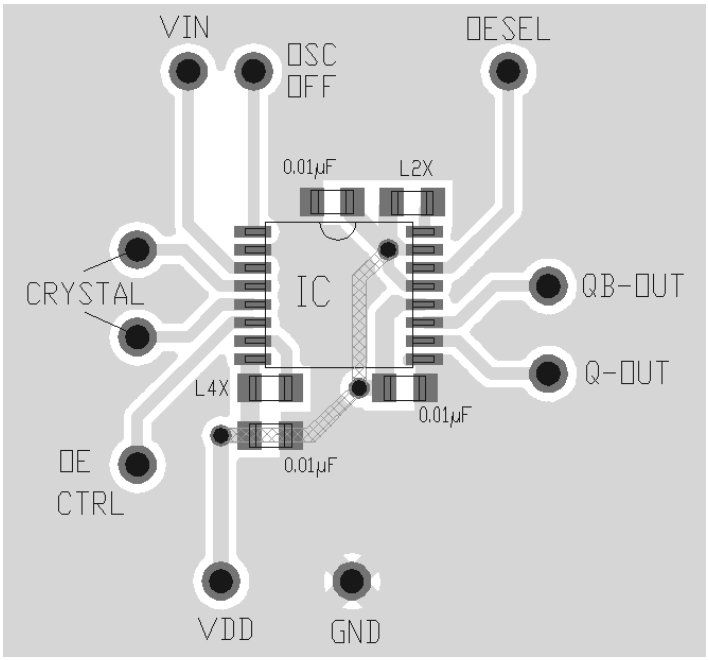


CMOS ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Clock Rise/Fall Time		10% ~ 90% VDD with 10 pF load		1.2	1.6	ns
Output Clock Duty Cycle		Measured @ 50% VDD	45	50	55	%
Short Circuit Current				±50		mA

BOARD LAYOUT DESIGN CONSIDERATIONS FOR 4X AFMs

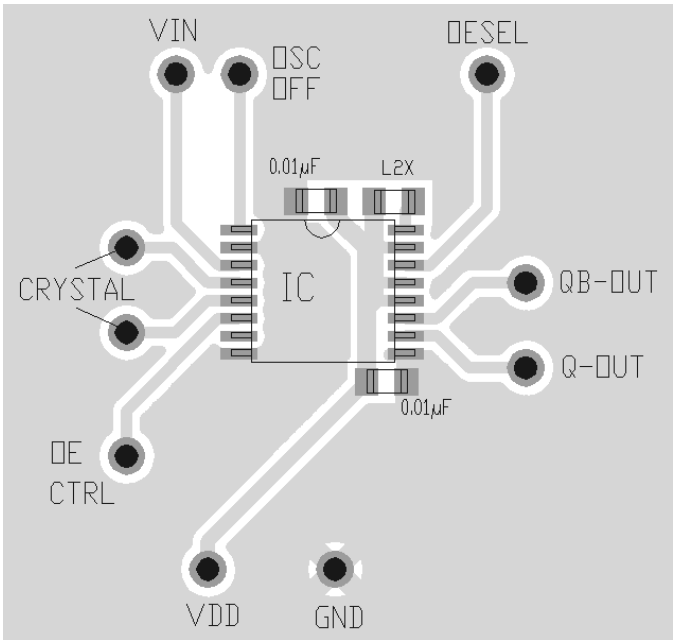
- Place L2X inductor as close as possible to the L2X [pin # 16], and adjacent to VDD [pin # 15].
- Place L4X inductor as close as possible to the L4X [pin # 7], and adjacent to VDD [pin # 8].
- Place a 0.01uF~0.1uF capacitor as close as possible to the VDDBUF [pin # 12] and GNDBUF [pin # 9].
- Place a 0.01uF~0.1uF capacitor as close as possible to the VDDOSC [pin # 15] and GNDOSC [pin # 2].
- Place a 0.01uF~0.1uF capacitor as close as possible to VDD [pin # 8] and GNDBUF [pin # 9].
- Place the crystal as close as possible to both crystal pins for the best frequency pulling and the least cross-talk of the crystal signal to the output. **Important**: Crystal traces must be symmetrical.
- Try to avoid a direct connection between VDDBUF [pin # 12) and adjacent VDDANA [pin # 13], to prevent cross-talk from 0.5xFc into the output buffer.



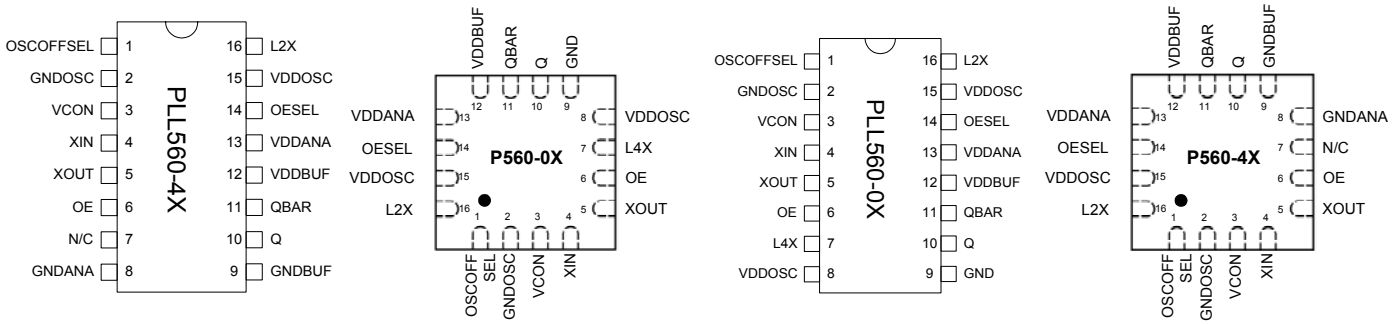
BOARD LAYOUT DESIGN CONSIDERATIONS FOR 2X AFMs

- Place L2X inductor as close as possible to the L2X [pin # 16], and the adjacent VDDOSC [pin # 15].
- Place a 0.01µF~0.1µF capacitor as close as possible to the VDDBUF [pin # 12] and GNDBUF [pin # 9].
- Place a 0.01µF~0.1µF capacitor as close as possible to the VDDOSC (Pin # 15) and GNDOSC (Pin # 2).
- Place the crystal as close as possible to both crystal pins for the least cross-talk of the crystal signal to the output. **Important**: Crystal traces must be symmetrical.

Note: Please contact PhaseLink for the Gerber files of the above board layouts.



PACKAGE PIN DESCRIPTION AND ASSIGNMENT



Name	Pin#	Type	Product	Description
OSCOFFSEL	1	I	2X	No Connection.
			4X	Set to "0" (GND) to choose to turn off the oscillator when outputs are disabled (OE). Default (no connect) is OSC always on.
GNDOSC	2	P	2X & 4X	GND connection for oscillator circuitry.
VCON	3	I	2X & 4X	Control Voltage input. Use this pin to change the output frequency by varying the applied Control Voltage.
XIN	4	I	2X & 4X	Input from crystal oscillator circuitry.
XOUT	5	O	2X & 4X	Output from crystal oscillator circuitry.
OECTRL	6	I	2X & 4X	Output Enable input (see "OE LOGIC SELECTION TABLE").
L4X	7	I	2X	DNC (Do Not Connect).
			4X	Set to "0" (GND) to choose to turn off the oscillator when outputs are disabled (OE). Default (no connect) is OSC always on.
GNDANA	8	P	2X	GND connection.
VDDOSC			4X	VDD connection for oscillator circuitry.VDDOSC should be separately decoupled from other VDDs whenever possible.
GNDBUF	9	P	2X & 4X	GND connection for output buffer circuitry.
Q	10	O	2X & 4X	PECL/LVDS or CMOS output.
QBAR	11	O	2X & 4X	Complementary PECL/LVDS output or same phase CMOS.
VDDBUF	12	P	2X & 4X	VDD connection for output buffer circuitry. VDDBUF should be separately decoupled from other VDDs whenever possible.
VDDANA	13	P	2X & 4X	VDD connection for analog circuitry. VDDANA should be separately decoupled from other VDDs whenever possible.
OESEL	14	I	2X & 4X	Selector input to choose the OE control logic (see "OE SELECTION TABLE".
VDDOSC	15	P	2X & 4X	VDD connection for oscillator circuitry. VDDOSC should be separately decoupled from other VDDs whenever possible.
L2X	16	I	2X & 4X	External inductor connection. The inductor is recommended to have a high Q value and must be placed between L2X and VDD.

OE LOGIC SELECTION

OUTPUT	OESEL	OE	Output State
PECL	0 (Default)	0 (Default)	Enabled
		1	Tri-state
	1	0	Tri-state
		1 (Default)	Enabled
LVDS or CMOS	0 (Default)	0	Tri-state
		1 (Default)	Enabled
	1	0 (Default)	Enabled
		1	Tri-state

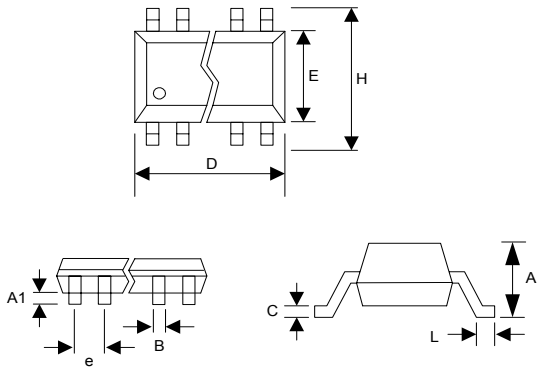
OESEL and OE: Connect to VDD to set to "1", connect to GND to set to "0". Internally set to default through pull-down / -up.

PACKAGE INFORMATION

16 PIN TSSOP

16 PIN TSSOP (mm)

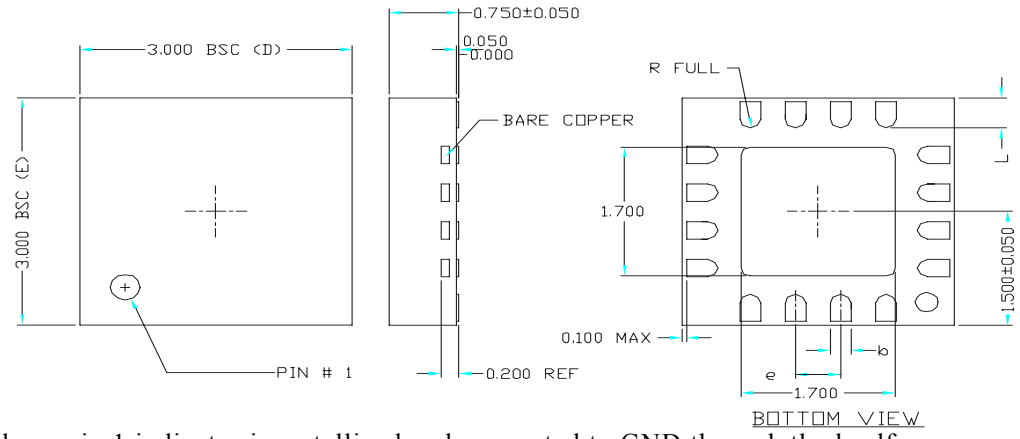
	TSSOP	
Symbol	Min.	Max.
A	-	1.20
A1	0.05	0.15
B	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.40 BSC	
L	0.45	0.75
e	0.65 BSC	



16 PIN 3x3 QFN

VARIATIONS:

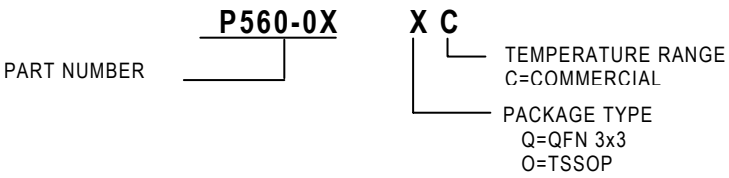
SYMBOL	16 LD		
	MIN	NOM	MAX
e	0.50 BSC		
b	0.18	0.23	0.30
L	0.30	0.40	0.50
ND	4		
NE	4		



Important note: QFN package pin 1 indicator is metallized and connected to GND through the leadframe.

ORDERING INFORMATION

Note: The order number for this device is a combination of Device number, Package type and Operating temperature range.



Order Number	Marking	Package Option
PL560-XXQC-R	P560-XX	QFN – Tape and Reel
PL560-XXOC-R	P560-XX OC	TSSOP – Tape and Reel
PL560-XXQC	P560-XX	QFN – Tube
PL560-XXOC	P560-XX OC	TSSOP – Tube

ORDERING INFORMATION

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