
PRODUCT SPECIFICATION

12864Z

128×64 GRAPHICS OLED DISPLAY MODULE



VGY12864Z

Yellow



VGG12864Z

Green

CONTENT

1	Overview	3
2	Features	3
3	Mechanical Data	3
4	Recommended Operation Conditions	4
5	Electrical Characteristics.....	4
6	Module Drawing	5
7	Function Block Diagram.....	8
8	Module Interface	8
9	Timing Characteristics	11
10	Display Control Instruction.....	14
11	Graphic Display Data Ram Address Map	19
12	Precautions for operation and Storage	21
	12.1 Precautions for Operation	21
	12.2 Soldering.....	21
	12.3 Precautions for Storage	21
	12.4 Warranty period.....	21
	12.5 Test Status	22

History of Specification Revision

Date	Rev.	Contents	Remark
2006.5	Initial	Release	Named
2007.3	Rev2.0	Add VGG12864Z-S001	Page 5 8
2007.4	Rev2.1	Unify voltage value	Page 4

1 Overview

12864Z is an OLED monochrome 128×64 · 16 Gray Scale dot matrix display module. The characteristics of this display module are high brightness, self-emission, high contrast ratio, slim/thin outline, wide viewing angle, wide temperature range, and low power consumption.

The module displays data directly from its internal 128x80x4 bits Graphic Display Data RAM(GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

The embedded on-chip oscillator and DC-DC voltage converter reduce the number of external components.

2 Features

- 128×64 pixels
- High contrast ratio
- Wide viewing angle
- Wide range of operating temperature
- low power consumption
- 8-bit 8080-Databus or 8-bit 6800-series parallel interface or series peripheral interface(S003 & S005 only have 8-bit 8080-Databus and series peripheral interface)
- Display data is stored in Display Data RAM from MPU
- Power supply to logic system: +3V±10%
- Power supply to OLED driving system: +12V to +16V
- Built-in Solomon SSD1325 standard OLED controller

3 Mechanical Data

NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128(Columns) x 64(rows)	
2	Dot Size	0.45(W) x 0.45 (H)	mm
3	Dot Pitch	0.48 (W) x 0.48 (H)	mm
4	Aperture Rate	67.2	%
5	Active Area	61.41 (W) x 30.69 (H)	m ²
6	Panel Size	75(W) x 41.86 (H) x2.16(T)	mm
7	Module Size	75 (W) x 53.5 (H) x 5(MAX) (T)	mm

8	Polarizer	with	
9	Duty	1/64	

4 Recommended Operation Conditions

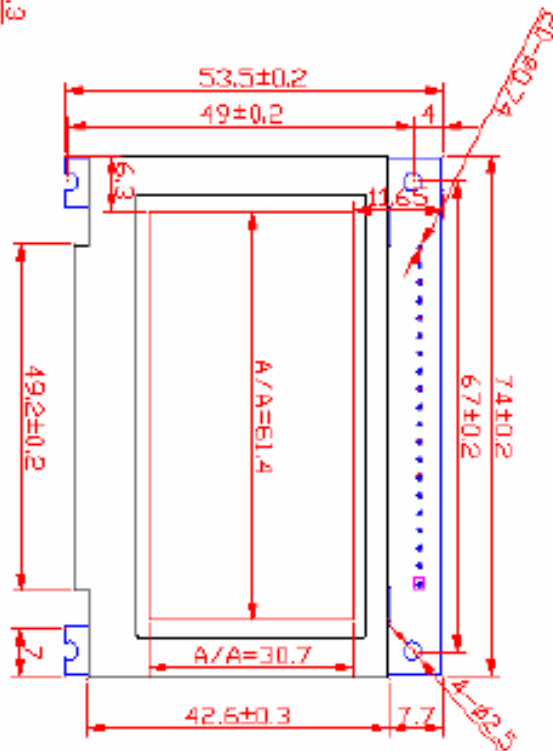
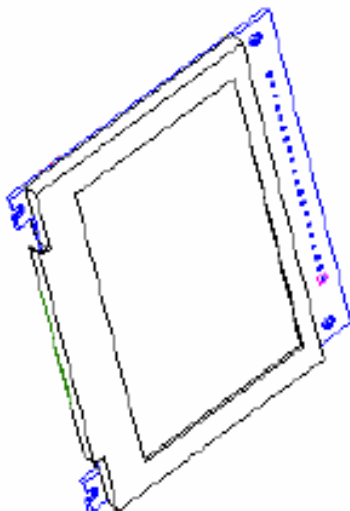
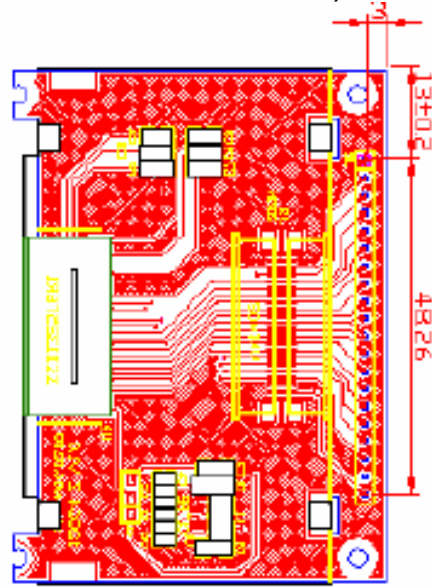
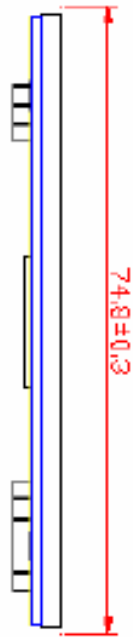
Symbol	ITEM	MIN	TYP	MAX	UNIT
V _{DD}	Logic supply voltage	2.4	3.0 (Z-S002)	3.5	V
		4.5	5.0 (Z-S005)	5.5	
V _{CC}	Operating voltage	12	14	16	V
T _{op}	Operating Temp.	-20	-	+70	°C
T _{stg}	Storage Temp	-30	-	+80	°C

5 Electrical Characteristics

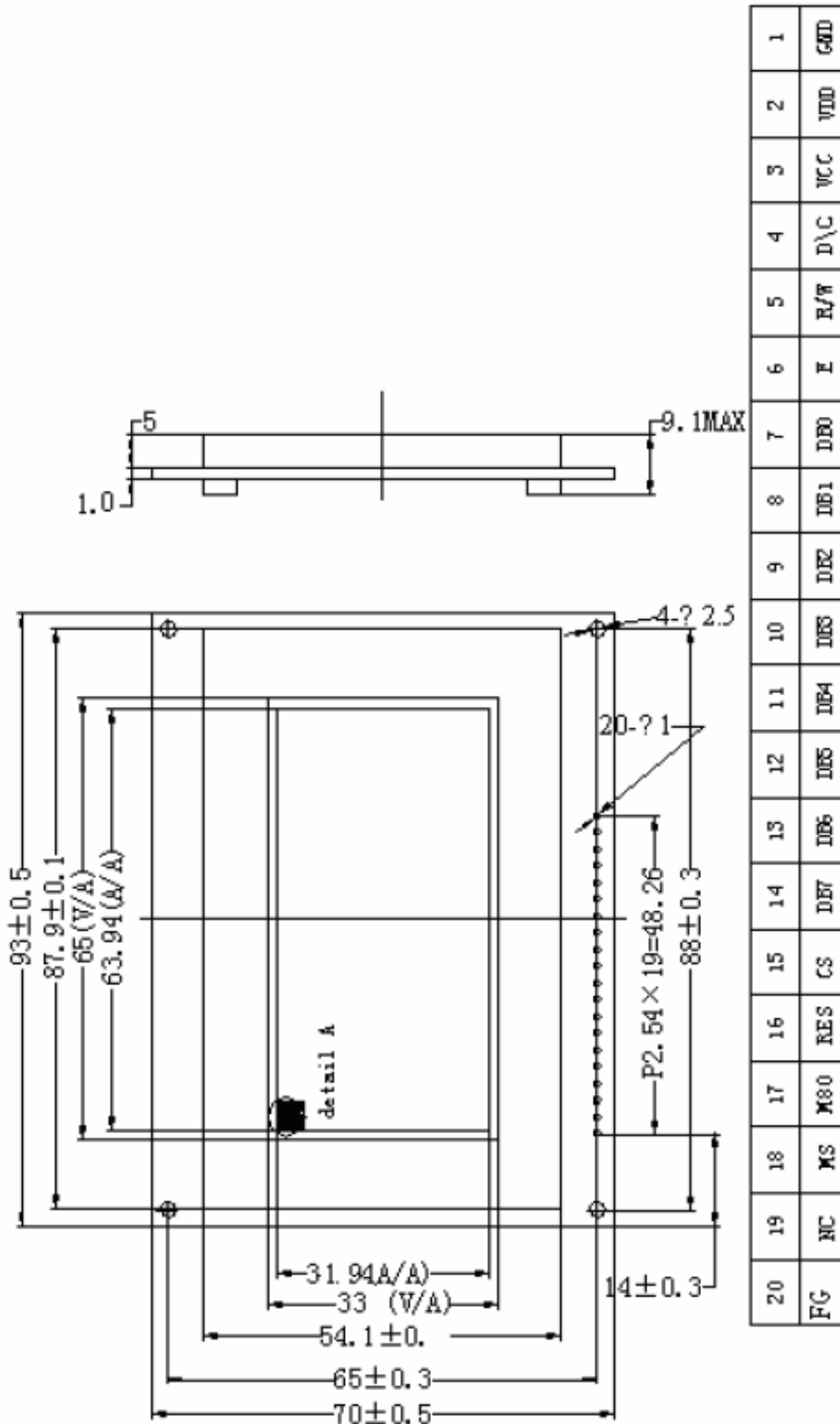
symbol	ITEM	Test condition	MIN	TYP	MAX	Unit
I _{CC}	Operating supply Current	VDD=3.0	-	18	-	mA
I _{DD}	Logic supply Current	VCC=14.0	-	-	-	mA
p _T	Total Power	Note: 40cd/m ² T _{op} =25°C	-	-	250	mW
V _{IH}	Digital Input HIGH	-	2.4	-	3.5	Volts
V _{IL}	Digital Input LOW	-	0	-	0.2V _{DD}	Volts
F _{FRM}	Frame Frequency					Hz

Note: 40cd/m² with polarization film, be equal to 100cd/m²

(VGG12864Z-S002,VGG12864Z-S005)

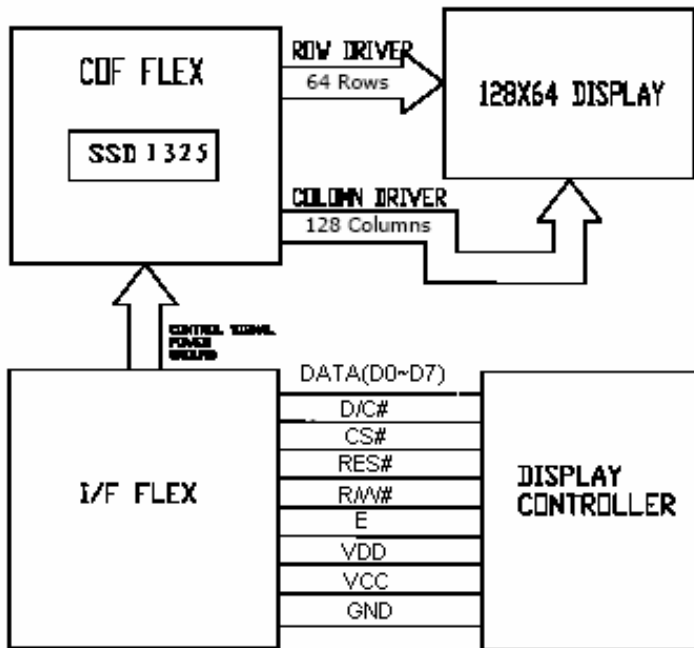


(VGG12864Z-S003)



7 Function Block Diagram

128X64Z OLED Module



NOTE: Some pins omitted

8 Module Interface

VGG12864Z-S001

PIN NAME	PIN NO	DESCRIPTION
NC	1	No Connection
VCC	2	OLED drive voltage 12~16V, It should be supplied externally (S001) .
VCOMH	3	This is an input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
IREF	4	This is a segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10uA.
D7-D0	5-12	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D1 will be the serial data input, SDIN, and D0 will be the serial clock input, SCLK.
E(RD#)	13	This is a MCU interface input pin. When 6800-series Parallel Interface is selected, this pin is used as Enable (E) signal. Read/Write operation is initiated when this pin is pulled HIGH and the CS# pin is pulled LOW. When 8080-series Parallel Interface is selected, this pin is used to receive the Read Data (RD#) signal. Data read operation is initiated when this pin is pulled LOW and CS# pin is pulled LOW.

R/W(WR#)	14	This is a MCU interface input pin. When 6800-series Parallel Interface mode is selected, this pin is used as Read/Write (R/W) selection input. Pull this pin to HIGH for read mode and pull it to LOW for write mode. When 8080-series Parallel Interface mode is selected, this pin is used as Write (WR#) selection input. Pull this pin to LOW for write mode. Data write operation is initiated when this pin is pulled LOW and the CS# is pulled LOW.			
D/C	15	Data/Command Select. This is the Data/Command control pin. When it is pulled HIGH, the input at D7-D0 is treated as display data. When it is pulled LOW, the input at D7-D0 is transferred to the command registers. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.			
RES#	16	Reset, active low			
CS#	17	Chip Select, active low			
NC	18	No Connection			
BS2	19	These are MCU interface input selection pins. See the following table for selecting different interfaces:			
			6800-parallel interface	8080-parallel interface	Serial interface
BS1	20	BS1	0	1	0
		BS2	1	1	0
VDD	21	Logic Voltage +3V			
NC	22	No Connection			
NC	23	No Connection			
NC	24	No Connection			
VBREF	25	This is an internal voltage reference pin for booster circuit. A stabilization capacitor, typ. 1uF, should be connected to Vss.			
NC	26	No Connection			
NC	27	No Connection			
Vddb	28	This is a power supply pin for the internal buffer of the DC-DC voltage converter. It must be connected to VDD when the converter is used.			
NC	29	No Connection			
VSS	30	Ground			
NC	31	No Connection			

VGG12864(Z-S002 Z-S003 Z-S005)

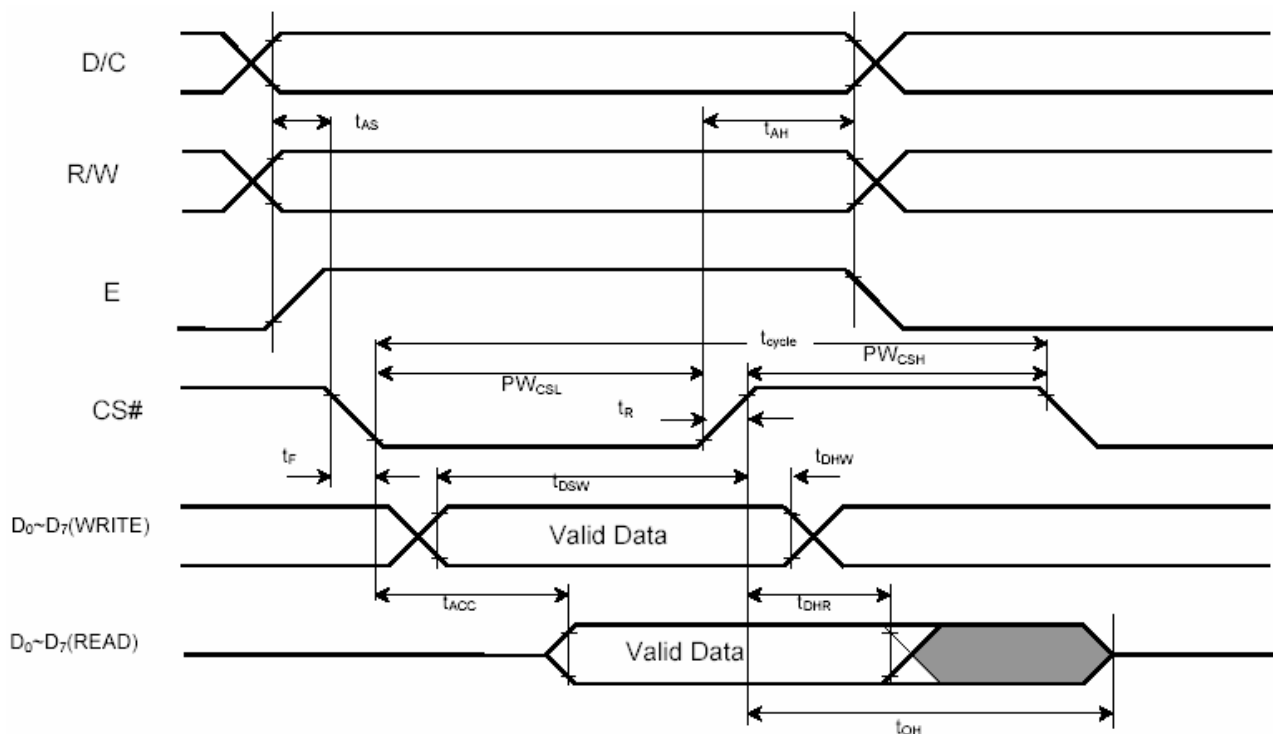
PIN NAME	PIN NO	DESCRIPTION			
GND	1	Ground			
VDD	2	Logic Voltage +3V(S002) +5V(S003 S005)			
VCC	3	OLED drive voltage +14V (Don't care.)			
D/C#	4	Data/Command Select. This is the Data/Command control pin. When it is pulled HIGH, the input at D7-D0 is treated as display data. When it is pulled LOW, the input at D7-D0 is transferred to the command registers. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.			
R/W#	5	This is a MCU interface input pin. When 6800-series Parallel Interface mode is selected, this pin is used as Read/Write (R/W) selection input. Pull this pin to HIGH for read mode and pull it to LOW for write mode. When 8080-series Parallel Interface mode is selected, this pin is used as Write (WR#) selection input. Pull this pin to LOW for write mode. Data write operation is initiated when this pin is pulled LOW and the CS# is pulled LOW.			
E(RD#)	6	This is a MCU interface input pin. When 6800-series Parallel Interface is selected, this pin is used as Enable (E) signal. Read/Write operation is initiated when this pin is pulled HIGH and the CS# pin is pulled LOW. When 8080-series Parallel Interface is selected, this pin is used to receive the Read Data (RD#)signal. Data read operation is initiated when this pin is pulled LOW and CS# pin is pulled LOW.			
D0-D7	7-14	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D1 will be the serial data input, SDIN, and D0 will be the serial clock input, SCLK.			
CS#	15	Chip Select,active low			
RES#	16	Reset,active low			
M80/68#	17	These are MCU interface input selection pins. S003 & S005 only have 8-bit 8080-Databus and series peripheral interface. See the following table for selecting different interfaces:			
MS	18	Ttable	6800-paralle interface	8080-parallel interface	Serial interface
		M80/68#	0	1	0
		MS	1	1	0
E(RD#)	19	The same to Pin6 (S003 & S005); NC(S002 & S004)			
FG	20	Frame Ground			

9 Timing Characteristics

VGG12864Z

6800-Series MPU Parallel Interface Timing Characteristics (VDD - VSS = 2.4 to 3.5V, TA =25°C)

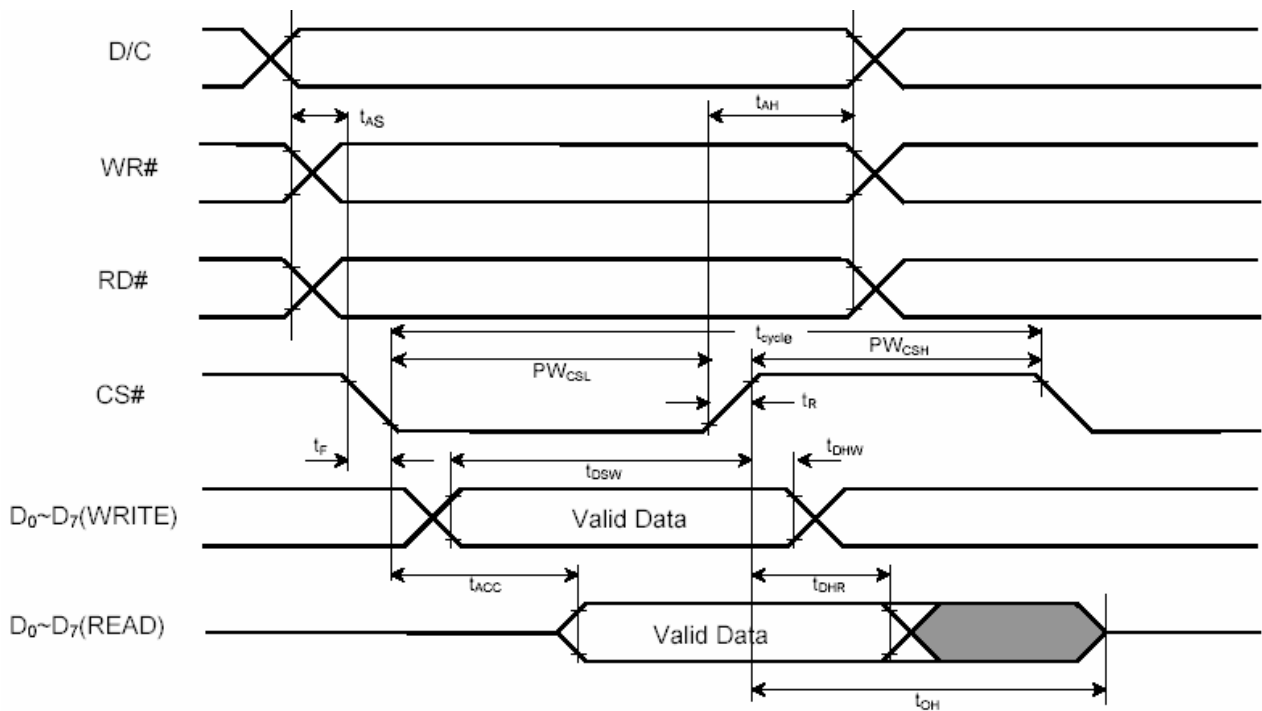
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



6800-series MPU parallel interface characteristics(S002)

8080-Series MPU Parallel Interface Timing Characteristics (VDD - VSS = 2.4 to 3.5V, TA =25°C)

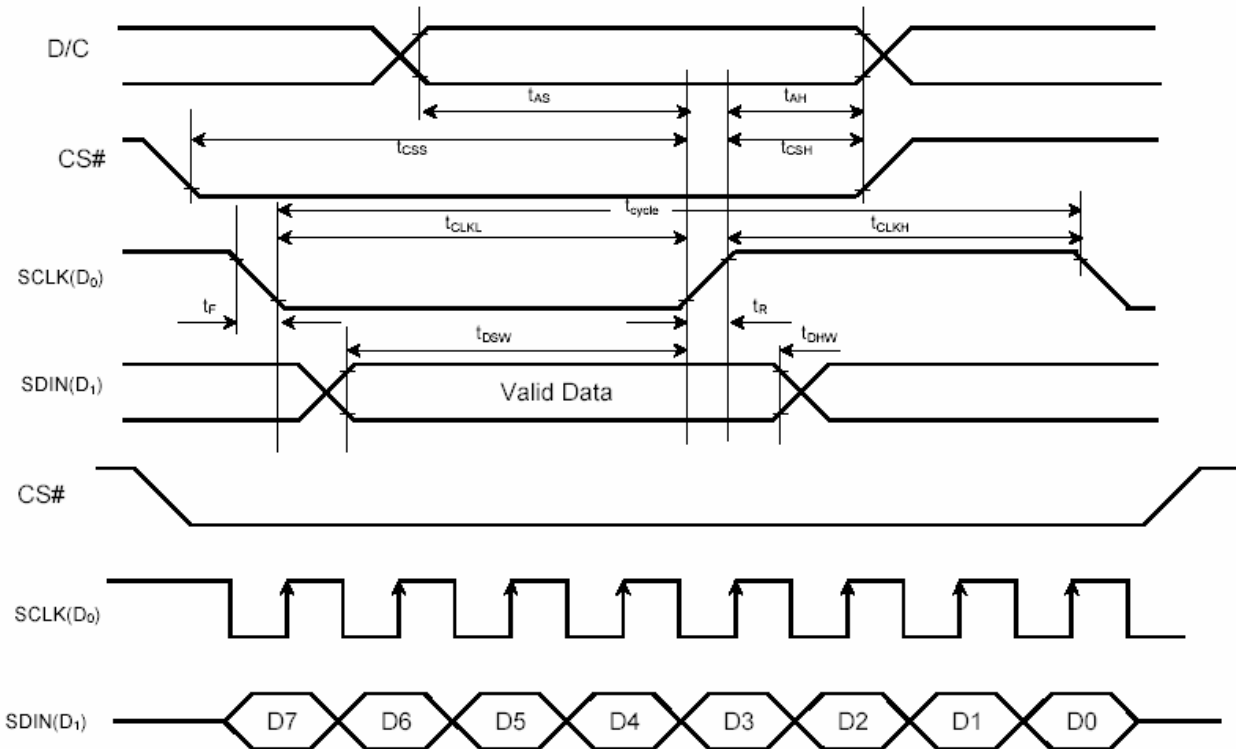
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



8080-series MPU parallel interface characteristics(S002 S003 S005)

Serial Interface Timing Characteristics (VDD - VSS = 2.4 to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



Serial interface characteristics(S002 S003 S005)

10 Display Control Instruction

Table 12 - Command Table

Command table (D/C =0, R/W (WR#)=0, E (RD#)=1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	15	0	0	0	1	0	1	0	1	Set Column Address	Second command A[5:0] sets the column start address from 0-63, POR = 00H. Third command B[5:0] sets the column end address from 0-63, POR = 3FH.
0	A[5:0]	*	*	A5	A4	A3	A2	A1	A0		
0	B[5:0]	*	*	B5	B4	B3	B2	B1	B0		
0	75	0	1	1	1	0	1	0	1	Set Row address	Second command A[6:0]sets the row start address from 0-79, POR = 00H. Third command B[6:0] sets the row end address from 0-79, POR = 4FH.
0	A[6:0]	*	A6	A5	A4	A3	A2	A1	A0		
0	B[6:0]	*	B6	B5	B4	B3	B2	B1	B0		
0	81	1	0	0	0	0	0	0	1	Set Contrast Control Register	Double byte command to select 1 out of 128 contrast steps. Contrast increases as level increase. The level is set to 40H after POR
0	A[6:0]	*	A6	A5	A4	A3	A2	A1	A0		
0	84~86	1	0	0	0	0	1	X1	X0	Set Current Range	84H = Quarter Current Range (POR) 85H = Half Current Range 86H = Full Current Range
0	A0	1	0	1	0	0	0	0	0	Set Re-map	A[0]=0, Disable Column Address Re-map (POR) A[0]=1, Enable Column Address Re-map A[1]=0, Disable Nibble Re-map (POR) A[1]=1, Enable Nibble Re-map A[2]=0, Horizontal Address Increment (POR) A[2]=1, Vertical Address Increment A[4]=0, Disable COM Re-map
0	A[6:0]	*	A6	A5	A4	A3	A2	A1	A0		

											disable (POR) A[4]=1, Enable COM Re-map A[5]=0, Reserved (POR) A[5]=1, Reserved A[6]=0, Disable COM Split Odd Even (POR) A[6]=1, Enable COM Split Odd Even
0 0	A1 A[6:0]	1 *	0 A6	1 A5	0 A4	0 A3	0 A2	0 A1	1 A0	Set Display Start Line	Set display RAM display start line register from 079. Display start line register is reset to 00H after POR.
0 0	A2 A[6:0]	1 *	0 A6	1 A5	0 A4	0 A3	0 A2	1 A1	0 A0	Set Display Offset	Set vertical scroll by COM from 0-79. The value is reset to 00H after POR.
0	A4~A7	1	0	1	0	0	X2	X1	X0	Set Display Mode	A4H = Normal Display (POR) A5H = Entire Display On, all pixels turns on in GS level 15 A6H = Entire Display Off, all pixels turns off A7H = Inverse Display
0 0	A8 A[6:0]	1 *	0 A6	1 A5	0 A4	1 A3	0 A2	0 A1	0 A0	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-80MUX, POR=4FH(80MUX)
0	AD	1	0	1	0	1	1	0	1	Set Master Configuration	A[0] = 0, Disable DC-DC converter
0	A[1:0]	*	*	*	*	*	*	A1	A0		A[0] = 1, Enable DC-DC converter (POR)
											A[1] = 0, Disable internal VCOMH
											A[1] = 1, Enable internal VCOMH (POR)

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12864Z

0	AE~AF	1	0	1	0	X3	1	1	1	Set Display On/Off	AEH = Display Off (Sleep mode) (POR) AFH = Display On
0	BE	1	0	1	1	1	1	1	0	Set VCOMH Voltage	Second command A[5:0] sets the VCOMH voltage
0	A[5:0]	*	*	A5	A4	A3	A2	A1	A0		level 000000-011111
											A[5:0] = 1xxxxx = 1.0*VREF
											A[5:0] = 010001(POR)
0	BC	1	0	1	1	1	1	0	0	Set Precharge Voltage	Second command A[7:0] sets the precharge voltage level
0	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0		0000000-00011111
											A[7:0] = 1xxxxxxx connects to VCOMH
											A[7:0] = 001xxxxx equals 1.0*VREF
											A[7:0] = 00011000(POR)
0	B1	1	0	1	1	0	0	0	1	Set Phase Length	A[3:0] = P1, phase 1 period of 1-15 DCLK clocks,
0	A[3:0]	*	*	*	*	A3	A2	A1	A0		POR = 3DLKS = 3H
0	A[7:4]	A7	A6	A5	A4	*	*	*	*		A[7:4] = P2, phase 2 period of 1-15 DCLK clocks,
											POR = 5DLKS = 5H
0	B2	1	0	1	1	0	0	1	0	Set Row Period	The next command sets the number of DCLKs, K, per row between 2-158DLKS, POR = 37DLKS = 25H
0	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0		

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12864Z

											The K value should be set as
											K = P1+P2+GS15 pulse width (POR: 3+5+29DLKS)
0	B3	1	0	1	1	0	0	1	1	Set Display Clock Divide Ratio/Oscillator Frequency	The lower nibble of the next command sets the divide ratio of the display clocks: Divide ratio = 1-16, POR = 2
0	A[3:0]	*	*	*	*	A3	A2	A1	A0		
0	A[7:4]	A7	A6	A5	A4	*	*	*	*		
											The higher nibble of the next command sets the Oscillator Frequency. Oscillator Frequency increases with the value of
											A[7:4] and vice versa. POR=0
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next eight bytes of command set the gray scale level of GS1-15 as below:
0	A[2:0]	*	*	*	*	*	A2	A1	A0		
0	B[2:0]	*	*	*	*	*	B2	B1	B0		A[2:0] = L1, POR=1
0	B[6:4]	*	B6	B5	B4	*	*	*	*		B[2:0] = L2, POR=1
0	C[2:0]	*	*	*	*	*	C2	C1	C0		B[6:4] = L3, POR=1
0	C[6:4]	*	C6	C5	C4	*	*	*	*		C[2:0] = L4, POR=1
0	D[2:0]	*	*	*	*	*	D2	D1	D0		C[6:4] = L5, POR=1
0	D[6:4]	*	D6	D5	D4	*	*	*	*		D[2:0] = L6, POR=1
0	E[2:0]	*	*	*	*	*	E2	E1	E0		D[6:4] = L7, POR=1
0	E[6:4]	*	E6	E5	E4	*	*	*	*		E[2:0] = L8,

Preliminary
Subject To Change Without Notice

12864Z

											POR=1
0	F[2:0]	*	*	*	*	*	F2	F1	F0		E[6:4] = L9, POR=1
0	F[6:4]	*	F6	F5	F4	*	*	*	*		F[2:0] = L10, POR=1
0	G[2:0]	*	*	*	*	*	G2	G1	G0		F[6:4] = L11, POR=1
0	G[6:4]	*	G6	G5	G4	*	*	*	*		G[2:0] = L12, POR=1
0	H[2:0]	*	*	*	*	*	H2	H1	H0		G[6:4] = L13, POR=1
0	H[6:4]	*	H6	H5	H4	*	*	*	*		H[2:0] = L14, POR=1
											H[6:4] = L15, POR=1
0	CF	1	1	0	0	1	1	1	1	Set Biasing Current for	F0H = High (POR)
0	A[7:6]	A7	A6	*	*	*	*	*	*	DC-DC converter	70H = Low
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

11 Graphic Display Data Ram Address Map

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. (Refer to Table 3-7 for GDDRAM address map description)

Table 4 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM78	4E	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM79	4F	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	

COM Outputs Row Address (HEX)
(Display Startline=0)

Table 5 – GDDRAM address map showing Horizontal Address Increment A[2]=1, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM0	00	D0[3:0]	D0[7:4]	D80[3:0]	D80[7:4]		D4960[3:0]	D4960[7:4]	D5040[3:0]	D5040[7:4]	
COM1	01	D1[3:0]	D1[7:4]	D81[3:0]	D81[7:4]		D4961[3:0]	D4961[7:4]	D5041[3:0]	D5041[7:4]	
COM78	4E	D78[3:0]	D78[7:4]	D158[3:0]	D158[7:4]		D5038[3:0]	D5038[7:4]	D5118[3:0]	D5118[7:4]	
COM79	4F	D79[3:0]	D79[7:4]	D159[3:0]	D159[7:4]		D5039[3:0]	D5039[7:4]	D5119[3:0]	D5119[7:4]	

COM Outputs Row Address (HEX)
(Display Startline=0)

Table 6 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=1, Nibble Re-map A[1]=1, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		3F		3E			01		00		
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]	
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]	
COM78	4E	D5055[7:4]	D5055[3:0]	D5054[7:4]	D5054[3:0]		D4993[7:4]	D4993[3:0]	D4992[7:4]	D4992[3:0]	
COM79	4F	D5119[7:4]	D5119[3:0]	D5118[7:4]	D5118[3:0]		D5057[7:4]	D5057[3:0]	D5056[7:4]	D5056[3:0]	

COM Outputs Row Address (HEX)
(Display Startline=0)

Table 7 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=1, and Display Start Line=16H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM15	0F	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM14	0E	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM17	11	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM16	10	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	

COM Outputs Row Address (HEX)
(Display Startline=10H)

Table 8 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, ... , D4834, D4835), Column Start Address=01H, Column End Address=3EH, Row Start Address=01H and Row End Address=4EH

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM0	00										
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]			
COM78	4E			D4774[3:0]	D4774[7:4]		D4835[3:0]	D4835[7:4]			
COM79	4F										

COM Outputs Row Address (HEX)
(Display Startline=0)

12 Precautions for operation and Storage

12.1 Precautions for Operation

- (1) Since OLED panel is made of glass, in order to prevent from glass broken, please do not apply any mechanical shock or impact or excessive force to it when installing the OLED module. Any strong mechanical impact due to falling dropping etc. may cause damage (breakage or cracking).
- (2) The polarizer on the OLED surface is made of soft material and is easily scratched. Please take most care when handing.
- (3) If OLED surface is contaminated, please wipe it off gently by using moisten soft cloth with normal ethanol, do not use acetone, ketone, isopropyl alcohol or water. If there is saliva or water on the OLED surface, please wipe it off immediately.
- (4) When handling OLED module, please be sure that the body and the tools are properly rounded. And do not touch I/O pins with bare hands or contaminate I/O pins, it will cause disconnection or defective insulation of terminals.
- (5) Do not attempt to disassemble or process the OLED module.
- (6) OLED module should be used under recommended operating conditions shown in the specification. Since the higher voltage leads to the shorter lifetime, be sure to use the specified operating voltage.
- (7) Foggy dew, moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage, the deteriorated display quality and electrochemical reaction then leads to the shorter life time and permanent damage to the module probably. Please pay attention to the environmental temperature and humidity.

12.2 Soldering

- (1) Use the high quality solder. (60-63% tin mixed with lead)
- (2) Iron: no higher than 260°C and less than 3~4 sec during soldering.
- (3) Soldering: only to the I/O terminals.
- (4) Rewiring: no more than 3 times.

12.3 Precautions for Storage

- (1) Please store OLED module in a dark place, avoid exposure to sunlight, the light of fluorescent lamp or any ultraviolet ray.
- (2) Keep the environment temperature at between 10°C and 35°C and the relative humidity less than 60%. Avoid high temperature, high humidity.
- (3) That keeps the OLED modules stored in the container shipped from supplier before using them is recommended.
- (4) Do not leave any article on the OLED module surface for an extended period of time.

12.4 Warranty period

VT Co.Ltd. warrants for a period of 12 months from the shipping date when stored or used under normal condition.

12.5 Test Status

TEST ITEM	TEST CONDITION	QUANTITY
High temperature (storage)	70°C,240 hours	3pcs
Humidity (storage)	+85°C, 100%RH, 24hours	3pcs
Low temperature (storage)	- 25°C,120 hours	3pcs
Low temperature (operating)	-25°C, 120 hours	2pcs
High temperature (operating)	70°C, 120hours	2pcs

Note: After test 2 hours (room temperature), check function & appearance.

