

# PIC12F635/PIC16F636/639

## 12.12 Power-Down Mode (Sleep)

The Power-down mode is entered by executing a `SLEEP` instruction.

If the Watchdog Timer is enabled:

- WDT will be cleared but keeps running.
- $\overline{PD}$  bit in the STATUS register is cleared.
- $\overline{TO}$  bit is set.
- Oscillator driver is turned off.
- I/O ports maintain the status they had before `SLEEP` was executed (driving high, low or high-impedance).

For lowest current consumption in this mode, all I/O pins should be either at  $V_{DD}$  or  $V_{SS}$ , with no external circuitry drawing current from the I/O pin and the comparators and  $CVREF$  should be disabled. I/O pins that are high-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The  $T0CKI$  input should also be at  $V_{DD}$  or  $V_{SS}$  for lowest current consumption. The contribution from on-chip pull-ups on PORTA should be considered.

The  $\overline{MCLR}$  pin must be at a logic high level.

**Note 1:** It should be noted that a Reset generated by a WDT time-out does not drive  $\overline{MCLR}$  pin low.

**2:** The Analog Front-End (AFE) section in the PIC16F639 device is independent of the microcontroller's power-down mode (Sleep). See **Section 11.32.2.3 "Sleep Command"** for AFE's Sleep mode.

### 12.12.1 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. External Reset input on  $\overline{MCLR}$  pin.
2. Watchdog Timer wake-up (if WDT was enabled).
3. Interrupt from RA2/INT pin, PORTA change or a peripheral interrupt.

The first event will cause a device Reset. The two latter events are considered a continuation of program execution. The  $\overline{TO}$  and  $\overline{PD}$  bits in the STATUS register can be used to determine the cause of device Reset. The  $\overline{PD}$  bit, which is set on power-up, is cleared when Sleep is invoked.  $\overline{TO}$  bit is cleared if WDT wake-up occurred.

The following peripheral interrupts can wake the device from Sleep:

1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2. Special event trigger (Timer1 in Asynchronous mode using an external clock).
3. EEPROM write operation completion.
4. Comparator output changes state.
5. Interrupt-on-change.
6. External Interrupt from INT pin.

Other peripherals cannot generate interrupts, since during Sleep, no on-chip clocks are present.

When the `SLEEP` instruction is being executed, the next instruction ( $PC + 1$ ) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the `SLEEP` instruction. If the GIE bit is set (enabled), the device executes the instruction after the `SLEEP` instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction following `SLEEP` is not desirable, the user should have a `NOP` after the `SLEEP` instruction.

**Note:** If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from Sleep. The `SLEEP` instruction is completely executed.

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

**Note:** If WUR is enabled ( $WURE = 0$  in Configuration Word), then the Wake-up Reset module will force a device Reset.

### 12.12.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a `SLEEP` instruction, the `SLEEP` instruction will complete as a `NOP`. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will not be cleared, the  $\overline{TO}$  bit will not be set and the  $\overline{PD}$  bit will not be cleared.
- If the interrupt occurs **during or after** the execution of a `SLEEP` instruction, the device will immediately wake-up from Sleep. The `SLEEP` instruction will be completely executed before the wake-up. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will be cleared, the  $\overline{TO}$  bit will be set and the  $\overline{PD}$  bit will be cleared.

Even if the flag bits were checked before executing a `SLEEP` instruction, it may be possible for flag bits to become set before the `SLEEP` instruction completes. To determine whether a `SLEEP` instruction executed, test the  $\overline{PD}$  bit. If the  $\overline{PD}$  bit is set, the `SLEEP` instruction was executed as a `NOP`.

To ensure that the WDT is cleared, a `CLRWDT` instruction should be executed before a `SLEEP` instruction.