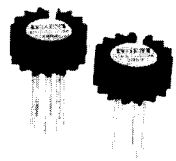
BURR-BROWN®



OPA101
OPA102

Low Noise - Wideband
PRECISION JFET INPUT OPERATIONAL AMPLIFIER

FEATURES

- GUARANTEED NOISE SPECTRAL DENSITY - 100% Tested
- LOW VOLTAGE NOISE - 8nV/$\sqrt{Hz}$ max at 10kHz
- LOW VOLTAGE DRIFT - 5μV/°C max (B grade)
- LOW OFFSET VOLTAGE - 250μV max (B grade)
- LOW BIAS CURRENTS - 10pA max at 25°C Ambient (B Grade)
- HIGH SPEED - 10V/μsec min (OPA102)
- GAIN BANDWIDTH PRODUCT - 40MHz (OPA102)

APPLICATIONS

- LOW NOISE SIGNAL CONDITIONING
- LIGHT MEASURMENTS
- RADIATION MEASUREMENTS
- PIN DIODE APPLICATIONS
- DENSITOMETERS
- PHOTODIODE/PHOTOMULTIPLIER CIRCUITS
- LOW NOISE DATA ACQUISITION

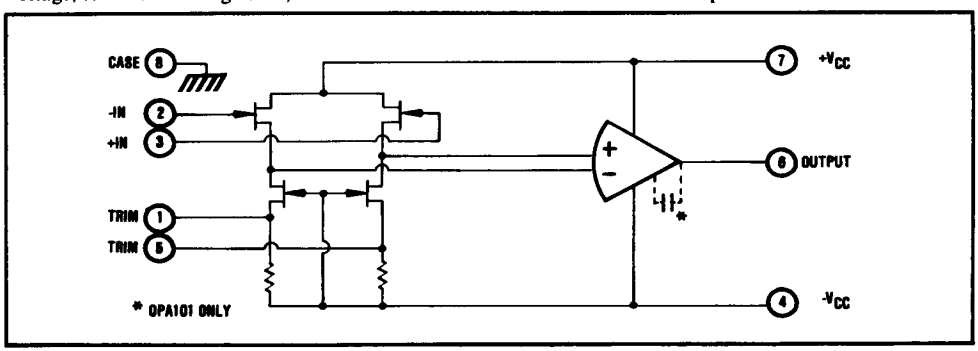
DESCRIPTION

The OPA101 and OPA102 are the first FET operational amplifiers available with noise characteristics (voltage spectral density) guaranteed and 100% tested.

The amplifiers have a complementary set of specifications permitting low errors in signal conditioning applications; low noise, low bias current, high open-loop gain, high common-mode rejection, low offset voltage, low offset voltage drift, etc.

In addition, the amplifiers have moderately high speed. The OPA101 is compensated for unity gain stability and has a slew rate of 5V/μsec, min. The OPA102 is compensated for gains of 3V/V and above and has a slew rate of 10V/μsec, min.

Each unit is laser-trimmed for low offset voltage and low offset voltage drift versus temperature. Bias currents are specified with the units fully warmed up at +25°C ambient temperature.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-434B

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL		OPA101/102AM			OPA101/102BM			
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT NOISE								
Voltage Noise Density	f_O = 1Hz(1)		100	200		80	100	nV/√Hz
	f_O = 10Hz		32	60		25	30	nV/√Hz
	f_O = 100Hz		14	30		11	15	nV/√Hz
	f_O = 1kHz		9	15		8	12	nV/√Hz
	f_O = 10kHz		7	8		7	8	nV/√Hz
	f_O = 100kHz		6.5	8		6.5	8	nV/√Hz
f_C: 1/f Corner Frequency			125			100		Hz
Voltage Noise	f_B = 0.1Hz to 10Hz(1)		1.3	2.6		1.0	1.3	µV, p-p
	f_B = 10Hz to 10kHz		1.0	1.2		0.8	1.0	µV, rms
	f_B = 10Hz to 100kHz		2.1	2.6		2.1	2.6	µV, rms
Current Noise Density	f_O = 0.1Hz thru 10kHz		2.0			1.4		fA/√Hz
Current Noise	f_B = 0.1Hz to 10Hz		38			26		fA, p-p
	f_B = 10Hz to 10kHz		200			140		fA, rms
DYNAMIC RESPONSE								
Bandwidth, Unity Gain	Small Signal							
OPA101			10			•		MHz
OPA102			Note 2			•		
Gain-Bandwidth Product	A_{CL} = 100							
OPA101			20			•		MHz
OPA102			40			•		MHz
Full Power Bandwidth	V_O = 20V, p-p; R_L = 1kΩ							
OPA101		80	100		•	•		kHz
OPA102		160	210		•	•		kHz
Slew Rate	V_O = ±10V; R_L = 1kΩ							
OPA101	A_{CL} = -1	5	6.5		•	•		V/µsec
OPA102	A_{CL} = -3	10	14		•	•		V/µsec
Settling Time (OPA101)	V_O = ±5V; A_{CL} = -1; R_L = 1kΩ							
ε = 1%			2			•		µsec
ε = 0.1%			2.5			•		µsec
ε = 0.01%			10			•		µsec
Settling Time (OPA102)	V_O = ±5V; A_{CL} = -3; R_L = 1kΩ							
ε = 1%			1			•		µsec
ε = 0.1%			1.5			•		µsec
ε = 0.01%			8			•		µsec
Small-Signal Overshoot	R_L = 1kΩ; C_L = 100pF							
OPA101	A_{CL} = +1		15			•		%
OPA102	A_{CL} = +3		20			•		%
Rise Time	10% to 90%, Small Signal							
OPA101			40			•		nsec
OPA102			30			•		nsec
Phase Margin	R_L = 1kΩ							
OPA101	A_{CL} = +1		60			•		Degrees
OPA102	A_{CL} = +3		45			•		Degrees
Overload Recovery(3)								
OPA101	A_{CL} = -1, 50% overdrive		1			•		µsec
OPA102	A_{CL} = -3, 50% overdrive		0.8			•		µsec
OPEN-LOOP GAIN, DC								
Full Load	V_O = ±10V; R_L = 1kΩ	94	105		•	•		dB
No Load	V_O = ±10V; R_L ≥ 10kΩ	96	108		•	•		dB
RATED OUTPUT								
Voltage	I_O = ±12mA	±12	±13		•	•		V
Current	V_O = ±12V	±12	±30		•	•		mA
Output Resistance	Open-Loop, f = DC		500			•		Ω
Short-Circuit Current			±45			•		mA
Capacitive Load Range	Phase Margin ≥ 25°							
OPA101	A_{CL} = +1		500			•		pF
OPA102	A_{CL} = +3		300			•		pF
INPUT OFFSET VOLTAGE								
Initial Offset	T_A = +25°C		±100	±500		±50	±250	µV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±6	±10		±3	±5	µV/°C
vs Supply Voltage	±5VDC ≤ | V_{CC} | ≤ ±20VDC		±10	±50		•	•	µV/V
vs Time			±10			•		µV/mo.
Adjustment Range	Circuit in "Connection Diagram"		±1			•		mV
INPUT BIAS CURRENT								
Initial Bias	T_A = +25°C		-12	-15		-6	-10	pA
vs Temperature			Note 4			•		
vs Supply Voltage			Note 5			•		

ELECTRICAL (CONT)

MODEL		OPA101/102AM			OPA101/102BM			
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT DIFFERENCE CURRENT								
Initial Difference	T_A = +25°C		±3	±6		±1.5	±4	pA
vs Temperature			Note 4			•		
vs Supply Voltage			Note 5			•		
INPUT IMPEDANCE								
Differential								
Resistance			10^{12}			•		Ω
Capacitance			1			•		pF
Common-mode								
Resistance			10^{13}			•		Ω
Capacitance			3			•		pF
INPUT VOLTAGE RANGE								
Common-mode Voltage Range	Linear Operation		±(| V_{CC} | -3)			•		V
Common-mode Rejection	f_O = DC, V_{CM} = ±10V	80	105		•	•		dB
POWER SUPPLY								
Rated Voltage			±15			•		VDC
Voltage Range	Derated Performance	±5		±20	•		•	VDC
Current, Quiescent			5.8	8		•	•	mA
TEMPERATURE RANGE								
Specification		-25		+85	•		•	°C
Operating	Derated Performance	-55		+125	•		•	°C
Storage		-65		+150	•		•	°C

NOTES: *Specifications same as for OPA101/102AM.
1. Parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.
2. Minimum stable gain for the OPA102 is 3V/V.
3. Time required for output to return from saturation to linear operation following the removal of an input overdrive signal.
4. Doubles approximately every 8.5°C.
5. See Typical Performance Curves.

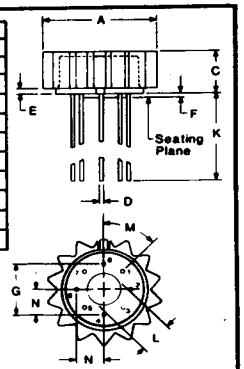
ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	750mW
Differential Input Voltage(2)	±20VDC
Input Voltage, Either Input(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-Circuit Duration(3)	60 seconds
Junction Temperature	+175°C

NOTES:
1. Package must be derated according to the details in the Application Information section.
2. For supply voltages less than ±20VDC, the absolute maximum input is equal to the supply voltage.
3. Short-circuit may be to ground only. See discussion of Thermal Model in the Application Information section.

MECHANICAL SPECIFICATIONS

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.489	.522	12.42	13.26
C	.243	.307	6.17	7.80
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67



NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

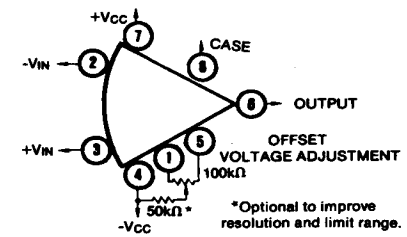
Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

Weight: 2 grams

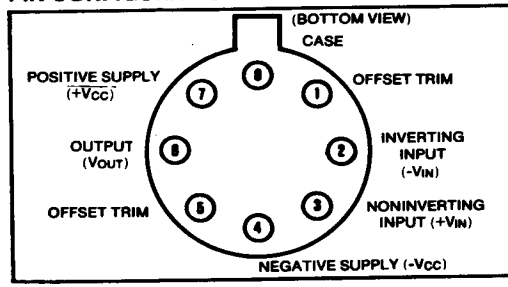
Order Number:
OPA101AM OPA101BM
OPA102AM OPA102BM

CONNECTION DIAGRAM



NOTE: Offset voltage adjustment affects voltage drift vs temperature by approximately ±0.3μV/°C for each 100μV of offset adjusted.

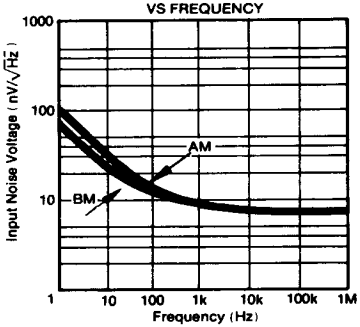
PIN CONFIGURATION



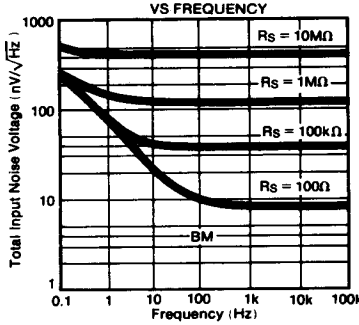
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = ±15VDC, unless otherwise noted. Performance curves apply to both OPA101 and OPA102 unless otherwise noted.)

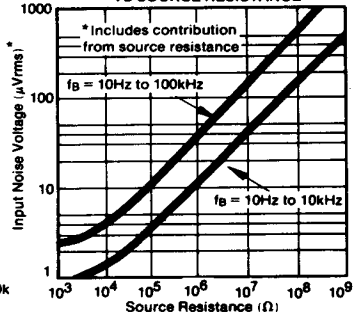
INPUT NOISE VOLTAGE VS FREQUENCY



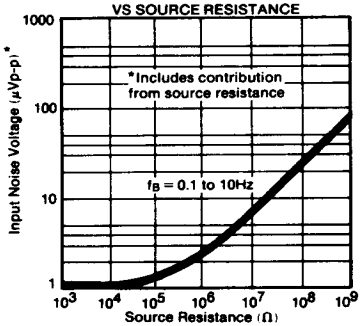
TOTAL INPUT NOISE VOLTAGE VS FREQUENCY



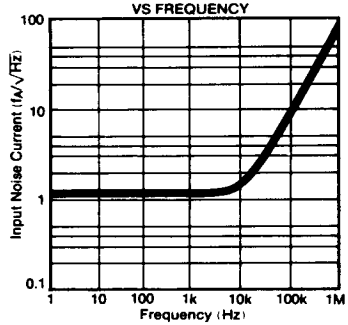
RMS INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



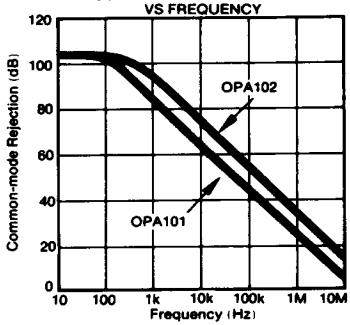
PEAK-TO-PEAK INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



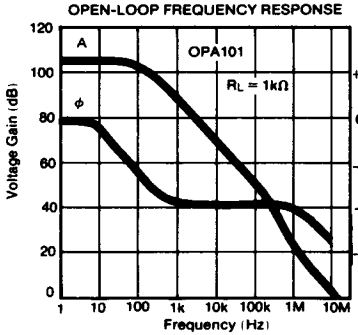
INPUT NOISE CURRENT VS FREQUENCY



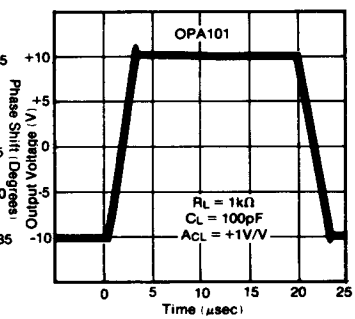
COMMON-MODE REJECTION VS FREQUENCY



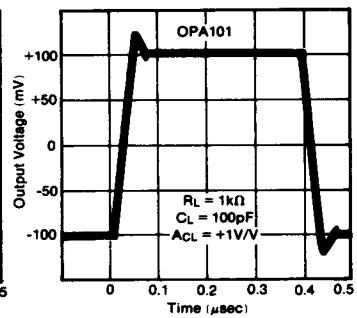
OPEN-LOOP FREQUENCY RESPONSE



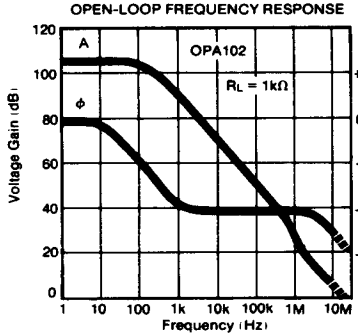
LARGE SIGNAL TRANSIENT RESPONSE



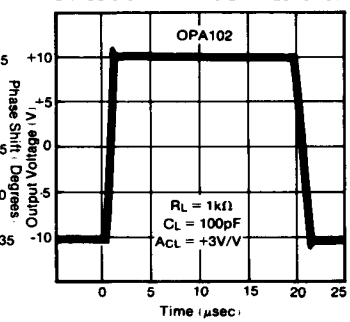
SMALL SIGNAL TRANSIENT RESPONSE



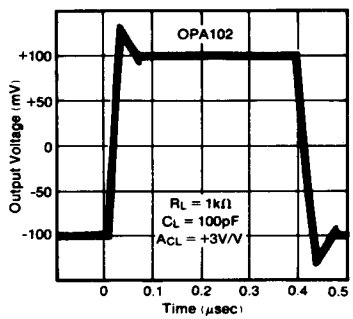
OPEN-LOOP FREQUENCY RESPONSE



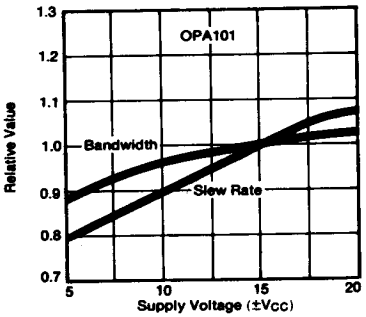
LARGE SIGNAL TRANSIENT RESPONSE



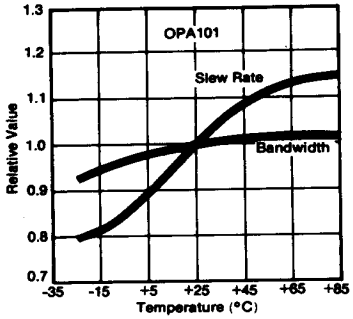
SMALL SIGNAL TRANSIENT RESPONSE



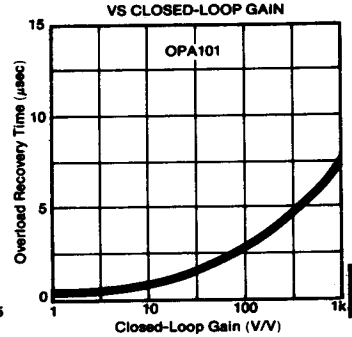
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



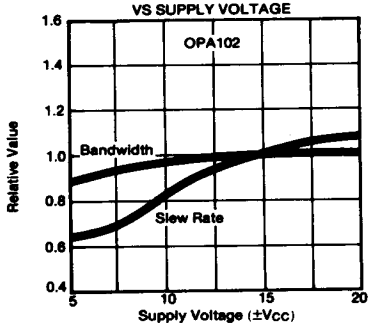
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



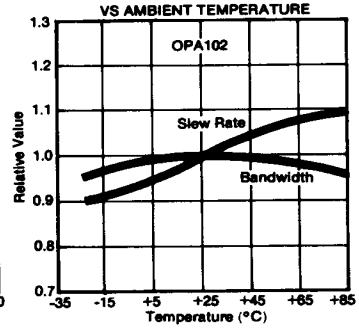
OVERLOAD RECOVERY TIME VS CLOSED-LOOP GAIN



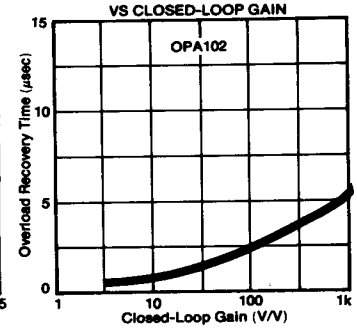
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



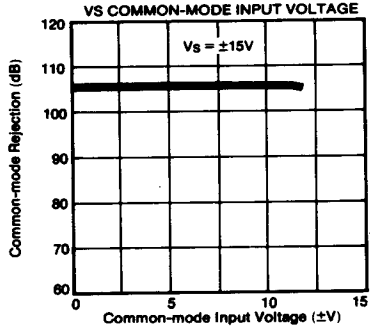
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



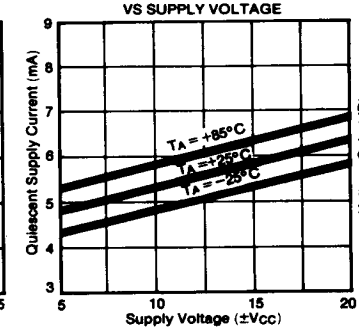
OVERLOAD RECOVERY TIME VS CLOSED-LOOP GAIN



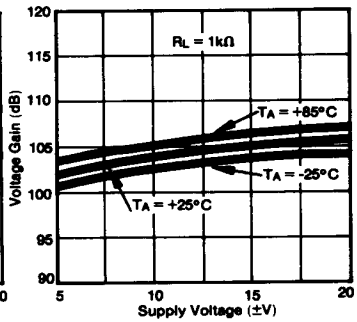
COMMON-MODE REJECTION VS COMMON-MODE INPUT VOLTAGE



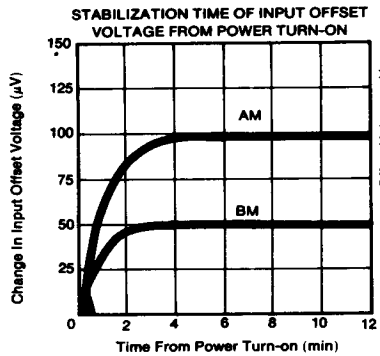
QUIESCENT SUPPLY CURRENT VS SUPPLY VOLTAGE



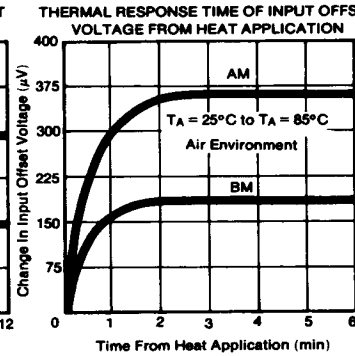
VOLTAGE GAIN VS SUPPLY VOLTAGE



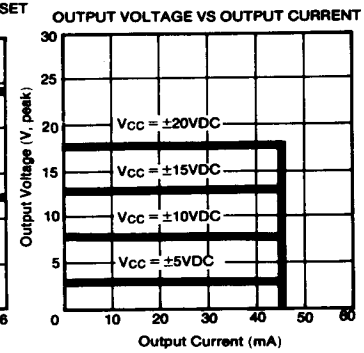
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



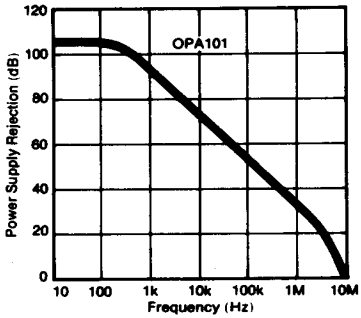
THERMAL RESPONSE TIME OF INPUT OFFSET VOLTAGE FROM HEAT APPLICATION



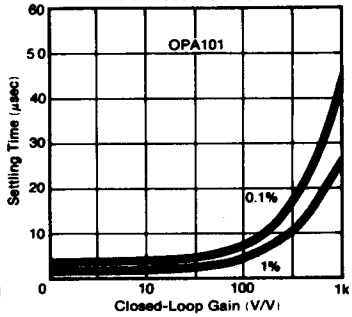
OUTPUT VOLTAGE VS OUTPUT CURRENT



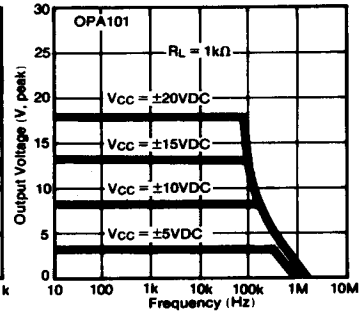
POWER SUPPLY REJECTION VS FREQUENCY



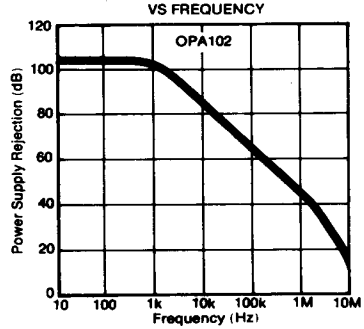
SETTLING TIME VS CLOSED-LOOP GAIN



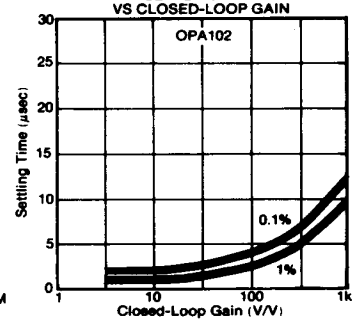
OUTPUT VOLTAGE VS FREQUENCY



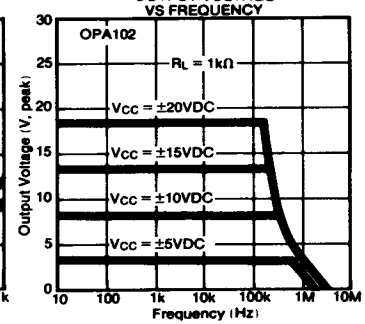
POWER SUPPLY REJECTION VS FREQUENCY



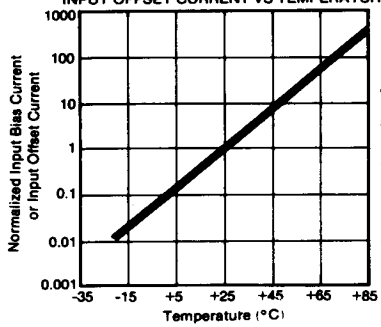
SETTLING TIME VS CLOSED-LOOP GAIN



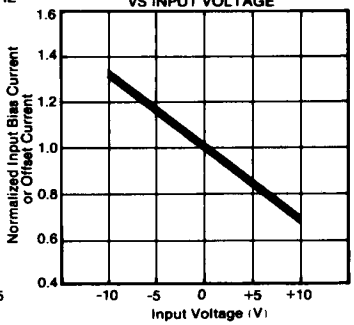
OUTPUT VOLTAGE VS FREQUENCY



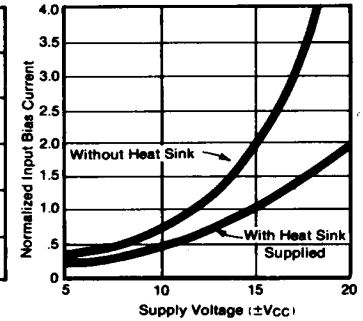
INPUT BIAS CURRENT VS TEMPERATURE AND INPUT OFFSET CURRENT VS TEMPERATURE



INPUT BIAS CURRENT VS INPUT VOLTAGE AND INPUT OFFSET CURRENT VS INPUT VOLTAGE



INPUT BIAS CURRENT VS SUPPLY VOLTAGE



APPLICATION INFORMATION

INTRODUCTION

The availability of detailed noise spectral density characteristics for the OPA101/102 amplifiers allows an accurate noise error analysis in a variety of different circuit configurations. The fact that the spectral characteristics are guaranteed maximums allows absolute noise errors to be truly bounded. Other FET amplifiers normally use simpler specifications of rms noise in a given bandwidth (typically 10Hz to 10kHz) and peak-to-peak noise (typically specified in the band 0.1Hz to 10Hz). These specifications do not contain enough information to allow accurate analysis of noise behavior in any but the simplest of circuit configurations.

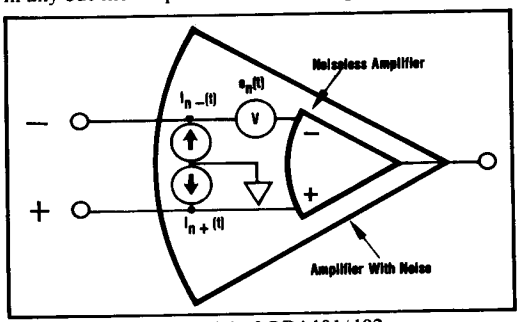


FIGURE 1. Noise Model of OPA101/102.

Noise in the OPA101/102 can be modeled as shown in Figure 1. This model is the same form as the DC model for offset voltage (E_{OS}) and bias currents (I_B). In fact, if the voltage $e_n(t)$ and currents $i_n(t)$ are thought of as general instantaneous error sources, then they could represent either noise or DC offsets. The error equations for the general instantaneous model are shown in Figure 2 below.

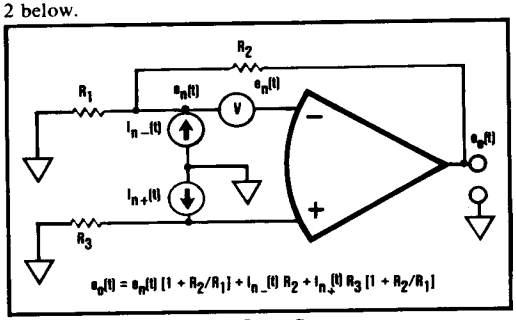


FIGURE 2. Circuit With Error Sources.

If the instantaneous terms represent DC errors (i.e., offset voltage and bias currents) the equation is a useful tool to compute actual errors. It is not, however, useful in the same direct way to compute noise errors. The basic problem is that noise cannot be predicted as a function of time. It is a random variable and must be described in probabilistic terms. It is normally described by some type of average - most commonly the rms value.

$$N_{rms} \triangleq \sqrt{1/T \int_0^T n^2(t)\, dt} \qquad (1)$$

where N_{rms} is the rms value of some random variable n(t). In the case of amplifier noise, n(t) represents either $e_n(t)$ or $i_n(t)$.

The internal noise sources in operational amplifiers are normally uncorrelated. That is, they are randomly related to each other in time and there is no systematic phase relationship. Uncorrelated noise quantities are combined as root-sum-squares. Thus, if $n_1(t)$, $n_2(t)$, and $n_3(t)$ are uncorrelated then their combined value is

$$N_{TOTAL_{rms}} = \sqrt{N_1^2{}_{rms} + N_2^2{}_{rms} + N_3^2{}_{rms}} \qquad (2)$$

The basic approach in noise error calculations then is to identify the noise sources, segment them into conveniently handled groups (in terms of the shape of their noise spectral densities), compute the rms value of each group, and then combine them by root-sum-squares to get the total noise.

TYPICAL APPLICATION

The circuit in Figure 3 is a common application of a low noise FET amplifier. It will be used to demonstrate the above noise calculation method.

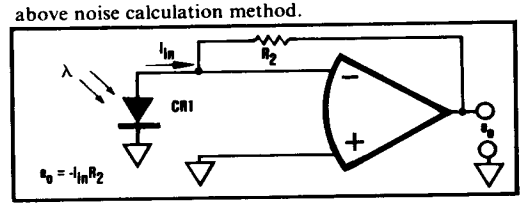


FIGURE 3. Pin Photo Diode Application.

CR1 is a PIN photo diode connected in the photovoltaic mode (no bias voltage) which produces an output current i_{in} when exposed to the light, λ.

A more complete circuit is shown in Figure 4. The values shown for C_1 and R_1 are typical for small geometry PIN diodes with sensitivities in the range of 0.5 A/W. The value of C_2 is what would be expected from stray capacitance with moderately careful layout (0.5pF to 2pF). A larger value of C_2 would normally be used to limit the bandwidth and reduce the voltage noise at higher frequencies.

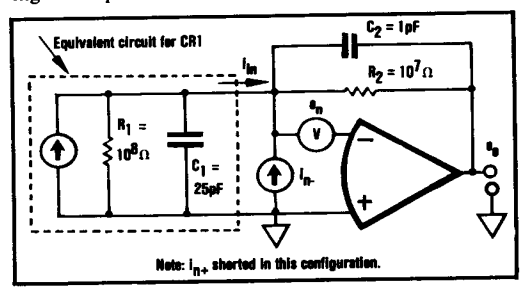


FIGURE 4. Noise Model of Photo Diode Application.

In Figure 4, e_n and i_n represent the amplifier's voltage and current spectral densities, $e_n(\omega)$ and $i_n(\omega)$ respectively. These are shown in Figure 5.

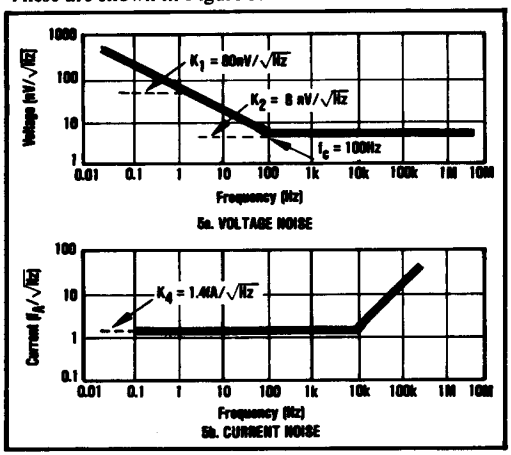


FIGURE 5. Noise Voltage and Current Spectral Density.

Figure 6 shows the desired "gain" of the circuit (transimpedance of $e_o/i_{in} = Z_2(s)$). It has a single-pole rolloff at $f_2 = 1/(2\pi R_2 C_2) = \omega_2/2\pi$. Output noise is minimized if f_2 is made smaller. Normally R_2 is chosen for the desired DC transimpedance based on the full scale input current (i_{in} full scale) and maximum output (e_o max). Then C_2 is chosen to make f_2 as small as possible consistent with the necessary signal frequency response.

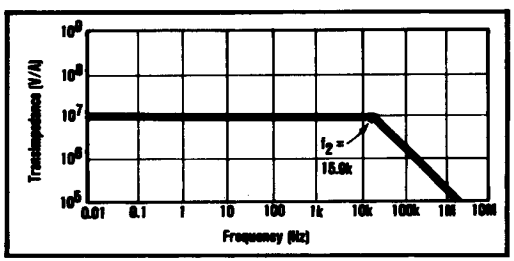


FIGURE 6. Transimpedance.

Voltage Noise

Figure 7 shows the noise voltage gain for the circuit in Figure 4. It is derived from the equation

$$e_o = e_n \left[\frac{A}{1 + A\beta} \right] = e_n \frac{1}{\beta} \left[\frac{1}{1 + \frac{1}{A\beta}} \right] \quad (3)$$

where:

A = $A(\omega)$ is the open-loop gain

β = $\beta(\omega)$ is the feedback factor. It is the amount of output voltage feedback to the input of the op amp.

$A\beta$ = $A(\omega)\,\beta(\omega)$ is the loop gain. It is the amount of the output voltage feedback to the input and then amplified and returned to the output.

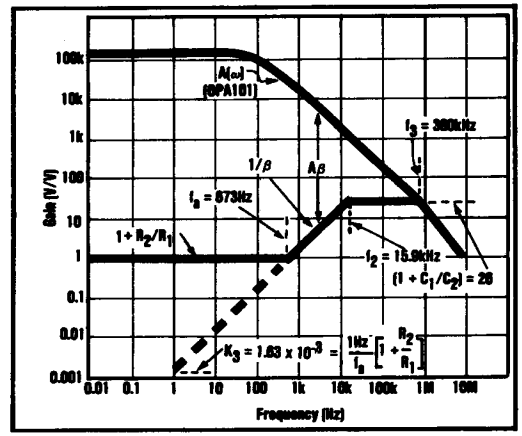


FIGURE 7. Noise Voltage Gain.

Note that for large loop gain ($A\beta >> 1$)

$$e_o \approx e_n \frac{1}{\beta} . \quad (4)$$

For the circuit in Figure 4 it can be shown that

$$\frac{1}{\beta} = 1 + \frac{R_2(R_1C_1s + 1)}{R_1(R_2C_2s + 1)} . \quad (5)$$

This may be rearranged to

$$\frac{1}{\beta} = \frac{R_2 + R_1}{R_1} \left[\frac{\tau_a s + 1}{\tau_2 s + 1} \right] \quad (5a)$$

where $\tau_a = (R_1 \parallel R_2)(C_1 \parallel C_2)$ (5b)

$$= \left[\frac{R_1R_2}{R_1 + R_2} \right] (C_1 + C_2)$$

and $\tau_2 = R_2C_2$. (5c)

Then, $f_a = \frac{1}{2\pi\tau_a}$ and $f_2 = \frac{1}{2\pi\tau_2}$. (5d)

For very low frequencies ($f << f_a$), s approaches zero and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{R_2}{R_1} . \quad (6)$$

For very high frequencies ($f >> f_2$), s approaches infinity and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{C_1}{C_2} . \quad (7)$$

The noise voltage spectral density at the output is obtained by multiplying the amplifier's noise voltage spectral density (Figure 5a) times the circuits noise gain (Figure 7). Since both curves are plotted on log-log scales the multiplication can be performed by the addition of the two curves. The result is shown in Figure 8.

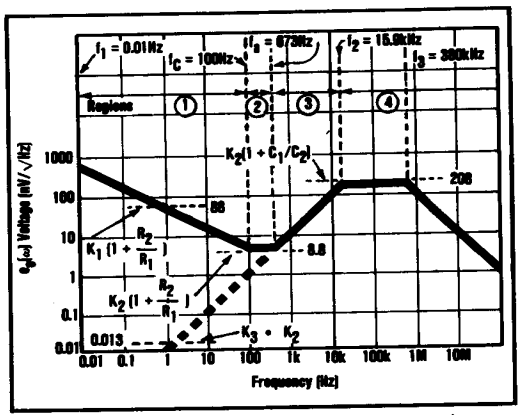


FIGURE 8. Output Noise Voltage Spectral Density.

The total rms noise at the amplifier's output due to the amplifier's internal voltage noise is derived from the $e_o(\omega)$ function in Figure 8 with the following expression:

$$E_{o\ rms} = \sqrt{\int_{-\infty}^{+\infty} e_o^2(\omega)\, d\omega} \qquad (8)$$

It is both convenient and informative to calculate the rms noise using a piecewise approach (region-by-region) for each of the four regions indicated in Figure 8.

Region 1; $f_l = 0.01$Hz to $f_c = 100$Hz

$$E_{n1\ rms} = K_1 \left(1 + \frac{R_2}{R_1}\right) \sqrt{\ln(f_c/f_l)} \qquad (9)$$

$$= 80\text{nV}/\sqrt{\text{Hz}} \left(1 + \frac{10^7}{10^8}\right) \sqrt{\ln \frac{100}{0.01}} \qquad (9a)$$

$$= 0.267\mu\text{V}$$

This region has the characteristic of 1/f or "pink" noise (slope of -10dB per decade on the log-log plot of $e_n(\omega)$). The selection of 0.01Hz is somewhat arbitrary but it can be shown that for this example there would be only negligible additional contribution by extending f_l several decades lower. Note that $K_1(1 + R_2/R_1)$ is the value of e_o at f = 1Hz.

Region 2; $f_c = 100$Hz to $f_a = 673$Hz

$$E_{n2\ rms} = K_2 \left(1 + \frac{R_2}{R_1}\right) \sqrt{f_a - f_c} \qquad (10)$$

$$= 8\text{nV}/\sqrt{\text{Hz}} \left(1 + \frac{10^7}{10^8}\right) \sqrt{673 - 100} \qquad (10a)$$

$$= 0.21\mu\text{V}$$

This is a region of "white" noise which leads to the form of equation (10).

Region 3; $f_a = 673$Hz to $f_2 = 15.9$kHz

$$E_{n3\ rms} = K_2 \cdot K_3 \sqrt{\frac{f_2^3}{3} - \frac{f_a^3}{3}} \qquad (11)$$

$$= 8\text{nV}/\sqrt{\text{Hz}}\,(1.63 \times 10^{-3}) \sqrt{\frac{(15.9\text{k})^3}{3} - \frac{(673)^3}{3}} \qquad (11a)$$

$$= 15.1\mu\text{V}$$

This is the region of increasing noise gain (slope of +20dB/decade on the log-log plot) caused by the lead network formed by the resistance $R_1 \| R_2$ and the capacitance $(C_1 + C_2)$. Note that $K_3 \cdot K_2$ is the value of the $e_o(\omega)$ function for this segment projected back to 1Hz.

Region 4; f > 15.9kHz

$$E_{n4\ rms} = K_2 \left(1 + \frac{C_1}{C_2}\right) \sqrt{\left[\frac{\pi}{2}\right] f_3 - f_2} \qquad (12)$$

$$= 8\text{nV}/\sqrt{\text{Hz}} \left(1 + \frac{25}{1}\right) \sqrt{\left[\frac{\pi}{2}\right] 380\text{k} - 15.9\text{k}} \qquad (12a)$$

$$= 158.5\mu\text{V}$$

This is a region of white noise with a single order rolloff at $f_3 = 380$kHz caused by the intersection of the $1/\beta$ curve and the open-loop gain curve. The value of 380kHz is obtained from observing the intersection point of Figure 7. The $\pi/2$ applied to f_3 is to convert from a 3dB corner frequency to an effective noise bandwidth.

Current Noise

The output voltage component due to current noise is equal to:

$$E_{ni} = i_n \times Z_2(s) \qquad (13)$$

where $Z_2(s) = R_2 \| X_{C_2}$ (13a)

This voltage may be obtained by combining the information from figures 5 (b) and 6 together with the open loop gain curve of Figure 7. The result is shown in Figure 9 below.

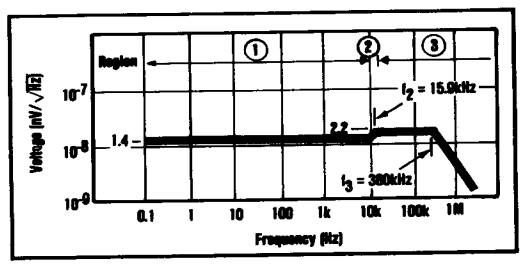


FIGURE 9. Output Voltage Due to Noise Current.

Using the same techniques that were used for the voltage noise:

Region 1; 0.1Hz to 10kHz

$$E_{ni1} = 1.4 \times 10^{-8} \sqrt{10k - 0.1} \quad (14)$$

$$= 1.4\mu V$$

Region 2; 10kHz to 15.9kHz

$$E_{ni2} = 1.4 \times 10^{-12} \sqrt{\frac{(15.9k)^3}{3} - \frac{(10k)^3}{3}} \quad (14a)$$

$$= 1.4\mu V$$

Region 3; f > 15.9kHz

$$E_{ni3} = 2.2 \times 10^{-8} \sqrt{\frac{\pi}{2} 380k - 15.9k} \quad (14b)$$

$$= 16.8\mu V$$

$$E_{ni\ total} = 10^{-6} \sqrt{(1.4)^2 + (1.4)^2 + (16.8)^2} \quad (14c)$$

$$= 16.9\mu V_{rms}$$

Resistor Noise

For a complete noise analysis of the circuit in Figure 4, the noise of the feedback resistor, R_2, must also be included. The thermal noise of the resistor is given by:

$$E_{R\ rms} = \sqrt{4kTRB} \quad (15)$$

K = Boltzmann's constant = 1.38×10^{-23} Joules/°Kelvin
T = Absolute temperature (degrees Kelvin)
R = Resistance (ohms)
B = Effective noise bandwidth (Hz) (ideal filter assumed)

At 25°C this becomes

E_R rms $\approx 0.13 \sqrt{RB}$
E_R rms in μV
R in MΩ
B in Hz

For the circuit in Figure 4

$R_2 = 10^7\Omega = 10M\Omega$

$$B = \frac{\pi}{2}(f_2) = \frac{\pi}{2} 15.9k$$

Then

$$E_R\ rms = (411nV/\sqrt{Hz}) \sqrt{B}$$

$$= (411nV/\sqrt{Hz}) \sqrt{\frac{\pi}{2} 15.9kHz}$$

$$= 64.9\mu V\ rms$$

Total Noise

The total noise may now be computed from

$$E_{n\ total} = \sqrt{E_{n1}^2 + E_{n2}^2 + E_{n3}^2 + E_{n4}^2 + E_{nR}^2 + E_{ni}^2} \quad (16)$$

$$= \sqrt{0.267^2 + 0.21^2 + 15.1^2 + 158.5^2 + 64.9^2 + 16.9^2} \quad (16a)$$

$$= \sqrt{0.07 + 0.04 + 228 + 25122 + 4212 + 286} \quad (16b)$$

$$= 173\mu V\ rms$$

Conclusions

Examination of the results in equation (16b) together with the curves in Figure 8 leads to some interesting conclusions. In this example 84% of the noise comes from E_{n4}. From Figure 8 it is seen that this is the area beyond the pole formed by R_2 and C_2.

The E_{n4} contribution could be reduced several ways. The most common method is to increase C_2. This reduces f_2 and the value of K2(1 + C1/C2) (see Figure 8). It also reduces the signal bandwidth (see Figure 6) and the final value of C_2 is normally a compromise between noise gain and necessary signal bandwidth.

It should be noted that increasing C_2 will also affect f_a since f_a is determined by $(C_1 + C_2)$ (see equation (5b)). Normally C_2 is larger than C_1 and f_2 will change more than for a given change in C_2.

The other means of reducing the noise in region 4 involves changing amplifier parameters. For example, the use of a slower amplifier would move the open-loop gain curve to the left and decrease f_3. Of course, reducing the value of K_2, the noise floor, would also reduce the noise in this region.

The second largest component is the resistor noise E_{nR} (14% of the total noise). A lower resistor value decreases resistor noise as a function of $\sqrt{R}$, but it also lowers the desired signal gain as a direct function of R. Thus, lowering R reduces the signal-to-noise ratio at the output which shows that the feedback resistor should be as large as possible. The noise contribution due to R_2 can be decreased by raising the value of C_2 (lowering f_2) but this reduces signal bandwidth.

It is interesting to note that the current noise of the amplifier accounted for only 1% of the total E_n. This is different than would be expected when comparing the current and voltage spectral densities with the size of the feedback resistor. For example, if we define a characteristic value of resistance as

$$R_{characteristic} = \frac{e_n(\omega)}{i_n(\omega)} \text{ at } f = 10kHz \quad (17)$$

$$= \frac{8nV/\sqrt{Hz}}{1.4fA/\sqrt{Hz}}$$

$$= 5.7M\Omega$$

Thus, in simple transimpedance circuits with feedback resistors greater than the characteristic value, the amplifier's current noise would cause more output noise than the amplifier's voltage noise. Based on this and the 10MΩ feedback resistor in the example, the amplifier noise current would be expected to have a higher contribution than the noise voltage. The reason it does not in the example of Figure 4 is that the noise voltage has high gain at higher frequencies (Figure 7) and the noise current does not (Figure 6).

The fourth largest component of total noise comes from E_{n3} (0.8%). Decreasing C_1 will also lower the term $K_2(1 + C_1/C_2)$. In this case, f_2 will stay fixed and f_a will move to the right (i.e., the +20dB/decade slope segment will move

to the right). This can have a significant reduction on noise without lowering the signal bandwidth. This points out the importance of maintaining low capacitance at the amplifier's input in low noise applications.

Shielding and Guarding

The low noise, low bias current and high input impedance of the OPA101/102 are well suited to a number of precision applications. In order to fully benefit from the outstanding specifications of this unit, careful layout, shielding, and guarding are required. Careless signal wiring or printed circuit board layout can easily degrade circuit performance several orders of magnitude below the capability of the OPA101/102.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. The metal case of the OPA101/102 is connected to pin 8 and is not connected to any internal amplifier circuitry. Thus it is possible to use the case as a shield to reduce noise pickup.

Unless care is used, leakage currents across printed circuit boards can easily exceed the bias current of the OPA101/102. To avoid leakage problems, it is recommended that a Teflon IC socket be used or that at least the signal input lead of the amplifier be wired to a Teflon standoff. If this is not done and instead the OPA101/102 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 10). The amplifier case, pin 8, should also be connected to the guard. This insures that the entire amplifier circuitry is fully surrounded by the guard potential. This minimizes the voltage placed across any leakage paths and thus reduces leakage currents. In addition, noise pickup is also reduced.

Figures 11, 12, and 13 show typical applications using the guard and case shielding.

Cleanliness is also a prime concern in low bias current circuits. It is recommended that after installation is complete the assembly be washed with a low residue solvent such as TMC Freon followed by rinsing with deionized water. The use of some form of high dielectric conformal coating such as a good two-part urathane should be considered if the assembly will be used in air environment which could deposit contaminants on the low current circuitry.

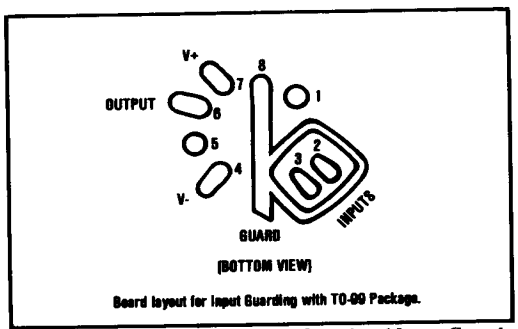


FIGURE 10. Connection of Case Guard and Input Guard.

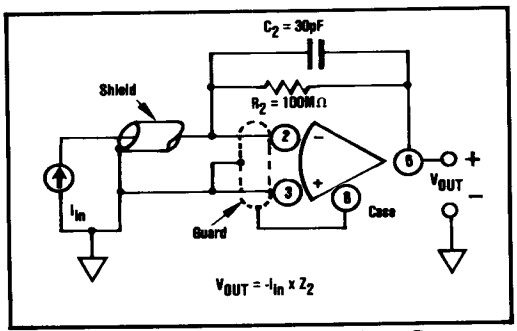


FIGURE 11. Ultra-Low Current to Voltage Converter.

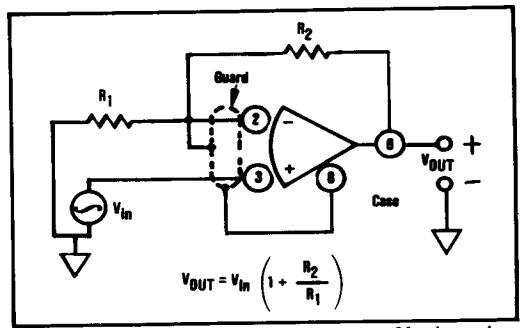


FIGURE 12. Ultra-High Input Impedance Noninverting Circuit.

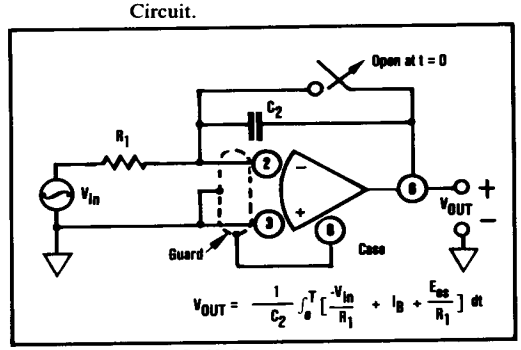


FIGURE 13. Low Drift Integrator.

Thermal Model

Figure 14 is the thermal model for the OPA101/102 where:

T_J = Junction temperature (output load)
T_J* = Junction temperature (no load)
T_C = Case temperature
T_A = Ambient temperature
θ_{CA} = Thermal resistance, case-to-ambient

θ_{HS} = Effective thermal resistance of the heat sink
P_{DQ} = Quiescent power dissipation
$|+V_{CC}|\ I_{+QUIESCENT} + |-V_{CC}|\ I_{-QUIESCENT}$
P_{DX} = Power dissipation in the output transistor
$= (V_{OUT} - V_{CC})\ I_{OUT}$

(In a complementary output stage only one output transistor is conducting current at a time.)

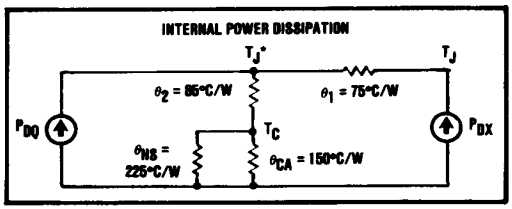


FIGURE 14. OPA101/102 Thermal Model

This model is obviously not the simple one-power source model used with most linear integrated circuits. It is, however, a more accurate model for multichip hybrid integrated circuits where the quiescent power is dissipated in the input stage and the internal power dissipation due to the load is dissipated in a somewhat physically separated output stage.

The model in Figure 14 must be used in conjunction with the OPA101/102's absolute maximum ratings of internal power dissipation and junction temperature to determine the derated power dissipation capability of the package.

As an example of how to use this model, consider this problem: Determine the output transistor junction temperature when the output has its maximum load resistance and is operated at the worst-case output voltage conditions. Assume $V_{CC} = \pm 15$VDC and $T_A = 25°C$.

Maximum P_{DX} occurs where $V_{OUT} = 1/2V_{CC}$. Then

$$P_{DX\ max} = \frac{(V_{CC})^2}{4R_{load}} \qquad (18)$$

$$T_j = T_A + P_{DQ}[\theta_2 + (\theta_{HS} \parallel \theta_{CA})] + P_{DX}[\theta_1 + \theta_2 + (\theta_{HS} \parallel \theta_{CA})] \qquad (19)$$

where $(\theta_{HS} \parallel \theta_{CA}) = \dfrac{\theta_{HS}\theta_{CA}}{\theta_{HS} + \theta_{CA}} = 90°C/W$

Substituting appropriate values yields

$$T_j = 25° + (30V \times 8mA)[85°C/W + 90°C/W] + \frac{(15V)^2}{4 \times 1k\Omega}[75°C/W + 85°C/W + 90°C/W]$$

$$= 25°C + 42°C + 14°C = T_A + 56°C$$

$$= 81°C$$

The conclusion is that under a worst-case output voltage condition and with a 1kΩ load the junction temperature rise is 56°C above ambient. Thus, under these conditions, the device could be operated in an ambient up to 119°C without exceeding the 175°C junction temperature rating.

A similar analysis for conditions of the output short-circuited to ground where

$$P_{DX\ ss} = V_{CC}\ I_{(output\ limit)} \qquad (20)$$

shows that the maximum junction temperature rating of 175°C is exceeded. Thus, the output should not be shorted to ground for sustained periods of time.

HEAT SINK

The heat sink used on the OPA101/102 should not be removed. It has the effect of reducing the package thermal resistance from 150°C/W to about 90°C per watt. Removing the heat sink would naturally increase the junction temperature of the amplifier which would in turn raise the input bias current. The change in thermal resistance also affects the noise performance. Removing the heat sink would increase the noise in the 1/f region.