STM32 Seminar
STM32F Connectivity-Line

COMPEL/STM Seminar

November 2010

Seminar Agenda

- Overview of ST Microcontroller Portfolio
- Introduction to Cortex-M Core
- STM32 General Purpose Lines
  - Product-Line Overview (F100/F101/F103)
  - Walk through the main peripherals
  - ST Standard Peripheral Library
  - Live demonstration of the STM32 Value Discovery Kit
- STM32 Low-Power Line
  - Product-Line Overview (L15x)
  - Low-Power modes and consumption
  - Specific Peripherals
- STM32 Connectivity Line
  - Product-Line Overview (F105/7 & next)
  - Ethernet & USB Host Peripherals
  - Stacks & Tools
  - Audio Support
- STM32 Wireless
  - Product-Line Overview (W108)
  - RF Performances
  - Wireless Stacks (Zigbee, RF4CE, proprietary)
- STM32 Tools
  - Third Party Compiler & IDE
  - Boards and Debuger
  - ST Libraries

STM32F10x Product Lines

All lines include:

- Multiple communication peripherals Up to 5 x USART, 3xSPI, 2xI²C
- ETM*
- FSMC**
- Dual 12-bit DAC***
- Multiple 16-bit Timers
- Main Osc 4-16MHz (25MHz on 105/107)
- Internal 8 MHz RC and 40 kHz RC
- Real Time Clock with Battery domain & 32KHz ext osc
- 2 x Watchdogs
- Reset circuitry and Brown Out Warning
- Up to 12 DMA cnls

+

Connectivity Line: STM32F107

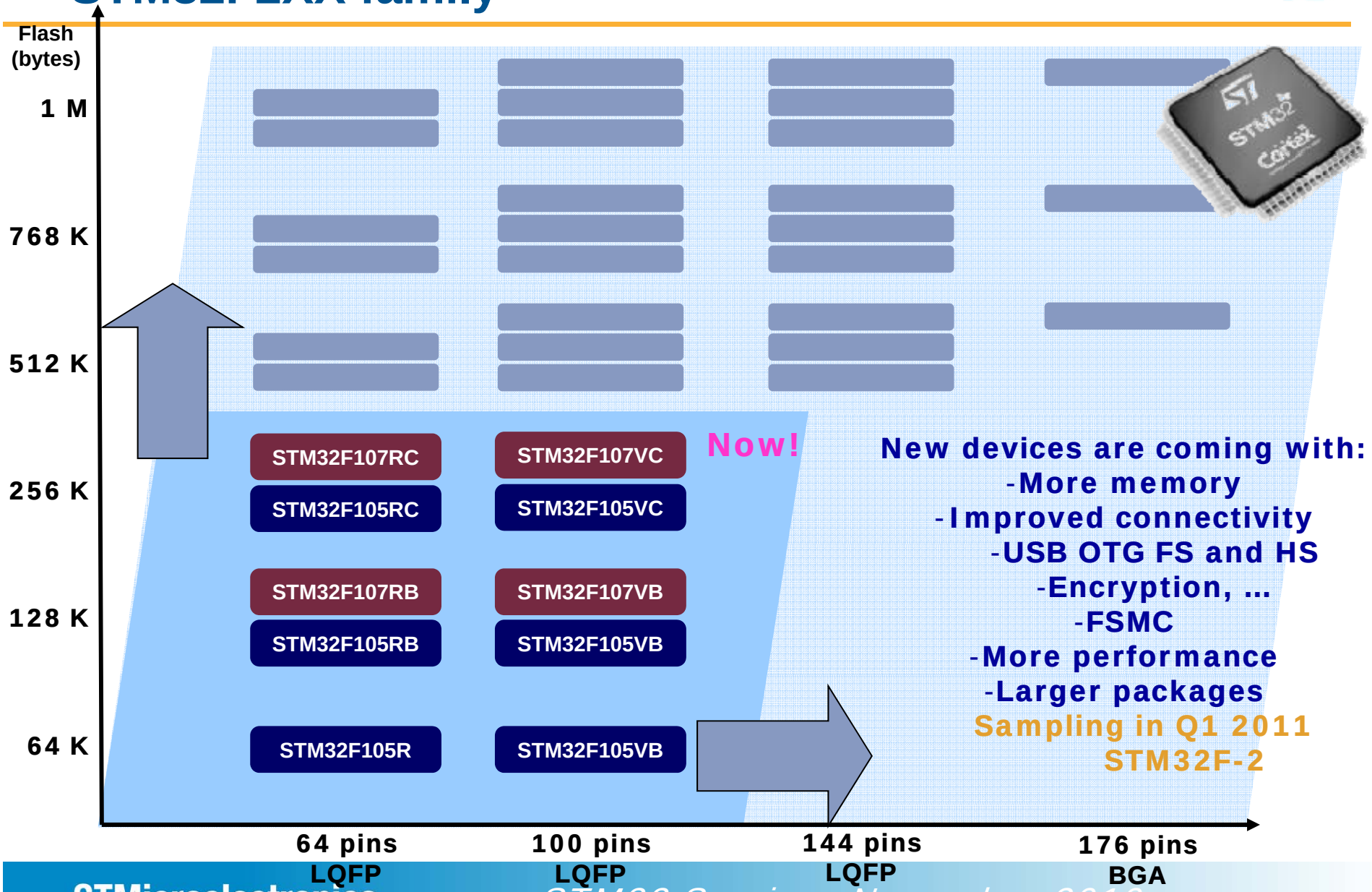
Connectivity Line: STM32F105

* Performance/Access Lines 256KB, 384KB, or 512KB devices and ALL Connectivity devices

** 256KB, 384KB, or 512KB Performance and Access devices

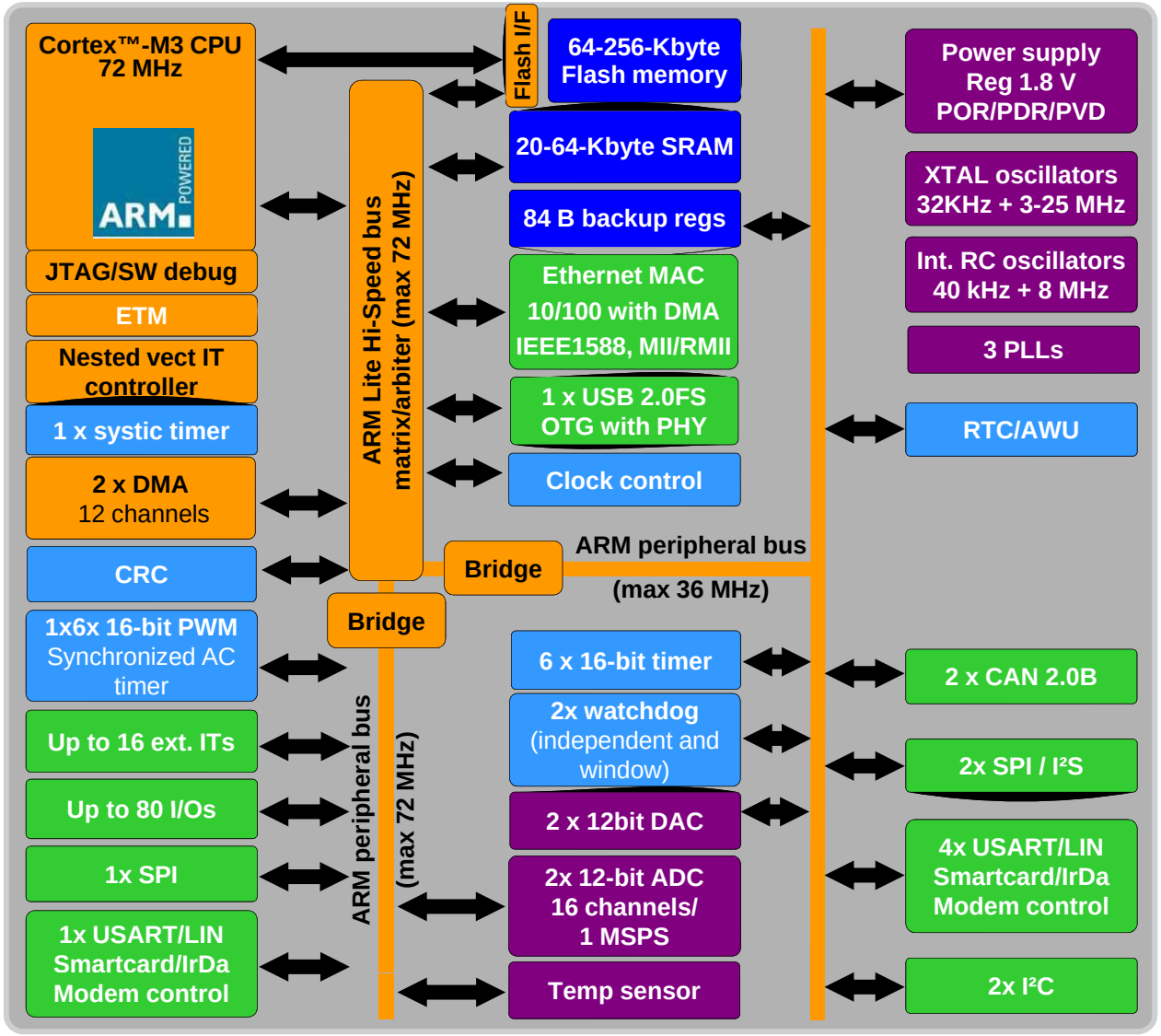
*** 256KB, 384KB, or 512KB devices except Value line where present on all memory range

The STM32 Connectivity line is growing with STM32F2XX family



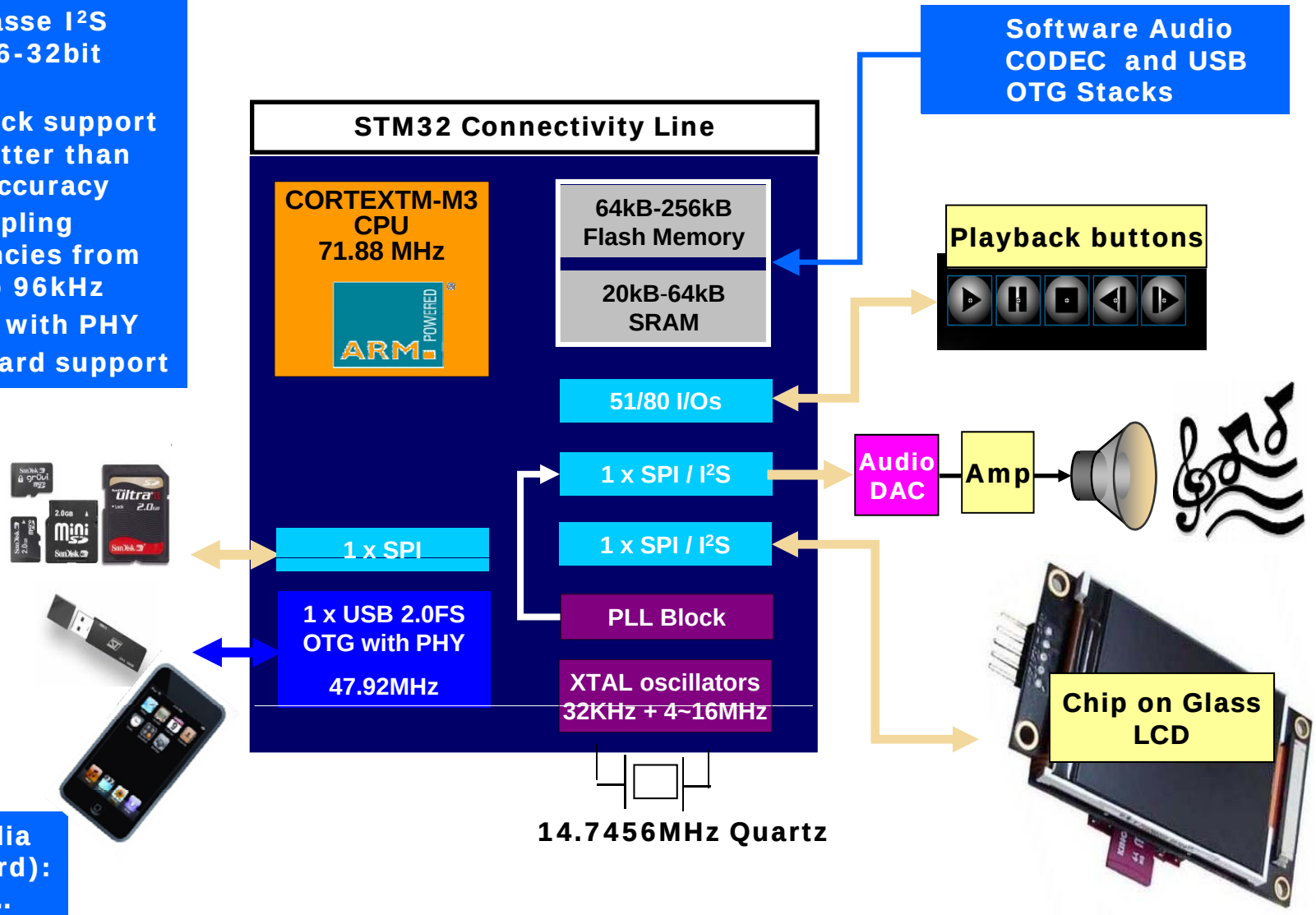
STM32F105/7 internal architecture

- Advanced clock tree
  - 8KHz-96KHz with less than 0.5% error on I2S clock
  - HQ Audio + USB
  - USB + Ethernet
- USB OTG
  - Support OTG or Device mode
- Ethernet
  - With IEEE1588 Real Time Stamping
- Dual Can
- Bootloader
  - USB/USART/CAN

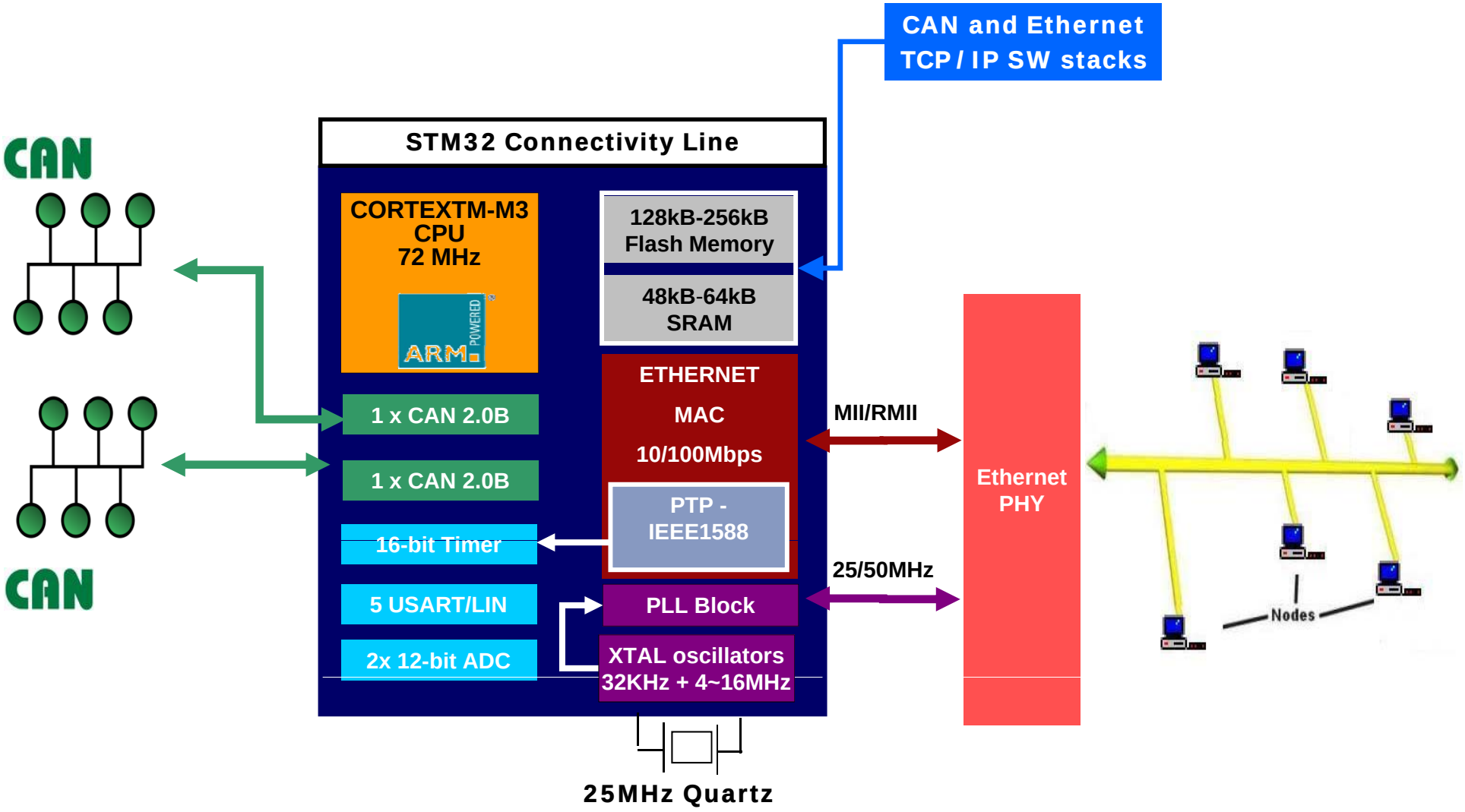


STM32 Connectivity Line Audio Applications Implementation example

- 147.46MHz PLL
- 2x Audio Classe I²S interface (16-32bit data)
  - →Master Clock support with better than 0.5% accuracy
  - →Audio sampling frequencies from 8kHz to 96kHz
- USB FS OTG with PHY
- SPI for SD card support



STM32 Connectivity Line Industrial gateway implementation example

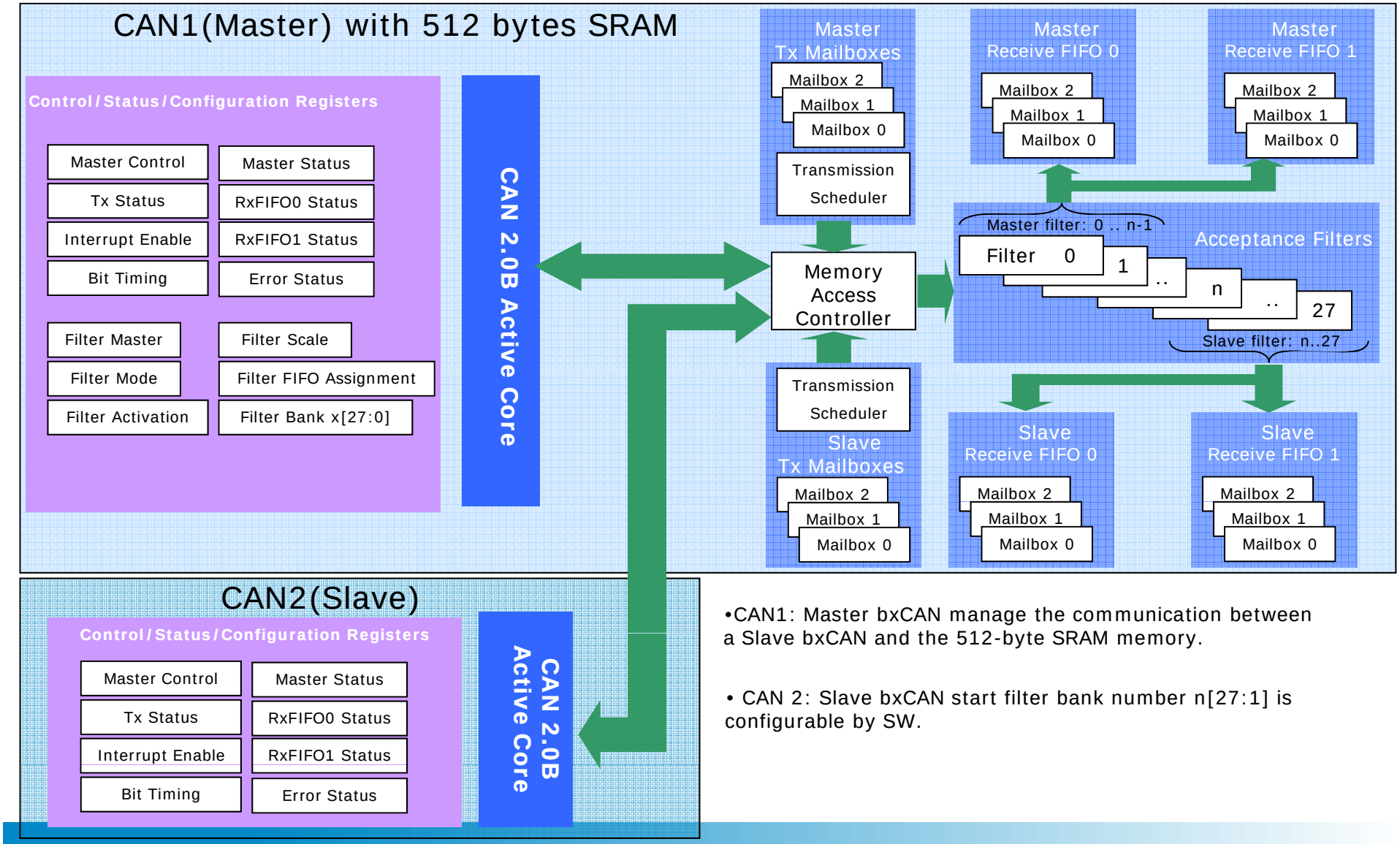


Controller Area Network (bxCAN)

CAN Features

- **Dual CAN** 2.0 A, B Active w/ Bit rates up to 1Mbit/s
- Support time Triggered Communication
- Three transmit mailboxes w/ configurable transmit priority
- Two receive FIFOs with three stages and 28 filter banks shared between CAN1 and CAN2
- Time Stamp on SOF reception and transmission
- Maskable interrupts for easy software management
- Software efficient mailbox mapping at a unique address space
- 4 dedicated interrupt vectors: transmit interrupt, FIFO0 interrupt, FIFO1 interrupt and status change error interrupt
- The two CAN cells share a dedicated 512-byte SRAM memory and capable to work simultaneously with USB OTG FS peripheral

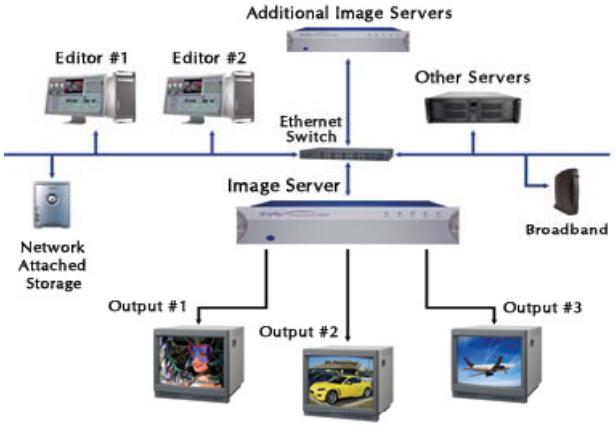
Block Diagram – Dual CAN



•CAN1: Master bxCAN manage the communication between a Slave bxCAN and the 512-byte SRAM memory.

• CAN 2: Slave bxCAN start filter bank number n[27:1] is configurable by SW.

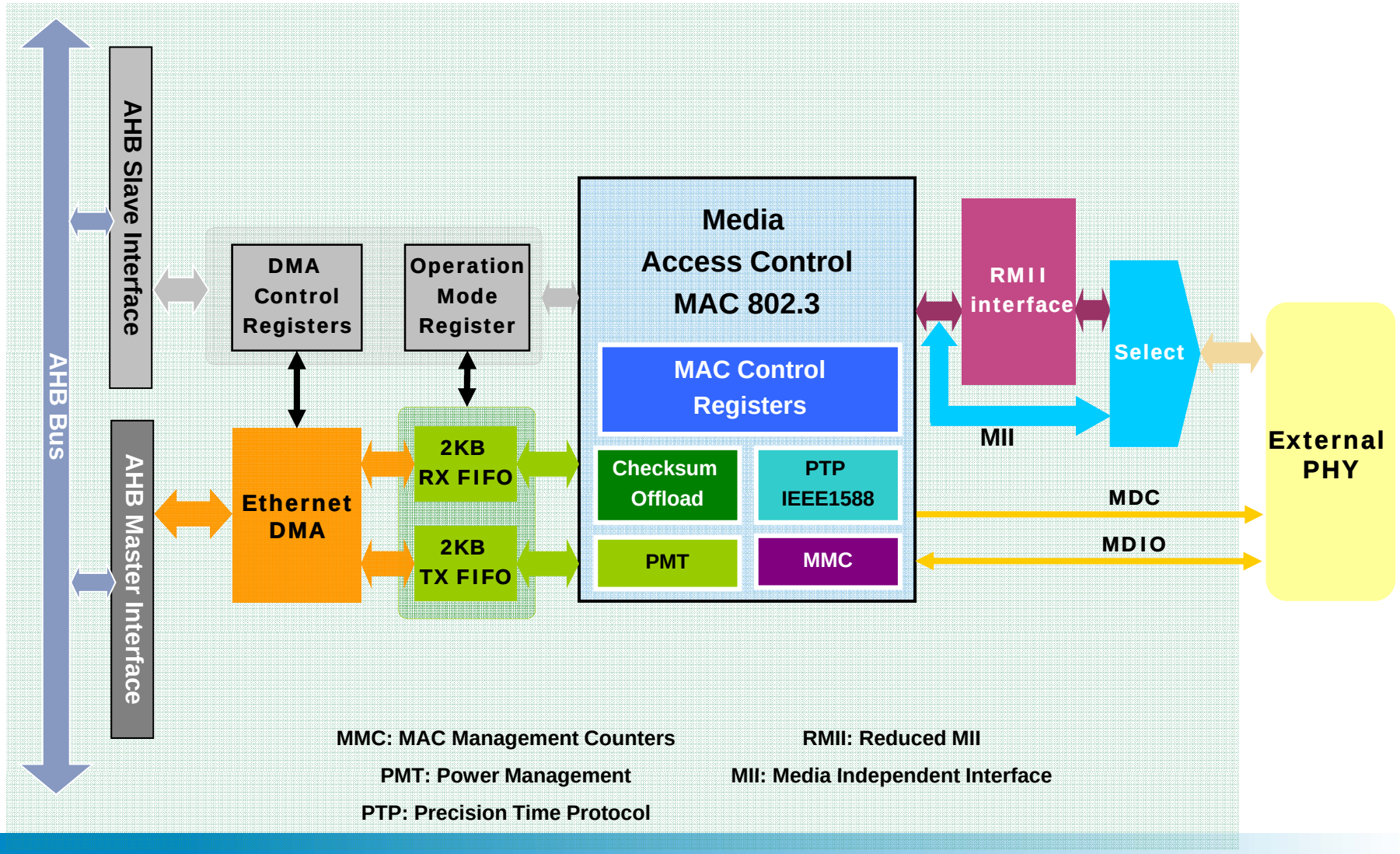
Ethernet MAC 10/100



STM32F107 Ethernet Interface Overview

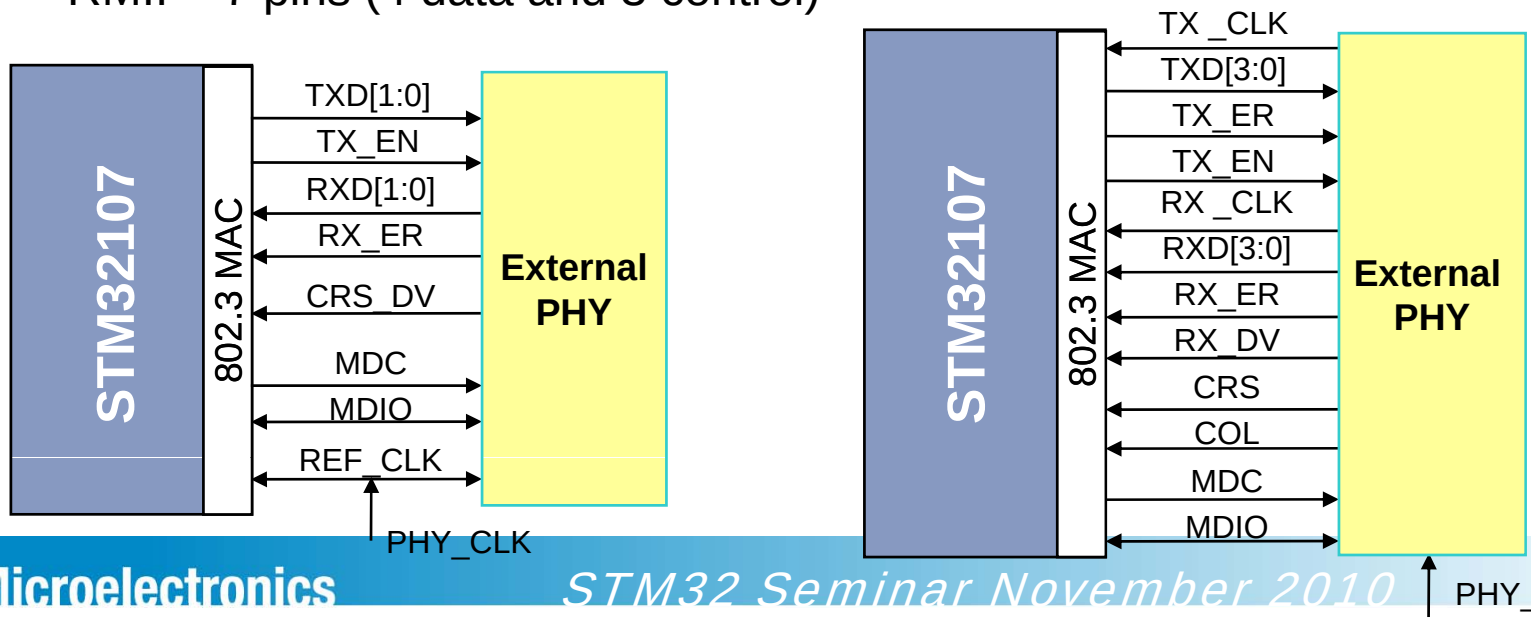
- Supports 10/100Mbits, Half/Full-duplex operations modes, with external PHY interface.
- Dedicated DMA controller with two sets of FIFOs.
- Supports Ethernet frame time stamping.
- Supports Power-down mode.
- Two interrupt vectors:
  - Ethernet normal operations.
  - Ethernet wakeup event.
- Compliant with the following standards:
  - IEEE 802.3-2002 for Ethernet MAC
  - IEEE 1588-2002 standard for precision networked clock synchronization
  - RMII specification from RMII consortium

Ethernet Block Diagram



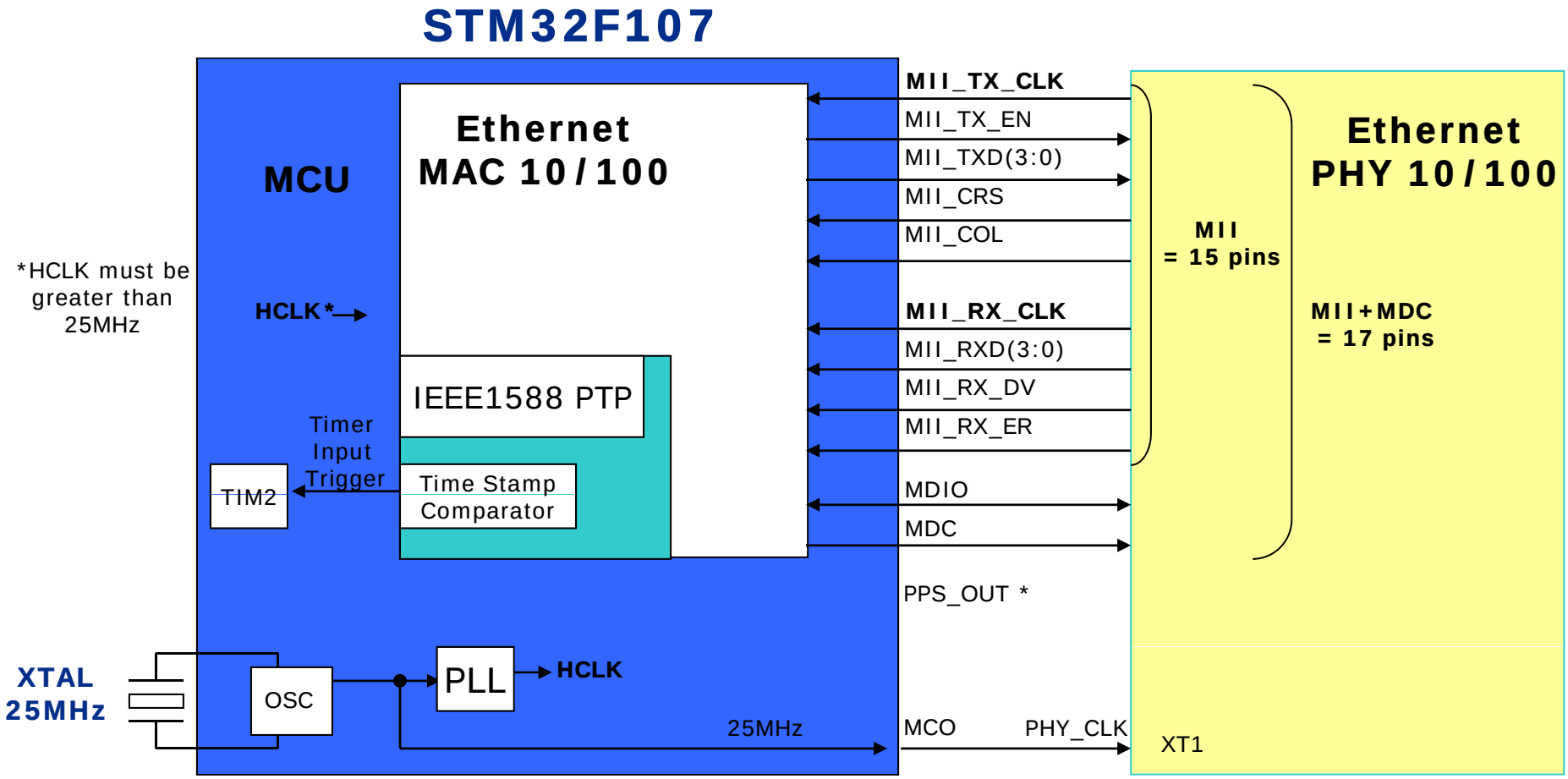
Physical Layer Interface

- Up to 32 PHY components can be interfaced.
- Supports both Media Independent Interface (MII) and Reduced Media Independent Interface (RMII).
- RMII is a lower pin count alternative, which targets multi-port applications and low cost design:
  - MII = 16 pins (8 data and 8 control)
  - RMII = 7 pins (4 data and 3 control)



Ethernet Interface Solution (1/4)

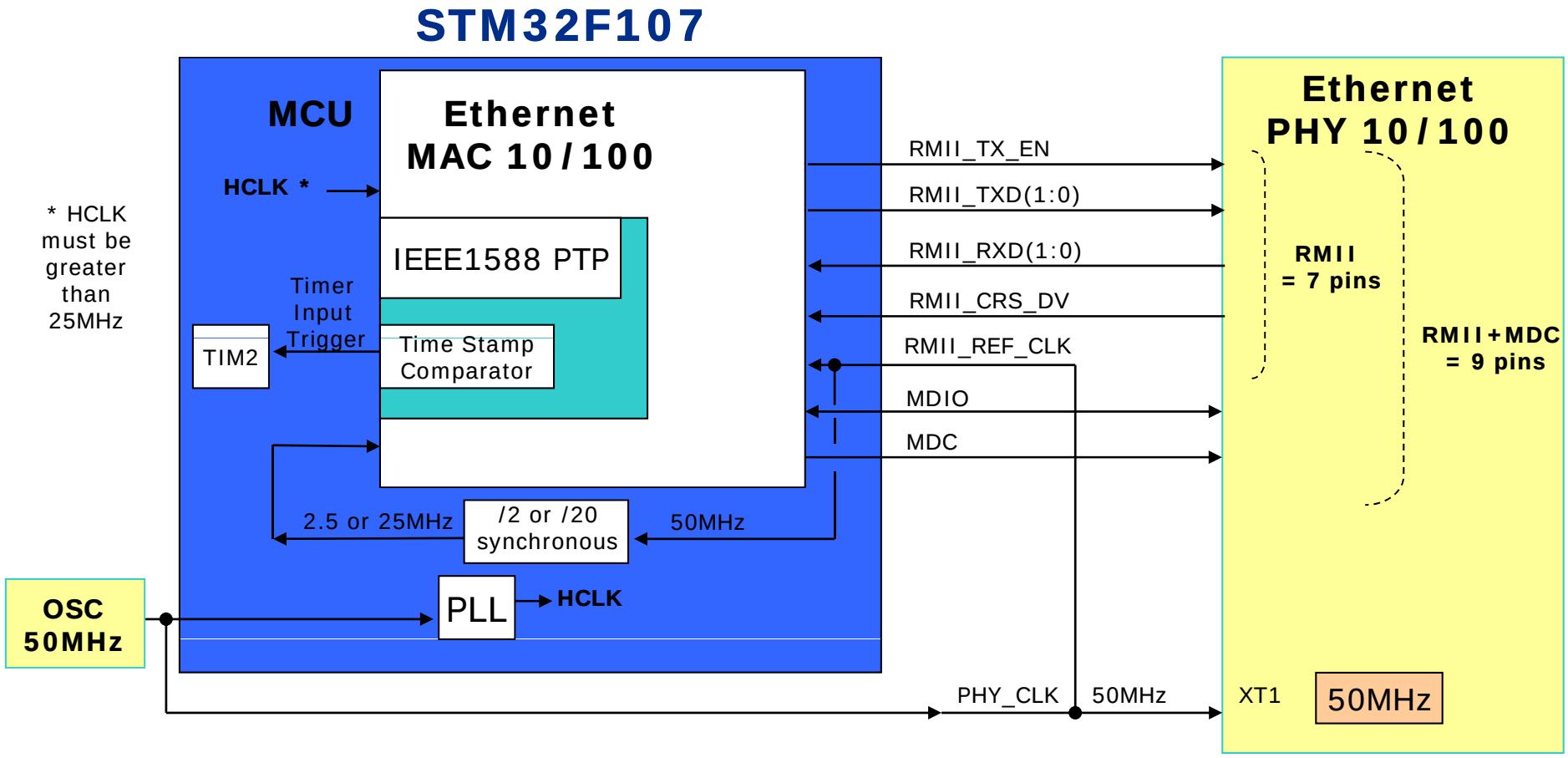
- MII mode using one 25MHz crystal



* Pulse Per Second when using IEEE1588 PTP, Optional Signal

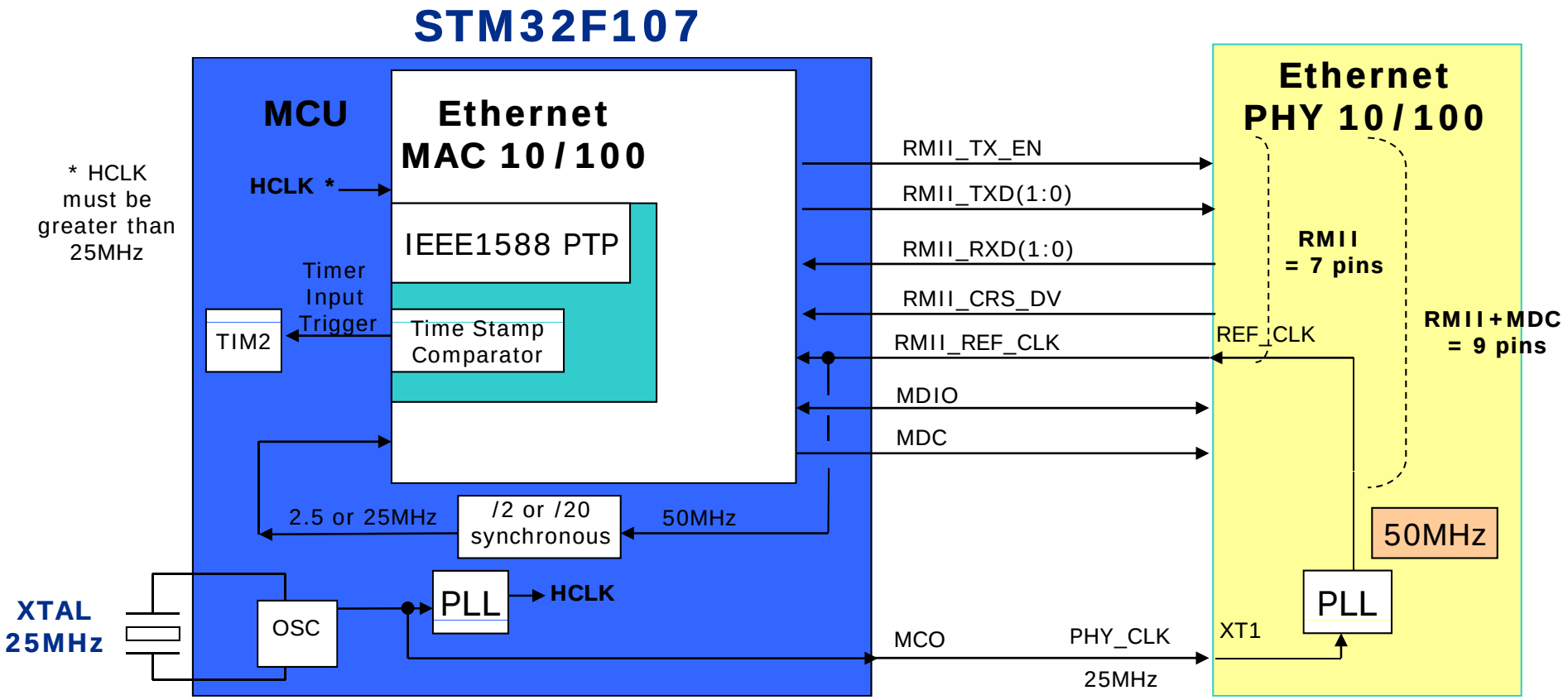
Ethernet Interface Solution (2/4)

- RMII with one 50MHz oscillator



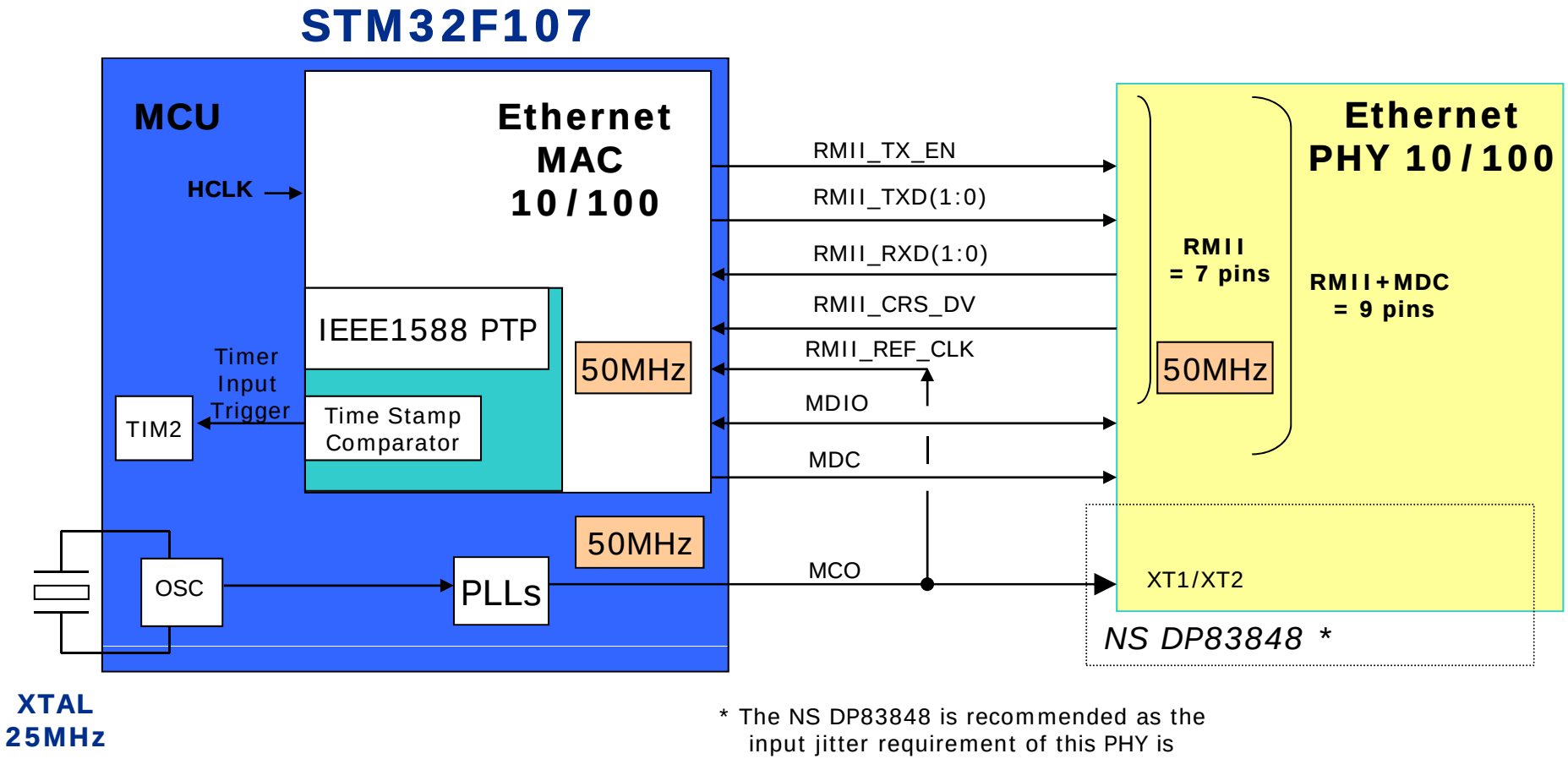
Ethernet Interface Solution (3/4)

- RMII with one 25MHz crystal and PHY with PLL



Ethernet Interface Solution (4/4)

- RMII with one 25MHz crystal



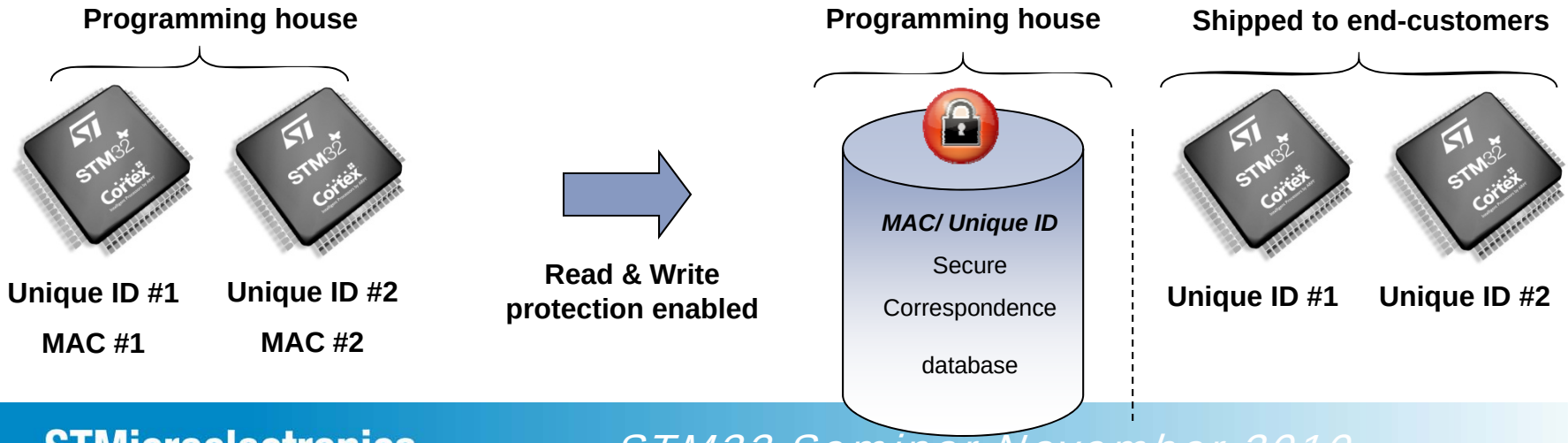
* The NS DP83848 is recommended as the input jitter requirement of this PHY is compliant with the output jitter specification of the MCU

Media Access Controller: MAC Features

- 10/100 Mbit/s transfer rates and Full/Half-duplex operation modes.
- Programmable frame length with size up to 16 KB.
- IEEE 802.1Q VLAN tag detection for reception frames.
- Checksum offload engine for transmit and receive of TCP/IP frames.
- Network statistics with RMON/MIB counters (RFC2819/RFC2665).
- Flexible address filtering modes.
- Power-down mode with Ethernet wakeup event.
- IEEE1588 Ethernet frame time stamping.
- Internal loopback on the MII for debugging.

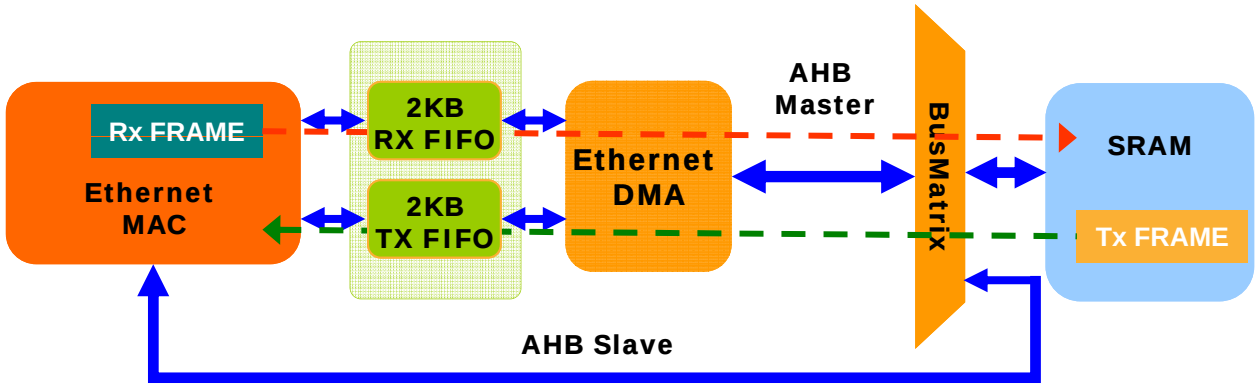
STM32F107 MAC address programming

- The IEEE organization is responsible of delivering MAC addresses.
- The MAC address (6 bytes long) is unique for every end-user Ethernet application in the world.
- Every STM32F107 device has a 96-bit unique ID.
- Once programmed in the user flash, the MAC address can be identified or re-programmed in the field thanks to the STM32 unique ID signature.



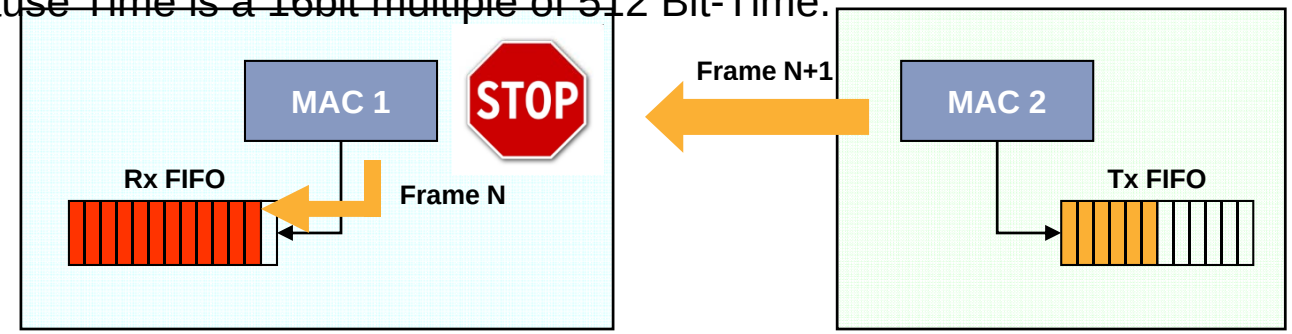
MAC FIFOs

- The MAC core has two sets of FIFOs, of 2KB each one, with a configurable threshold.
- Two modes for popping data towards the MAC, for frames transmission:
  - Threshold mode: as soon as the threshold level is reached.
  - Store-and-Forward mode: a complete frame is stored into the FIFO.
- Two modes for popping data towards the DMA, for frames reception:
  - Cut-through mode: as soon as the threshold level is reached.
  - Store-and-Forward mode: a complete frame is received into the FIFO.



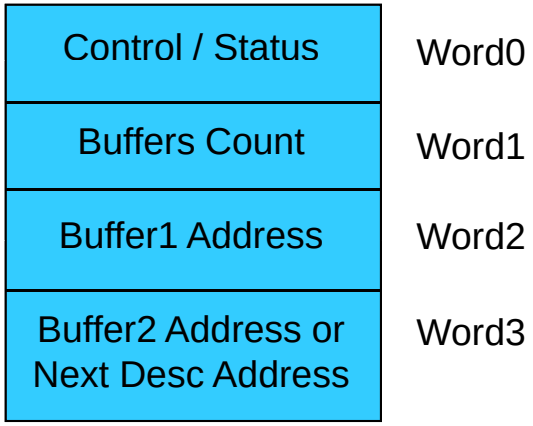
Flow Control

- Ethernet Flow Control consists on stopping temporarily data transmission.
- STM32F107 MAC supports Flow Control for Half/Full-duplex modes and can be:
  - Started automatically when the RX FIFO is Full.
  - Started by the Application.
- The Half-duplex Flow Control is provided by the Back Pressure mechanism.
- The Full-duplex Flow Control is provided by the Pause Frame mechanism:
  - Pause Frame is sent with multicast destination address 01-80-C2-00-00-01.
  - Pause Time is a 16bit multiple of 512 Bit-Time.



DMA Controller: Descriptors structure (1/2)

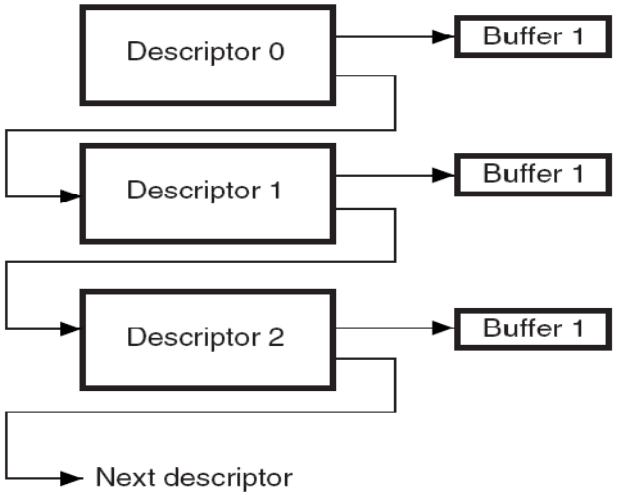
- The DMA transfers frames between the SRAM and the FIFOs.
- DMA transfers are managed by descriptors.
- Descriptors are configured by the user and located in the SRAM.
- Multiple descriptors are prearranged in two structures:
  - Ring structure.
  - Chain structure.
- Each descriptor is formed by four 32bit-words:
  - Word0: Control and Status information.
  - Word1: Counts.
  - Word2: (First) Buffer address
  - Word3: Ring mode: Second Buffer address.
    Chain mode: Next Descriptor address.



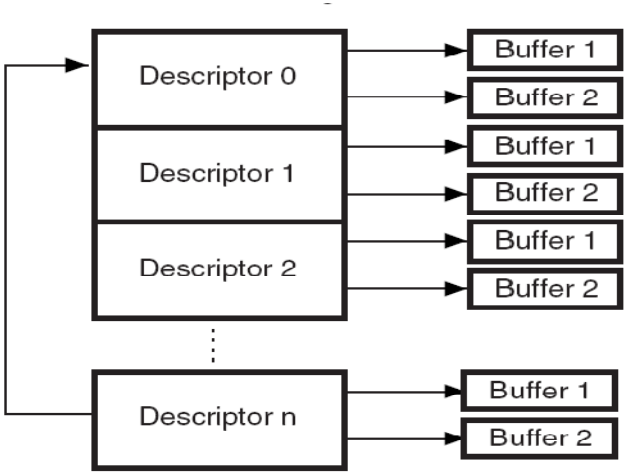
DMA Descriptor

DMA Controller: Descriptors Structure (2/2)

- **Chain mode**
  - Each descriptor can point to one buffer.
  - Each descriptor include the next descriptor address.



- **Ring mode**
  - Each descriptor can point to a maximum of two buffers.
  - Configurable descriptor skip length
  - The last descriptor point back to the first entry.



IEEE 1588 Precision Time Protocol

- PTP applies to local area networks supporting multicast messaging and aims to synchronize heterogeneous systems clocks with minimum network and local computing resources.

- The target accuracy of PTP IEEE1588-2002 V1 is the sub-microsecond range.

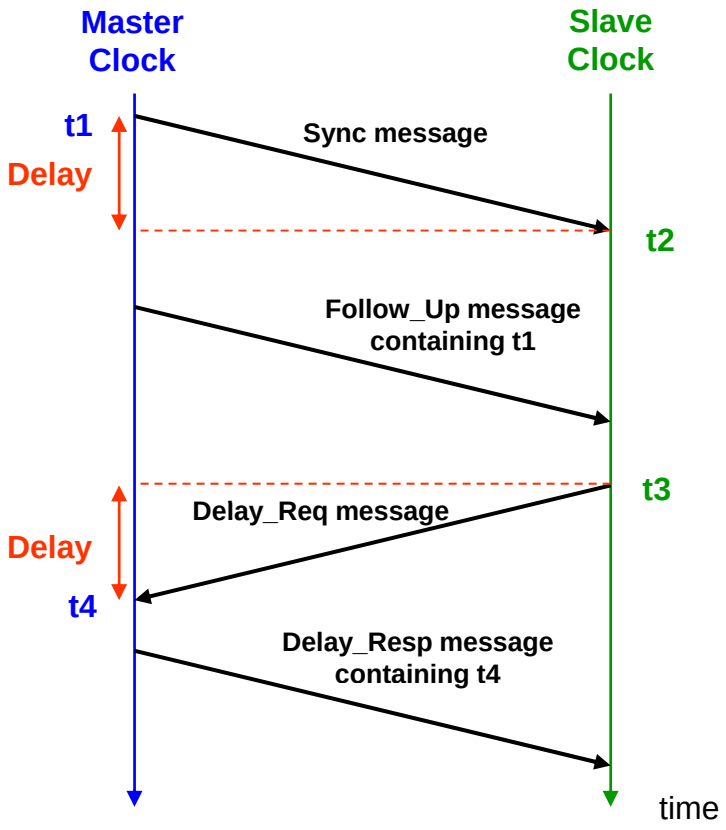
- IEEE1588 V2 improvements:
  - Sub-nanosecond accuracy.
  - Faster synchronization (SYNC) message rates.
  - Shorter PTP messages, unicast messaging, new messages (path delay request/response/response follow-up) and message fields:
  - Transparent Clocks.
  - Fault Tolerance.

IEEE1588 Precision Time Protocol Overview

- Clock synchronization is made into two stages:
  - Best clock selection.
  - Clock correction.

- The network is classified into Master and Slave nodes and the synchronization is done with the most accurate clock found: the Grand Master Clock.

- Offset estimation:
  - Slave lock = Master Clock + Offset
  - t2 = (t1 + Offset) + Delay
  - t3 = (t4 + Offset) – Delay
  - Offset = ½ [(t2 – t1) + (t3 – t4)]



USB 2.0 On-The-Go Full Speed (OTG FS)

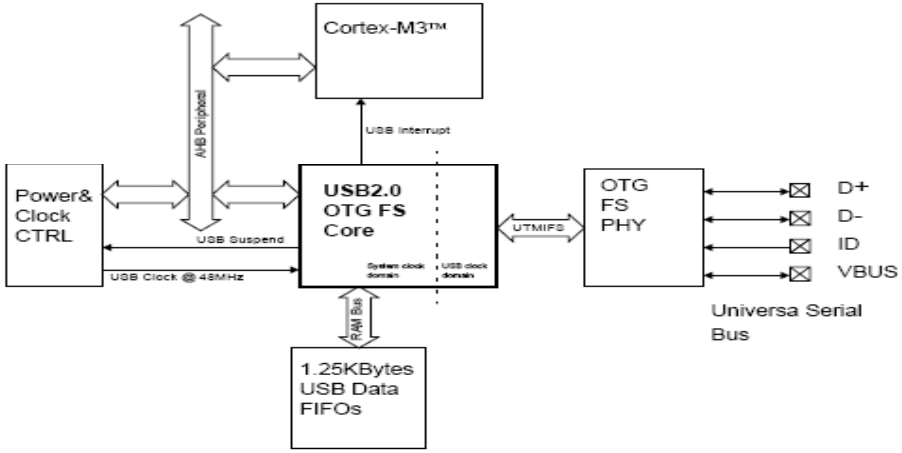
USB OTG FS core features 1/2

- **Main features**
  - Complies with the On-The-Go Supplement to the USB 2.0 Specification (Rev 1.3)
  - Operates in Full-Speed and Low Speed (FS, 12-Mbps, LS 1.5 Mbps) mode.
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP).
  - Operate in Host, device and OTG modes.

USB OTG FS core features 2/2

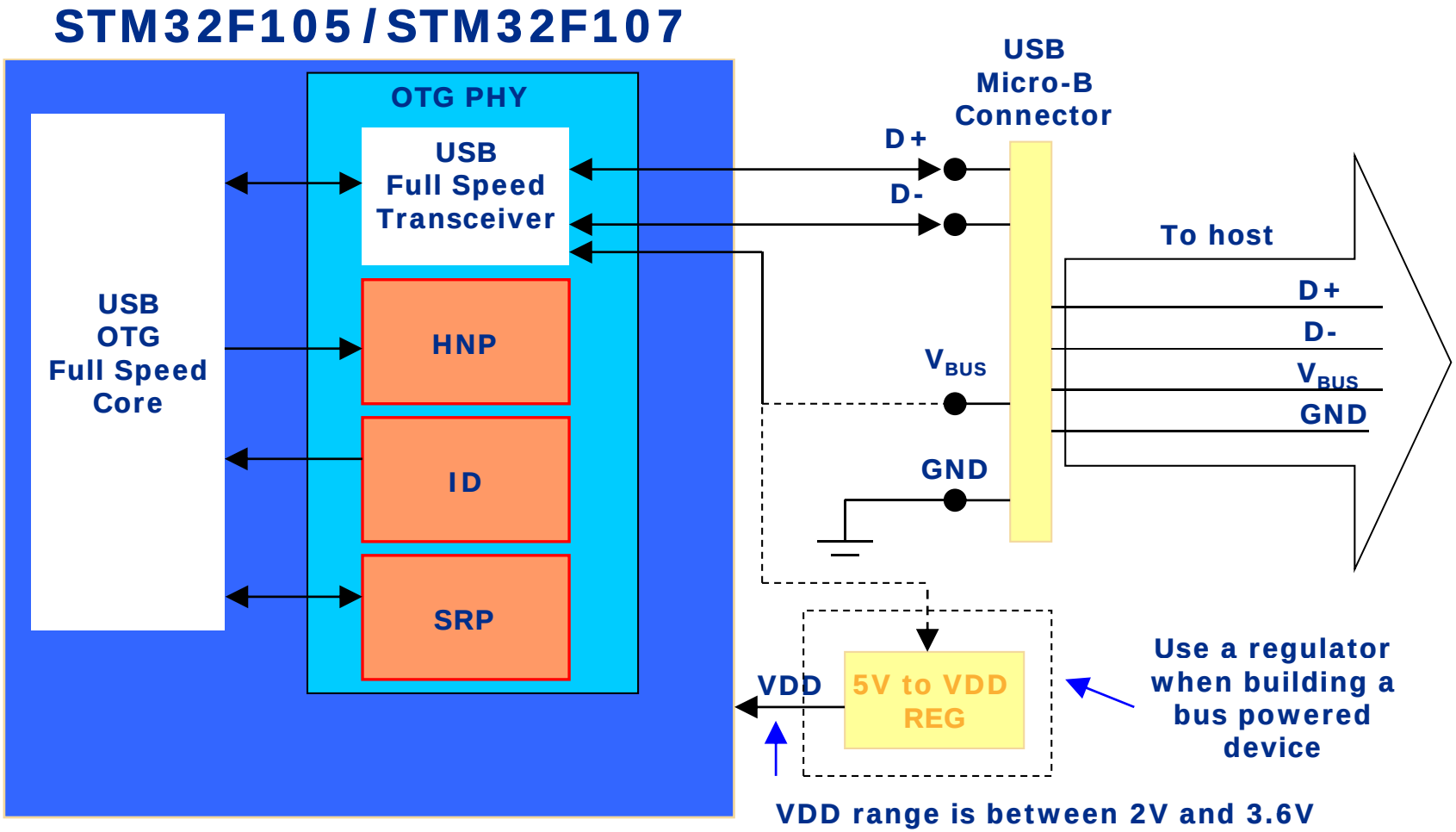
Characteristics

- 4 bidirectional endpoints, including:
- 1 control endpoint 0 and 3 device endpoints which support bulk interrupt, isochronous.
- 8 host channels with periodic OUT support.
- Dedicated transmit FIFO for each of the 4 device IN endpoints. Each FIFO can hold multiple packets.
- Combined Rx and Tx FIFO size of 320 x 35bit with Dynamic FIFO sizing (1.25 KB).
- 8 entries in periodic Tx queue, 8 entries in non periodic Tx queue.
- Controls OTG FS PHY on-chip for Host, Device or OTG operation
- Requires an external Charge pump for VBUS Voltage.
- 32-bit AHB Slave interface for accessing Control and Status Registers (CSRs), Data FIFO.
- Provides a trigger interrupt in each SOF, connected to Timer 2.



USB interface solution (1/3)

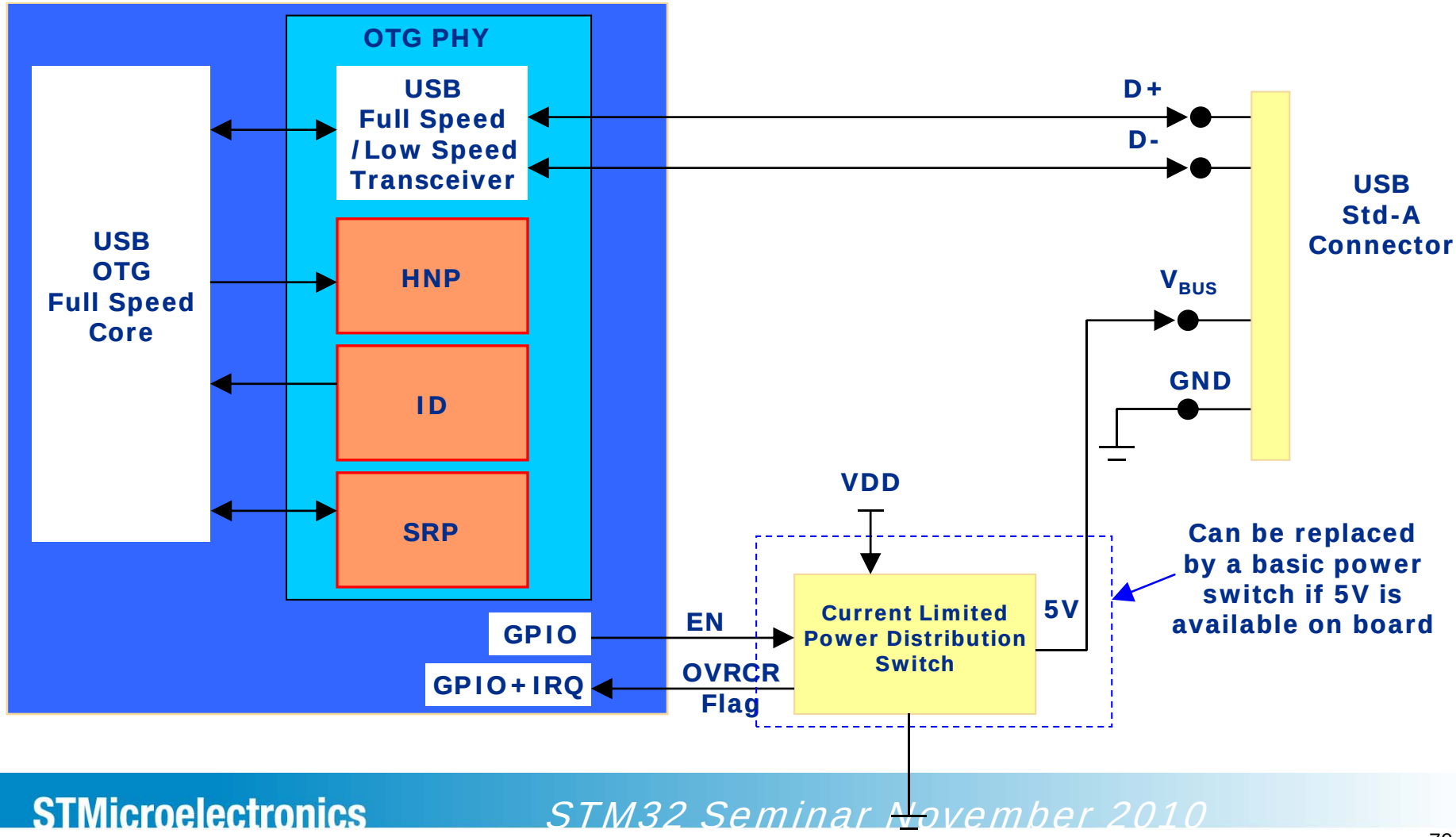
- STM32: USB device mode



USB interface solution (2/3)

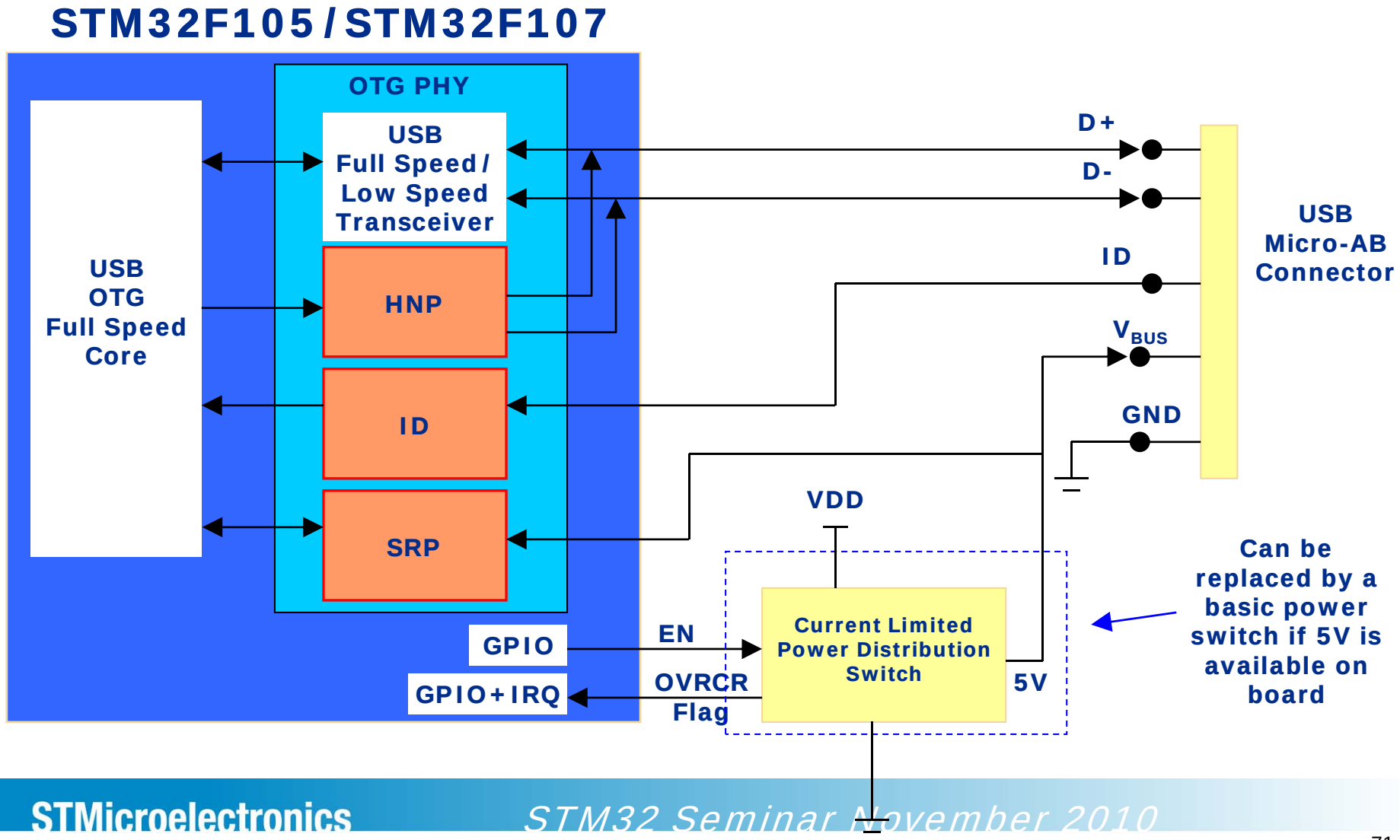
- STM32: Host connection

STM32F105/STM32F107



USB interface solution (3/3)

- STM32: OTG connection



Stacks & Tools

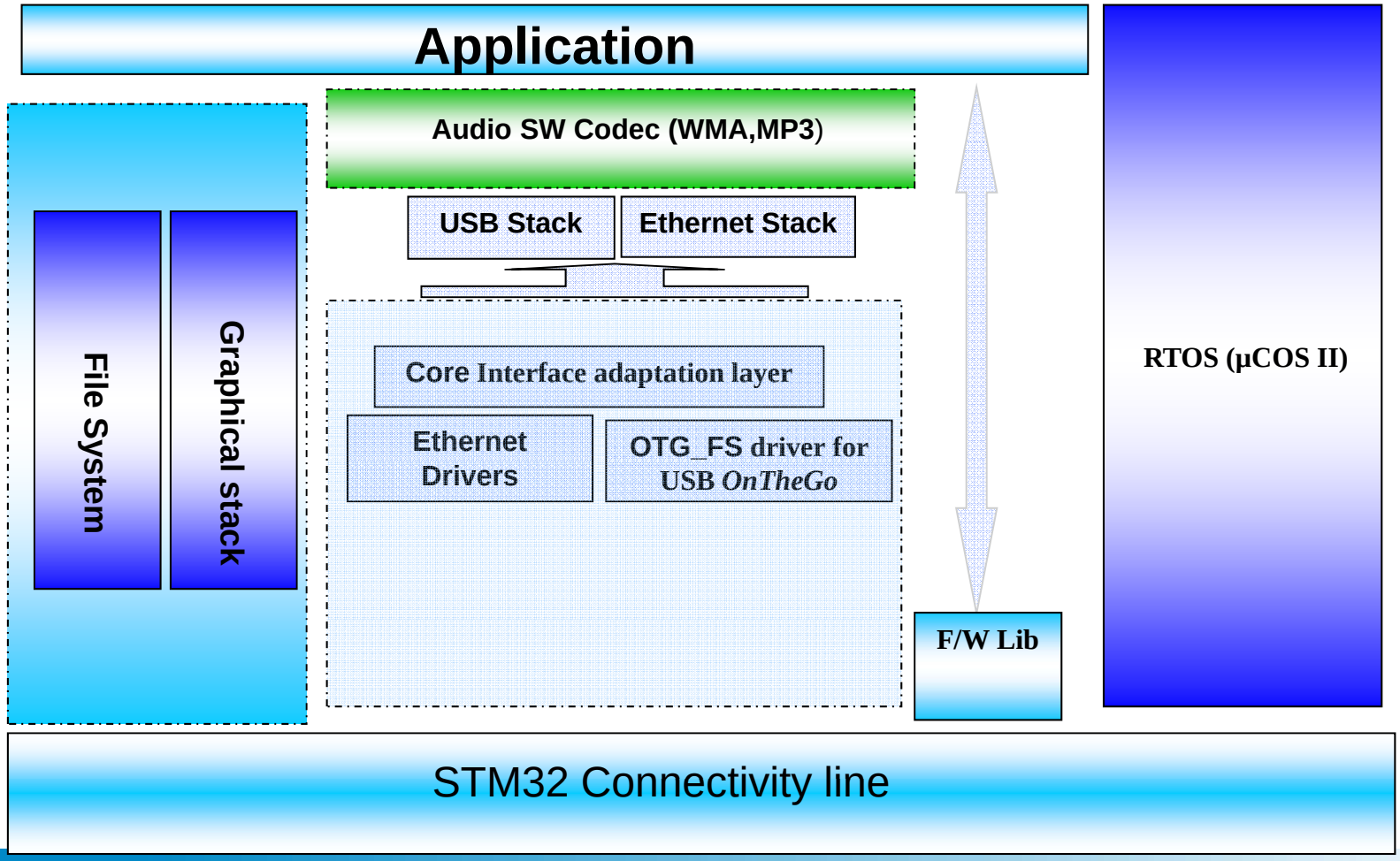
ST Solutions

- USB OTG/Host:
  - USB OTG Low-level firmware (Web)
  - USB Host free stack + MS/HID (Dec´2010)

- Ethernet
  - Ethernet Low-level firmware (Web)
  - lwIP TCP/IP stack demonstration (Web AN3102)
  - IAP over Ethernet (Web AN3226)

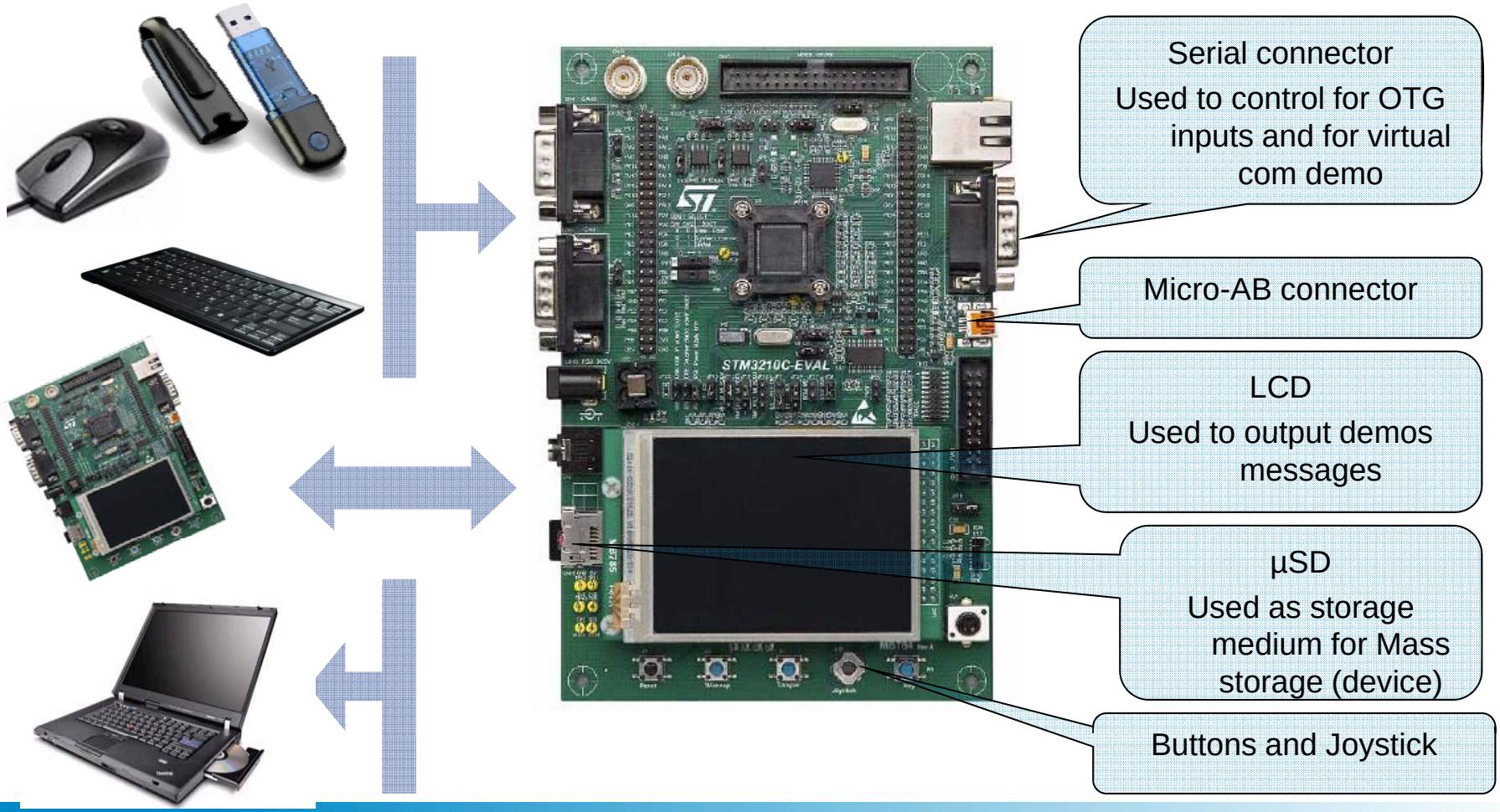
Firmware Packages & Applications Architecture

- Standard F/W library
- Micrium: µCOS2 RTOS
- Micrium: USB OTG/host/device stacks
- Micrium: USB OTG/host/device stacks
- SEGGER: Graphical stack & File System
- Interniche: Ethernet TCP/IP stack
- Software MP3 decoder
- Software WMA decoder



Connectivity Firmware Eval-Board

- The demos are built around uC/OS-II RTOS and uC/USB stack and use the STM3210C-EVAL board

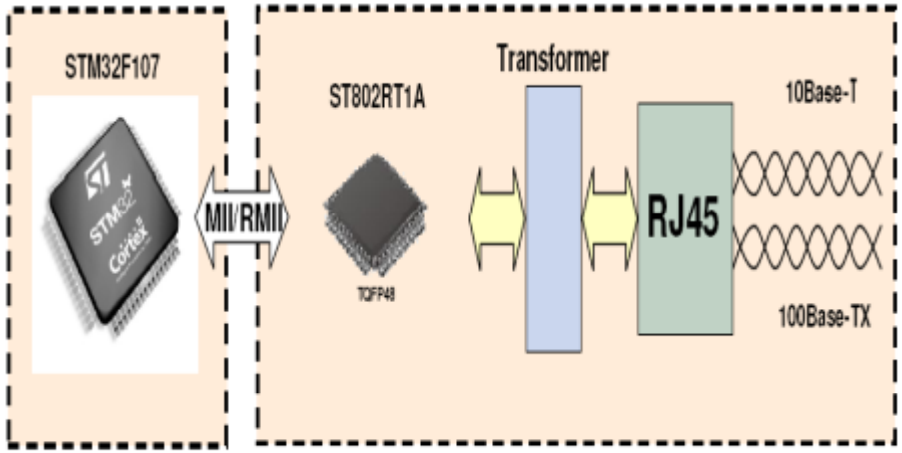


STM32F107+ST802RT1A Ethernet PHY STEVAL-PCC010V1 demo board

STEVAL-PCC010V1 demo board includes 2 boards

STM32F107
demonstration board

ST802RT1A
demonstration board



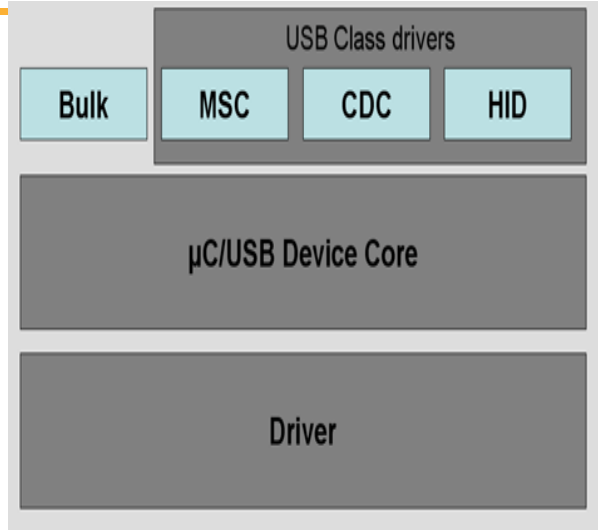
RRP 70EUR

USB OTG software solutions

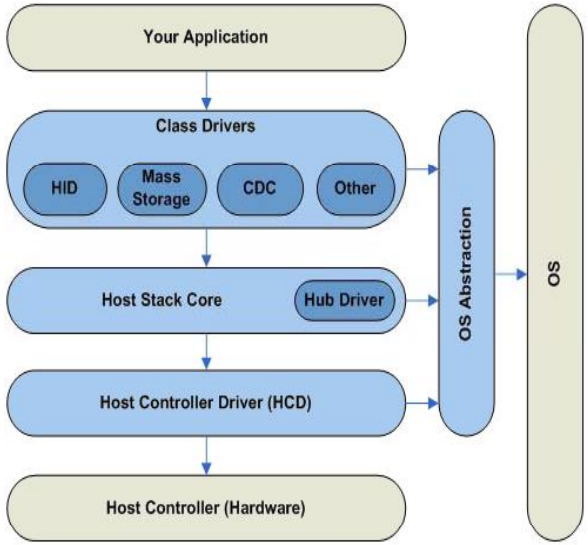
Logo	Company	Product	USB Device	USB Host	USB OTG	Website
HCC	HCC-Embedded	USB	Yes	Yes	Yes	www.hcc-embedded.com, /www.hcc-embedded.com/en/solution/st_micro
IAR SYSTEMS	IAR	PowerPac USB	Yes	Yes	Yes	www.iar.com, www.iar.com/st
KEIL An ARM® Company	Keil	RL-USB	Yes	-	-	
µC/USB OTG	Micrium	µC/USB	Yes	Yes	Yes	www.micrium.com, www.micrium.com/st/index.html
µd Micro Digital	Micro Digital	smxUSBD smxUSBH smxUSBO	Yes	Yes	Yes	www.smxrtos.com, www.smxrtos.com/stmicro.htm
Quadros Systems Inc.	Quadros Systems	RTXCusb	Yes	Yes	Yes	www.quadros.com
SEGGER	Segger	emUSB	Yes	Yes	Yes	www.segger.com

USB OTG FS: Micrium Offering

µC/USB-Device
- Bulk-device stack
- HID, MSD, CDROM Classes
- Audio class will be available in Q2 2009



µC/USB-Host
- HID, CDC, MSD, Audio, Printer Classes
- OHCI, EHCI, UHCI
- Audio class will be available in Q2 2009

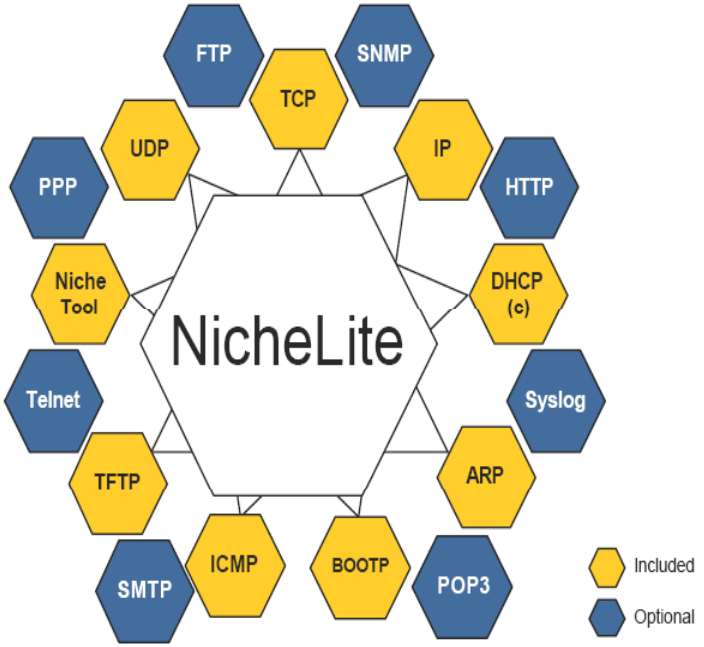


µC/USB-OTG

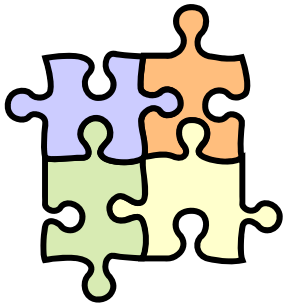
Ethernet Firmware solution

- ***Ethernet package <u>from ST</u>***
  - Low level driver
  - Free webserver demo based on NicheLite stack ➔ distribution through Interniche web site with link from ST web (user has to sign an agreement)
  - Free webserver demo based on uIP v1.3 stack ➔ distribution through ST web
  - AN "*NicheLite TCPIP stack use for STM32*"

    ➔ customizing/configuring the NicheLite stack to get the best with the Connectivity Line : memory management, performances, footprint...



- ***Third party software***
  - Other TCP/IP stack providers are working to support Connectivity line (Keil, Micrium, IAR, Segger, CMX, Quadros, eCosCentric…)



Ethernet software solutions from 3rd parties

Logo	Company	Product	Website
	Interniche	NicheLite	www.iniche.com, www.st.com/mcu
	IAR	PowerPac TCP/IP	www.iar.com, www.iar.com/st
	Keil	RL-TCPnet	www.keil.com
	Micrium	µC/TCP-IP	www.micrium.com, www.micrium.com/st/index.html
	Micro Digital	smxNS	www.smxrtos.com, www.smxrtos.com/stmicro.htm
	Quadros Systems	RTXC Quadnet RTXC Quark	www.quadros.com
	Segger	embOS/IP	www.segger.com

Micrium µC-OS/III and STM32F107 evaluation board

- Micrium's newest RTOS µC-OS/III bundle: a two-part book accompanied by an ST STM32F107 evaluation board.
  - The 1st part covers the internals of µC/OS-III
  - The 2nd part provides examples for using µC/OS-III on the popular STM32
- Available at Amazon, $199.95
- Available through ST: **STM32CMICOS-EVAL**, DCPL is $159 and RRP $199.95

STM32 Compact Dev Kit for Ethernet, USB OTG

- STM32 ComStick
  - *Everything* included
  - Firmware, User's Guide, CD
  - USB bus powered
- Demonstrate and Evaluate Ethernet, USB OTG connectivity
  - Web server with TCP/IP
  - USB mouse, USB host..
- *Full tool-chain* from Hitex*
  - *No limit to code size*
  - Full capability: Editing,compiling, Flash programming, and debugging with HiTop environment
- Access to I/O pins
  - ADC, PWM, GPIO

69$

Order from ST or from Hitex

* For use on one STM32 ComStick dongle

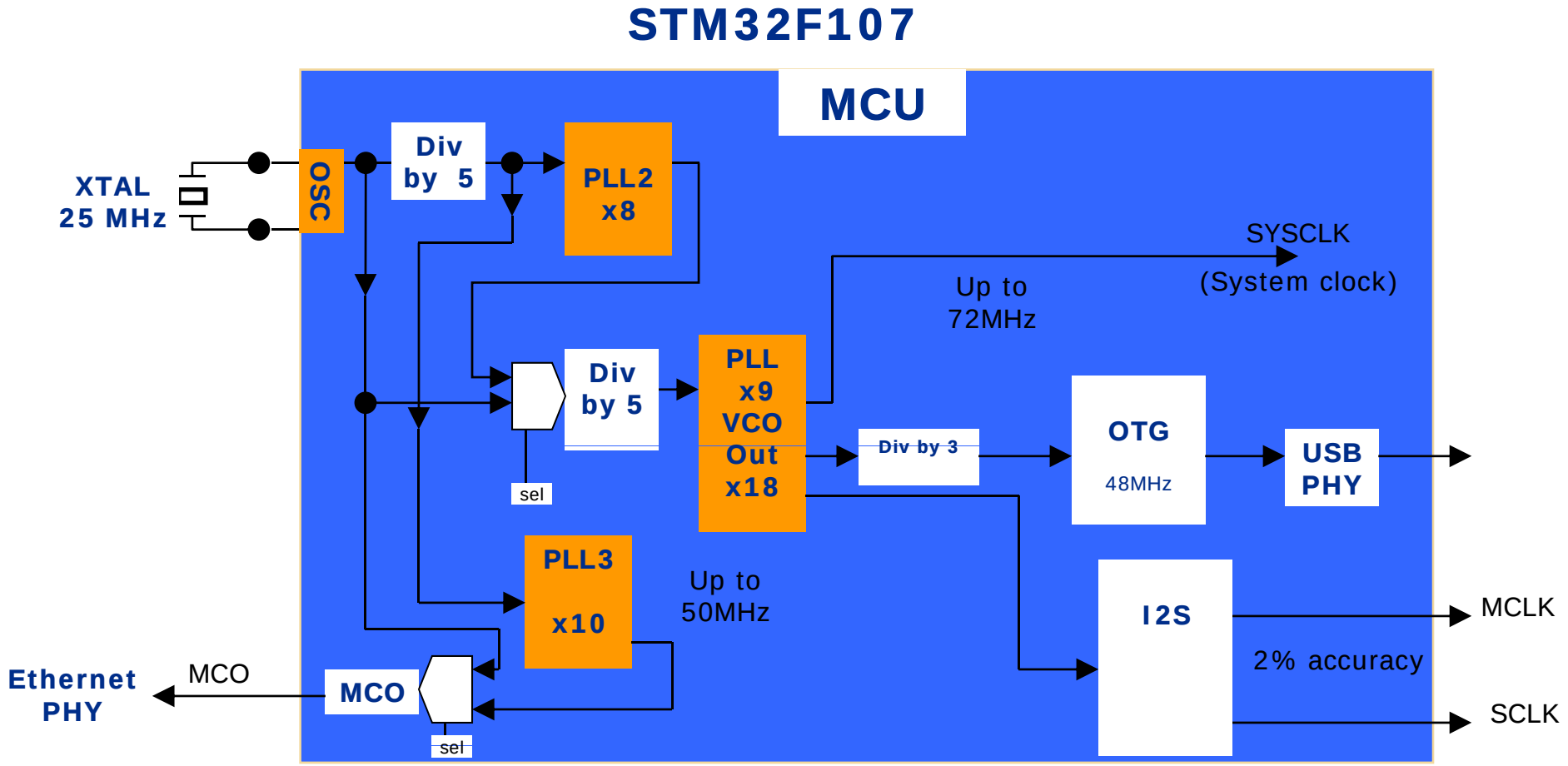
Enhanced Clock Scheme and Audio Class I2S

Enhanced Clock Scheme: Overview

- Connectivity Line implements an enhanced clock scheme w/ 3 PLLs and multiple selection of clock output sources (MCO pin)
  - Up to 8 clock signals can be output onto the external MCO pin (PA.08).
    - SYSCLK
    - HSI
    - HSE
    - PLL clock divided by 2 selected
    - PLL2 clock selected
    - PLL3 clock divided by 2 selected
    - XT1 external 3-25 MHz oscillator clock selected (for Ethernet)
    - PLL3 clock selected (for Ethernet)
  - With single *25MHz crystal* you can have at the same time
    - System clock up to 72MHz
    - 48MHz for USB OTG
    - 25/50MHz for external Ethernet PHY
  - With *14.7456MHz audio crystal* you can have at the same time
    - System clock up to 71.88MHz
    - Best in class I2S master clock capable to generate all standard sampling frequencies from 8 kHz to 96 kHz with less than 0.5% accuracy
    - Functional USB OTG (47.9232MHz input clock w/ 0.16% accuracy)

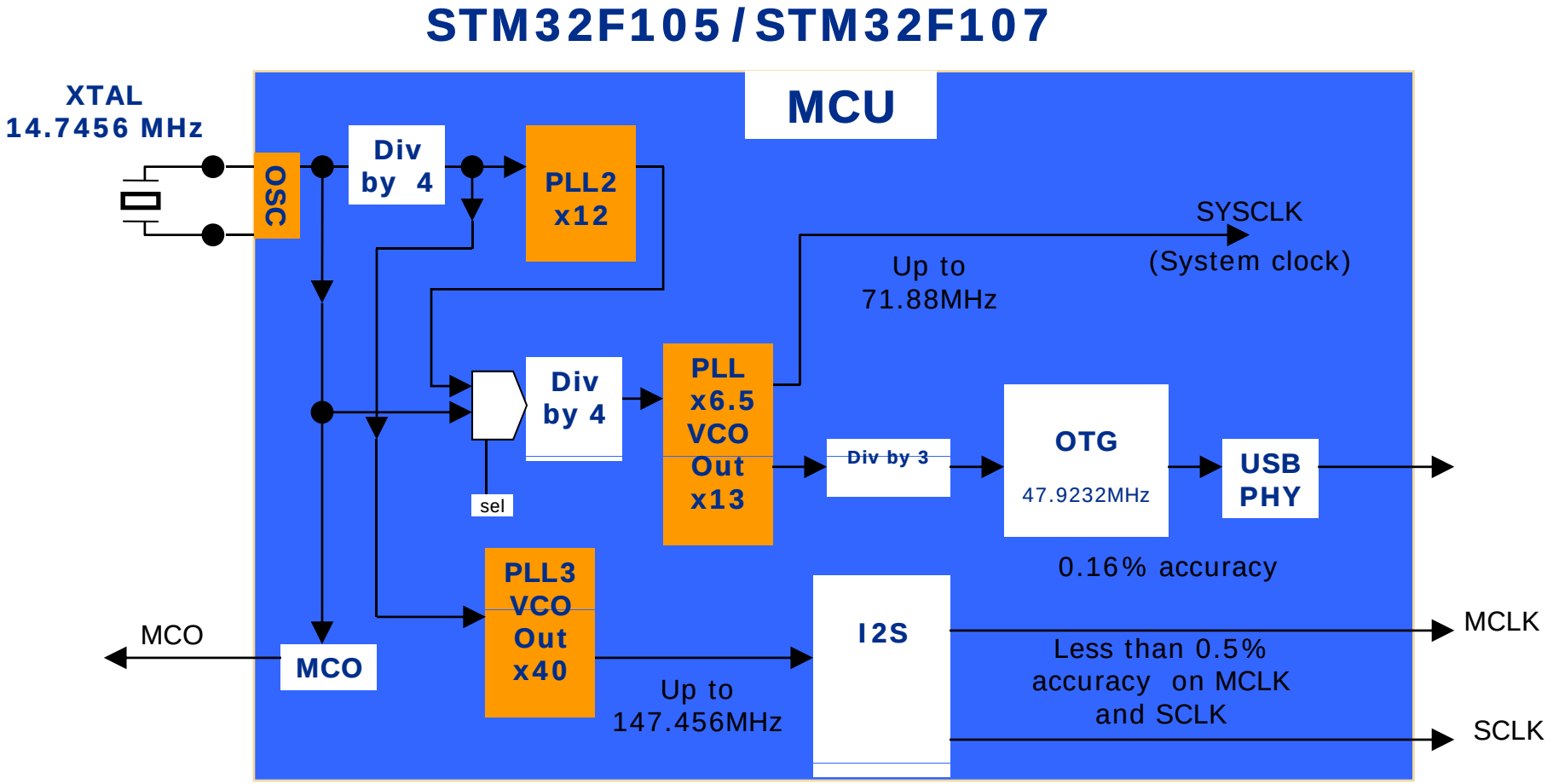
Enhanced Clock Scheme: OTG + Ethernet Solution

- The new clock tree allows to work with USB (host/device/OTG) and Ethernet (MII/RMII) with only **ONE** crystal



Enhanced Clock Scheme: OTG + Audio Class I2S

- The new clock tree allows to work with USB (host/device/OTG) and Audio (I2S) with only **ONE** crystal



Enhanced Clock Scheme: Audio class I2S

- For Connectivity Line devices (Audio Class compliant)
  - A separate PLL (PLL3) is dedicated for the I2S clock generation, thus allowing precision up to 0.0064% with usual 25MHz crystal for frequencies from 8KHz to 96KHz.
  - A precision external quartz could be used to increase accuracy up to 0.0%
    - Typically 14.7456MHz crystal preferred for 32KHz-Group (8, 16, 32, 48, 96 KHz)
    - Typically 16.93444MHz crystal preferred for 44.1KHz-Group (11.025, 22.050, 44.1 KHz)

Audio-frequency precision using standard 25 MHz & PLL3 and using standard 14.7456 MHz & PLL3 are available in the Reference manual Section "23.4.3 Clock generator"

Enhanced Clock Scheme: PLLs Configuration

PLL Configuration Table is available in STM32F105/107 Datasheet:

“Appendix A Applicative block diagrams”

Application	Crystal Value (XT1)	PREDIV2	PLL2MUL	PLLSRC	PREDIV1	PLLMUL	USB Prescaler (PLL VCO output)	PLL3MUL	I2Sn Clock Input	MCO (Main Clock Output)
Ethernet Only	25MHz	/5	PLL2ON x8	PLL2	/5	PLLON x9	Don’t care	PLL3ON x10	Don’t care	XT1 (MII) PLL3 (RMII)
Ethernet + OTG	25MHz	/5	PLL2ON x8	PLL2	/5	PLLON x9	/3	PLL3ON x10	Don’t care	XT1 (MII) PLL3 (RMII)
Ethernet + OTG + Basic Audio	25MHz	/5	PLL2ON x8	PLL2	/5	PLLON x9	/3	PLL3ON x10	PLL	XT1 (MII) PLL3 (RMII)
Ethernet + OTG + High Quality Audio *	14.7456 MHz	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	/3	PLL3ON x20	PLL3	Don’t care. ETH PHY must use its own crystal
OTG Only	8MHz	Don’t care	PLL2OFF	XT1	/1	PLLON x9	/3	PLL3OFF	Don’t care	Don’t care
OTG + Basic Audio	8MHz	Don’t care	PLL2OFF	XT1	/1	PLLON x9	/3	PLL3OFF	PLL	Don’t care
OTG + High Quality Audio *	14.7456 MHz	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	/3	PLL3ON x20	PLL3	Don’t care.
High Quality Audio Only *	14.7456 MHz	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	Don’t care	PLL3ON x20	PLL3	Don’t care.

* The SYSCLK is 72MHz except in this case SYSCLK will be at 71.88MHz

Connectivity Line Audio-frequency precision vs High Density

Supported I²S Audio sampling frequency								
Nominal I²S Audio sampling frequency	Current High Density				Connectivity with Audio support improvement			
	Audio applications (USB supported) with Input OSC Freq = 8 MHz		Audio applications (no USB supported) with Input OSC Freq = 6.144MHz		Ethernet / USB OTG FS / Audio supported with Input OSC Freq = 25MHz / Fcpu = 72MHz		USB OTG FS/ Audio supported with Input OSC Freq = 14.7456MHz / Fcpu = 71.88Mhz	
	Actual Sampling Freq	MCLK Error %	Actual Sampling Freq	MCLK Error %	Actual Sampling Freq	MCLK Error %	Actual Sampling Freq	MCLK Error %
96kHz	93.75	2.34	88	8.33	97.66	-1.72	96	0
48kHz	46.87	2.34	44	8.33	48.83	-1.72	48	0
44.1kHz	46.87	-6.29	44	-0.23	43.40	1.58	44.31	-0.47
32kHz	31.25	2.34	33	-3.12	32.55	-1.73	32	0
22.05kHz	21.63	1.88	22	2.94	21.70	1.58	22.15	-0.47
11.025kHz	15.62	2.34	11	0.23	11.16	-1.23	11.07	-0.47
8kHz	8.03	-0.44	8	0	7.97	0.35	8	0

High density Audio-frequency precision using standard 8 MHz HSE is available in the reference manual Section "23.4.3 Clock generator"

STM32 Audio Solutions

Complete STM32 Spirit DSP Audio Engine

- MP3 solutions from Spirit DSP
  - MP3 decoder with built-in equalizer
  - MP3 decoder+encoder (codec)
- WMA solutions from Spirit DSP
  - WMA decoder with built-in equalizer
- Audio utilities from Spirit DSP :
  - SPIRIT Channel Mixer Utility (for volume and mute control)
  - SPIRIT Stand-alone 3 bands Parametric Equalizer Utility
  - SPIRIT Loudness Control Utility

STM32 SPIRIT DSP audio engine

- ST has licensed a complete audio engine solution from SPIRIT DSP:
  - MP3, WMA and audio utilities software packages are available in object codes only, accessed by the user application through an API.

- Solution Licensing :
  - A license agreement requires that customers limit the usage of this solution to STM32 products only. A software and hardware protection mechanism checks that the SW is used on STM32 products only.
  - Even though this solution is free of charge, MP3 and WMA royalties must be paid to the corresponding patents owners (Thomson, Microsoft).
  - For MP3 royalties, ST is allowed to sub license MP3 rights from Thomson Licensing:
    - Royalties are included in the chip pricing ➔ the end customer does not need to pay MP3 royalties to Thomson Licensing.

➔ Delivery process:
  - After all required licenses are signed by the customers, ST will ship a free CDROM ordered by ST local sales and marketing people.

MP3 / WMA Library Ressources Usage

SPIRIT Audio Engine	Algorithm	Peak MIPS(*)	Average MIPS	Memory, Kbytes	
				Flash Total	RAM Total
MP3	Decoder	28	23	21.3	12.3
MP3 (optimized)	Decoder	22	20	21.3	12.3
MP3	Encoder	33	27	25.7	15.6
WMA Standard	Decoder	30	25	51.2	36
Parametric Equalizer	Utility	33	33	4	3
Loudness Control	Utility	10	8	2	3
Channel Mixer	Utility	4	4	2	6

Welcome & Main screen

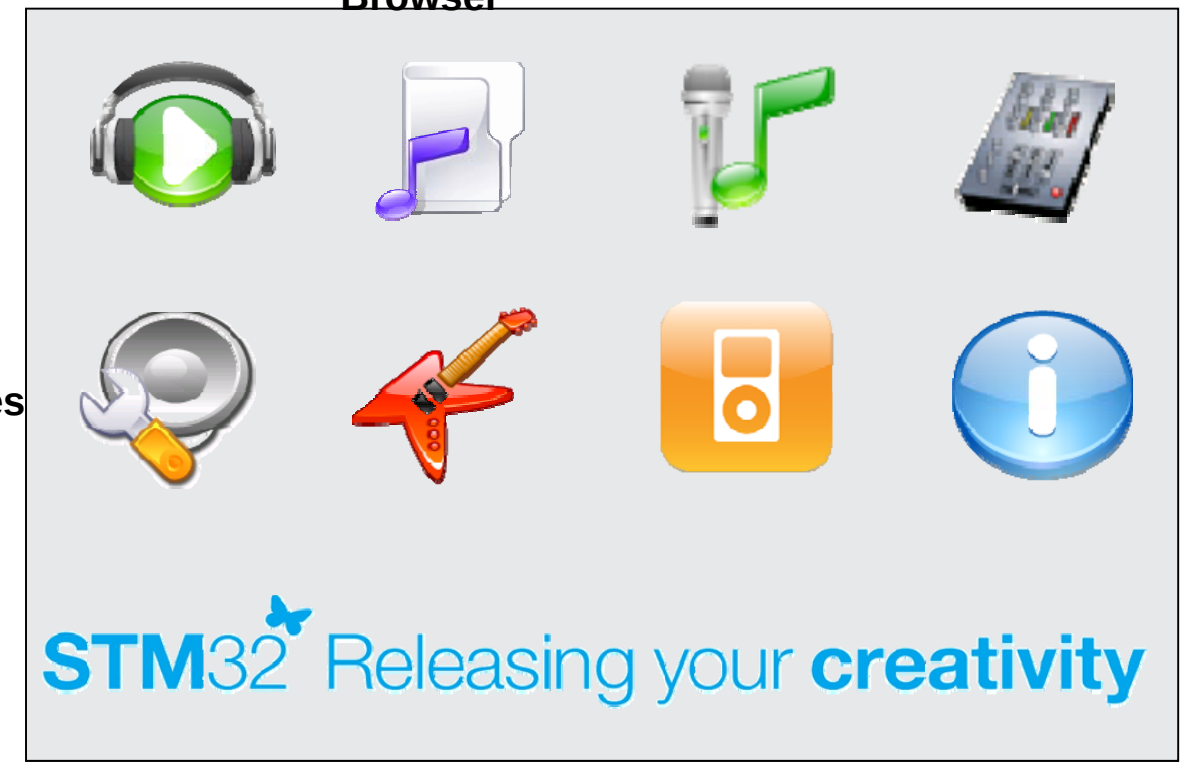
Media Player
WAV, MP3, WMA

Media Browser

MP3 Encoder

MP3

Mixer



Audio Utilities
Loudness
5 bands
Equalizer

Info & Credits

Karoake
Game

iPod Control
Under construction

Player Window (wav,mp3,wma)

Tags Display
WMA, MP3

Progress Bar

Volume Control
Using Software Mixer

Cursor (Multi-Input)
Joystick & Touch

Mute Control

Play

Pause

Stop

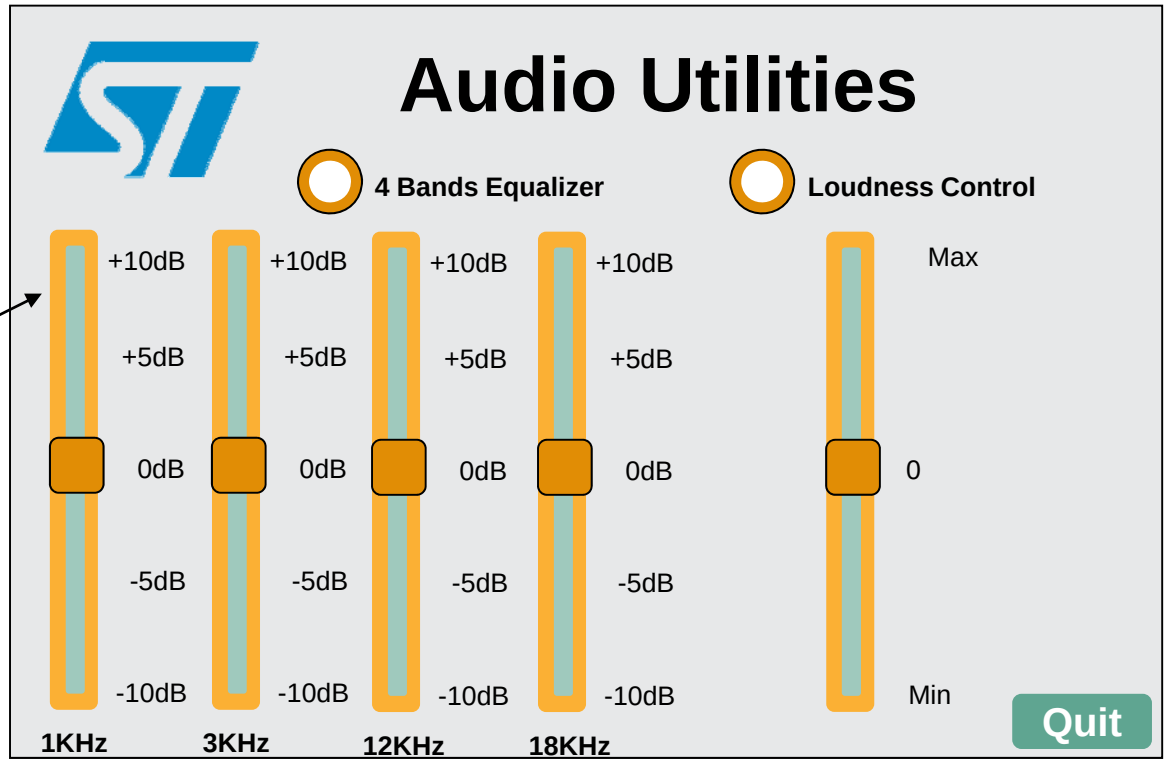
Fast Forward/Backward

Browser

Repeat

Back to Main Window

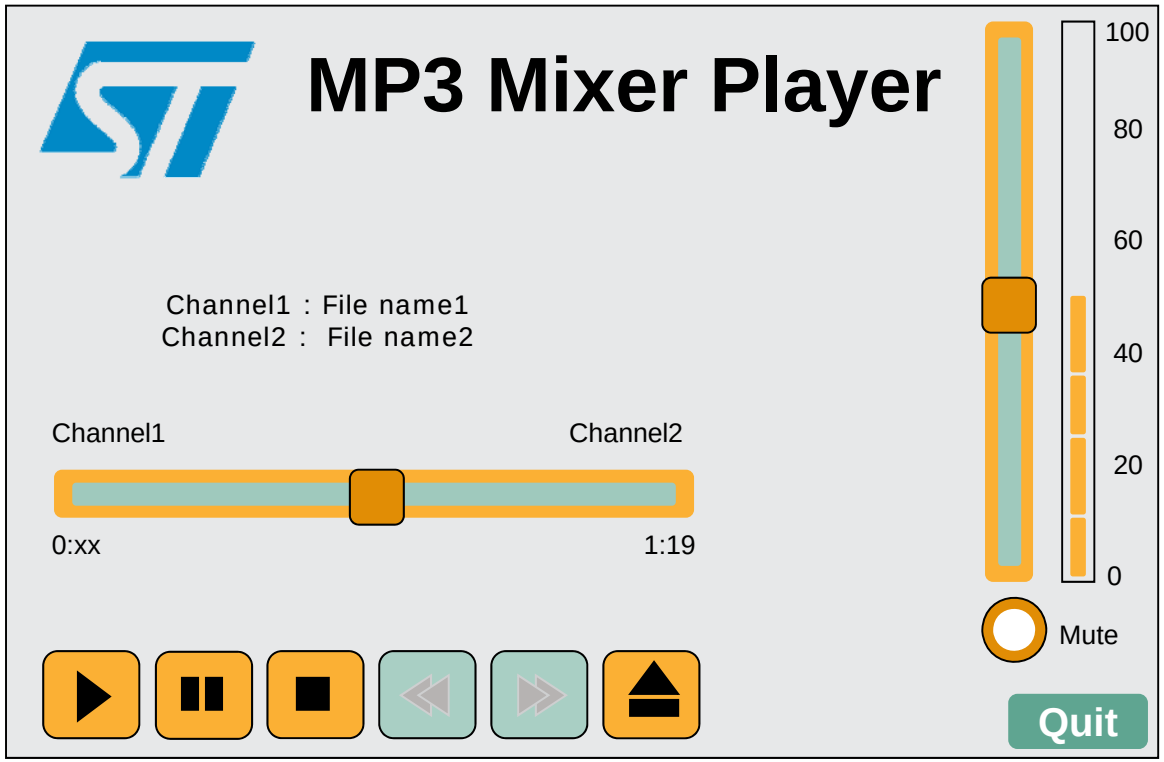
Audio Utilities (wav,mp3,wma)



Run-time Utilities
While playing

***Either* Loudness Control *Or* 3 to 5 bands Equalizers**

Mixer (Play & Mix two MP3 decoders)



Mixer Control

Volume Control
Using Software Mixer

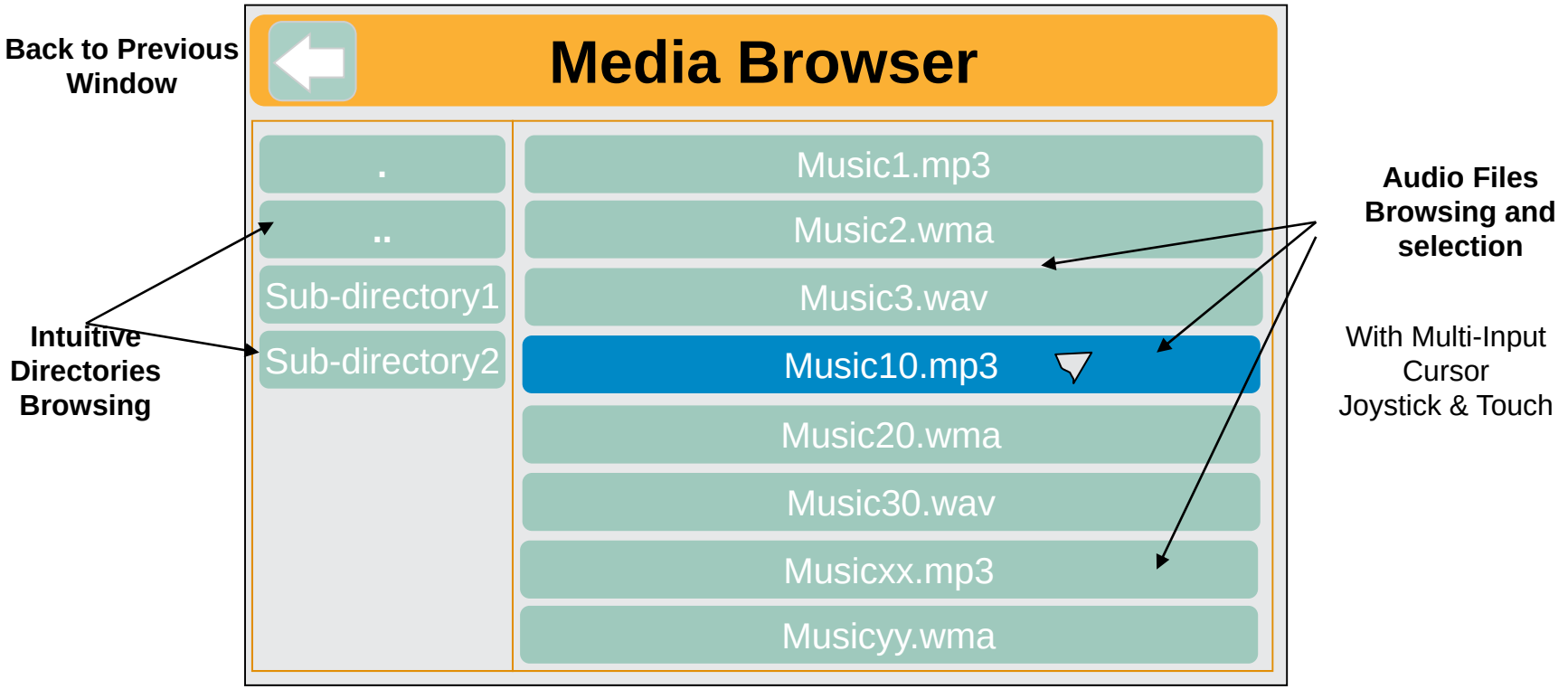
Play

Pause

Stop

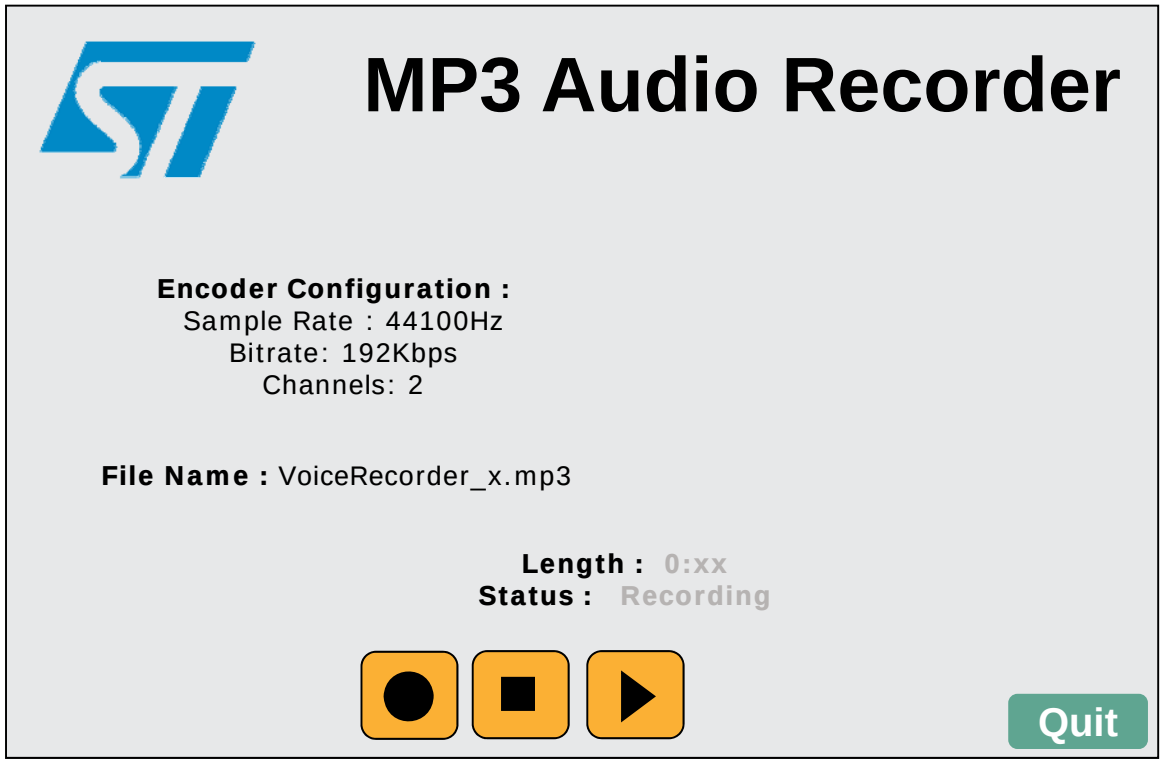
Browser

Media Browser



Browsing while Playing supported for best user Experience

MP3 Audio Encoder (Vocoder)



Thank You !