Sync. Signal Generator for Camera

Description

The CXD1030M is a sync. signal generator for video cameras.

Features

- Adapts to NTSC or PAL by switching mode
- Low power consumption
  (Standard NTSC: 25 mW; PAL: 30 mW)
- Built-in phase comparator and inverter for active filter (separate power supply for the filter inverter)
- External sync.

Function

Sync. signal generator

Structure

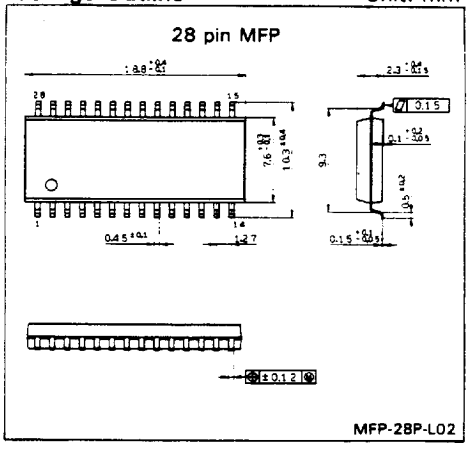
Silicon gate CMOS IC

Application

Video • Camera

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta = 25°C)

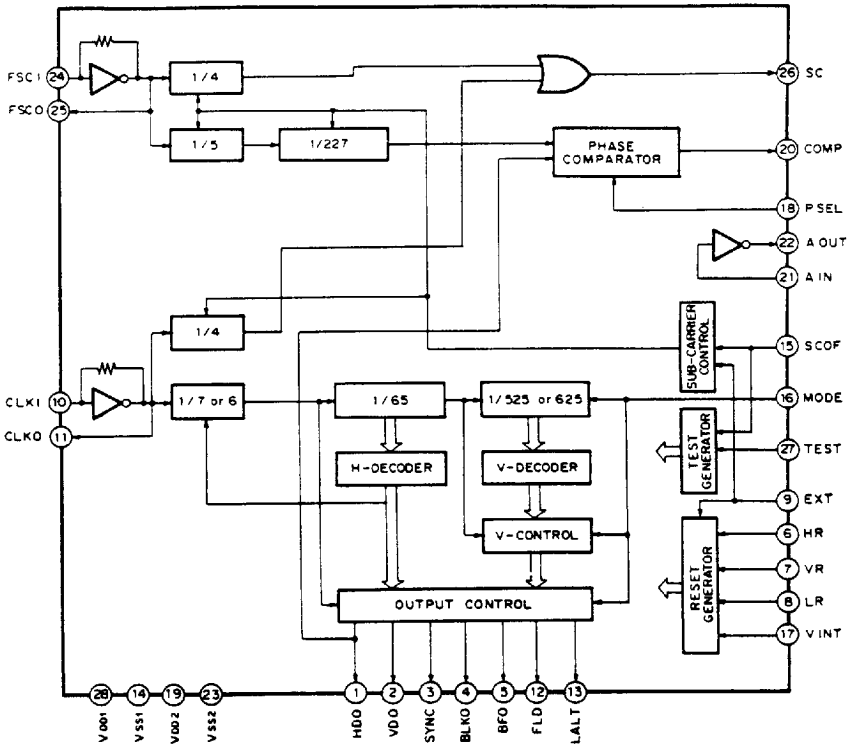
• Supply voltage	V_{DD}	V_{SS}* − 0.3 to 7.0	V
• Input voltage	V_I	V_{SS}* − 0.3 to V_{DD} + 0.3	V
• Output voltage	V_O	V_{SS}* − 0.3 to V_{DD} + 0.3	V
• Operating temperature	T_{opr}	− 20 to + 75	°C
• Storage temperature	T_{stg}	− 55 to + 150	°C

* V_{SS} = 0V

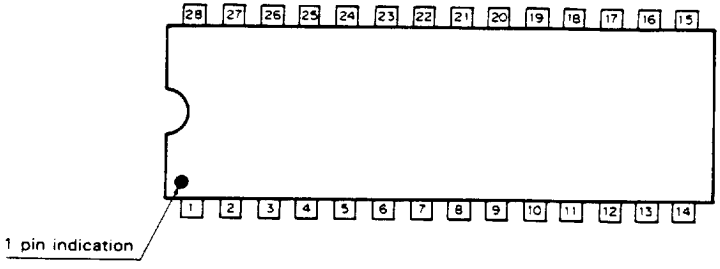
Recommended Operating Conditions

• Supply voltage	V_{DD}	4.50 to 5.50	V
• Operating temperature	T_{opr}	− 20 to + 75	°C

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	HDO	O	Horizontal drive pulse
2	VDO	O	Vertical drive pulse
3	SYNC	O	Complex synchronized pulse
4	BLKO	O	Complex branking pulse
5	BFO	O	Burst flug pulse
6	HR	I	H reset input
7	VR	I	V reset input
8	LR	I	LALT reset input
9	EXT	I	Internal/external mode switching $\overline{\text{INT}}$/EXT
10	CLKI	I	Clock input (NTSC: 14.31818 MHz, PAL: 14.1875 MHz)
11	CLKO	O	Clock output
12	FLD	O	Field pulse
13	LALT	O	Line alternate pulse
14	V_{SS1}	–	GND
15	SCOF	I	Sub carrier suppress input L: OFF
16	MODE	I	NTSC/PAL mode switching $\overline{\text{NTSC}}$/PAL
17	VINT	I	Initialize input
18	PSEL	I	Phase comparator polarity switching
19	V_{DD2}	–	Inverter +5V for filter
20	COMP	O	Phase comparator output
21	AIN	I	Inverter input for filter
22	AOUT	O	Inverter output for filter
23	V_{SS2}	–	Inverter GND for filter
24	FSCI	I	$4f_{SC}$ clock input
25	FSCO	O	$4f_{SC}$ clock output
26	SC	O	Sub carrier output
27	TEST	I	Test input (L normal)
28	V_{DD1}	–	+5V

Electrical Characteristics

DC characteristics

$V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_{opr} = -20$ to $+75°C$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current		I_{DD}	Test circuit (2)		2.0		mA
		I_{DDS}	Static state*1	0		0.1	μA
Output voltage I*2	H level	V_{OH}	$I_{OH} = -1.0$ mA	$V_{DD}-0.5$		V_{DD}	V
	L level	V_{OL}	$I_{OL} = 1.0$ mA	V_{SS}		0.4	V
Output voltage II*3	H level	V_{OH}	$I_{OH} = -0.5$ mA	$V_{DD}-0.5$		V_{DD}	V
	L level	V_{OL}	$I_{OL} = 0.5$ mA	V_{SS}		0.4	V
Input voltage	H level	V_{IH}		$0.7V_{DD}$			V
	L level	V_{IL}				$0.3V_{DD}$	V
Input leak current		I_{LI}	V_I = 0V to V_{DD}	−25		25	μA
Input leak current*4		I_{LZ}		−40		40	μA

Note) *1 $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$
*2 Output pins except "AOUT"
*3 "AOUT" pin
*4 Three state pin

I/O Capacitance

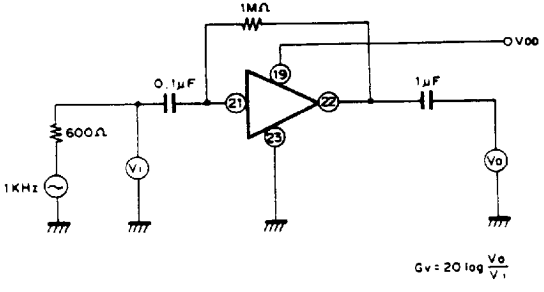
Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			12	pF
Output pin	C_{OUT}			12	pF

Test condition: $V_{DD} = V_I = 0V$, $f_M = 1$ MHz

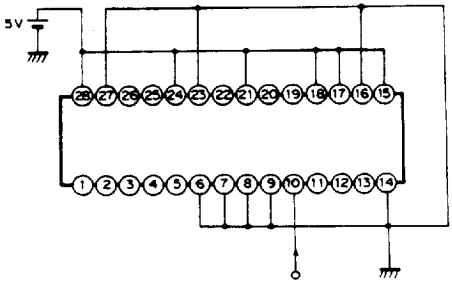
Filter amplifier characteristics

Voltage gain Gv 23dB (Typ.)

Test circuit (1)



Test circuit (2)



Description of Function

1. Generation of various sync. signals (See the Timing Chart.)
   Various sync. signals are generated from clocks.

- Clock frequencies
  NTSC: 910 fH (14.31818 MHz)
  PAL : 908 fH (14.1875 MHz)
  4 fSC (17.734475 MHz)

2. PAL 4 fSC PLL
   Using 908 fH as the master clock, the 4 fSC is put in phase. Corresponding to an external filter (passive or active), the phase comparator polarity can be switched.

Filter	PSEL	Master (908fH)	4fsc	COMP
Passive	L	Fast	Slow	H
		Slow	Fast	L
Active	H	Fast	Slow	L
		Slow	Fast	H

3. SC (SubCarrier) generation

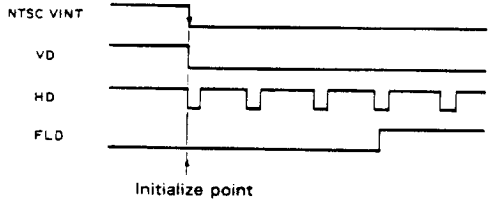
Mode	INT or EXT	SC
NTSC	INT	910fH/4
NTSC	EXT	4fsc/4
PAL	×	4fsc/4

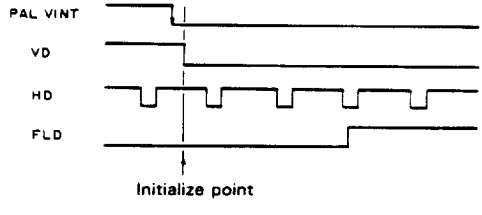
INT : INTERNAL mode (EXT = L)
EXT: EXTERNAL mode (EXT = H)

Unused counters are stopped in any of the mode.
When SC is not required, any counters on SC are stopped and SC is not output by SCOF being set to L.

4. Initialization and Reset
   In the INT mode, the circuit is initialized with the fall of VINT. At this time, the H reset, V reset, and LALT reset are not accepted. In the EXT mode, VINT is not accepted but the H reset, V reset, and LALT reset are accepted.

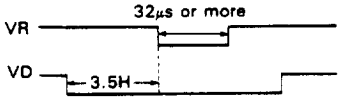
- Initialization (VINT)
  When EXT is L, the fall of VINT is detected and operation is started by the circuit being initialized at the VD fall position immediately prior to field I. (The initialization is completed within 100 ns after the fall is detected.)



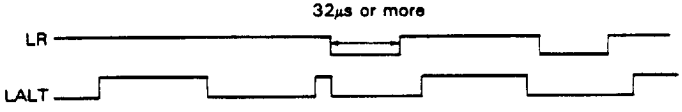


- H reset (HR)
  A reset is executed with the first fall but no reset will be done as long as the subsequent edges do not deviate by more than two clocks (0.98 μs).
  The minimum reset pulse width is 0.98 μs.
  HD is reset 2.94 to 3.43 μs in advance of HR input.

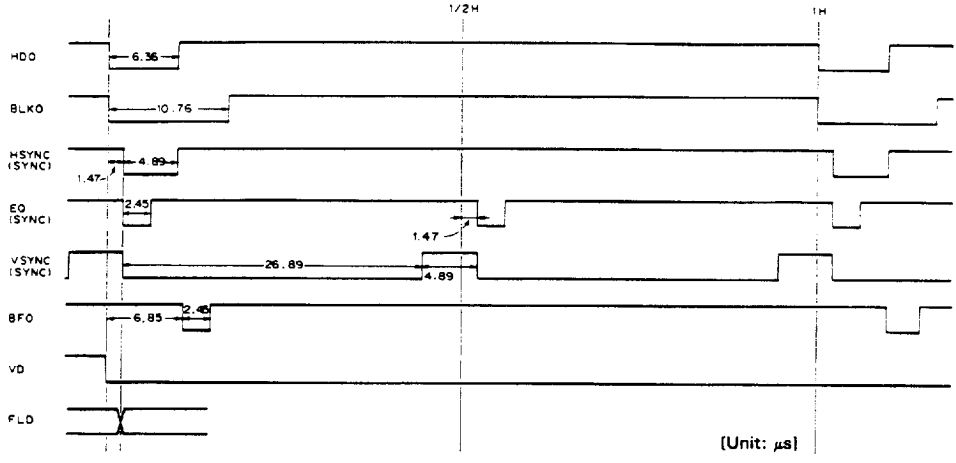
- V reset (VR)
  VD is reset 3.5H in advance of VR input.
  The minimum reset pulse width is 32 μs.



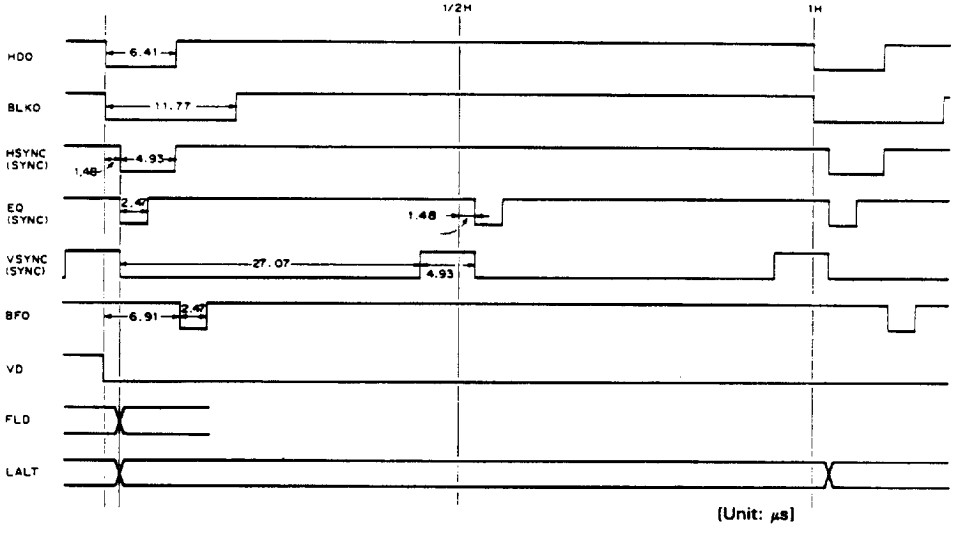
- LALT reset (LR)
  LALT is reset in the same phase as the LR input.
  The minimum reset pulse width is 32 μs.



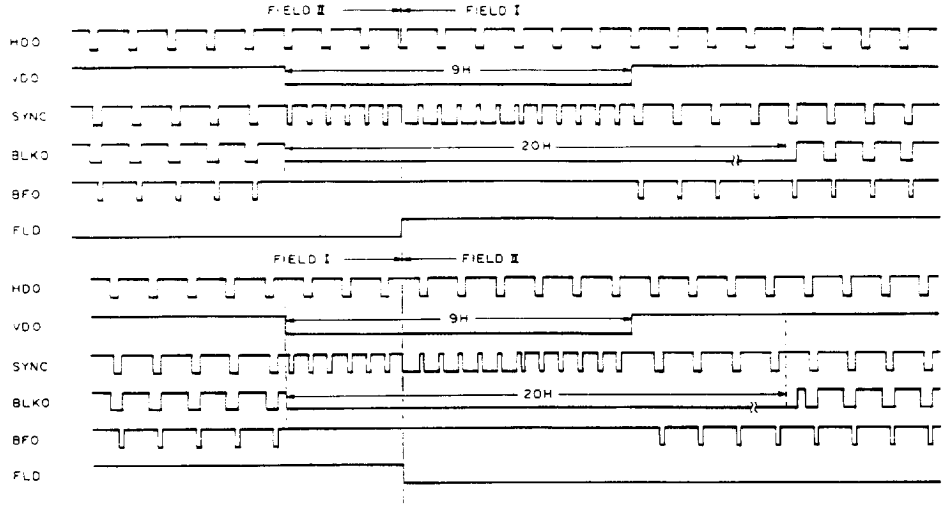
Timing Chart H (NTSC)



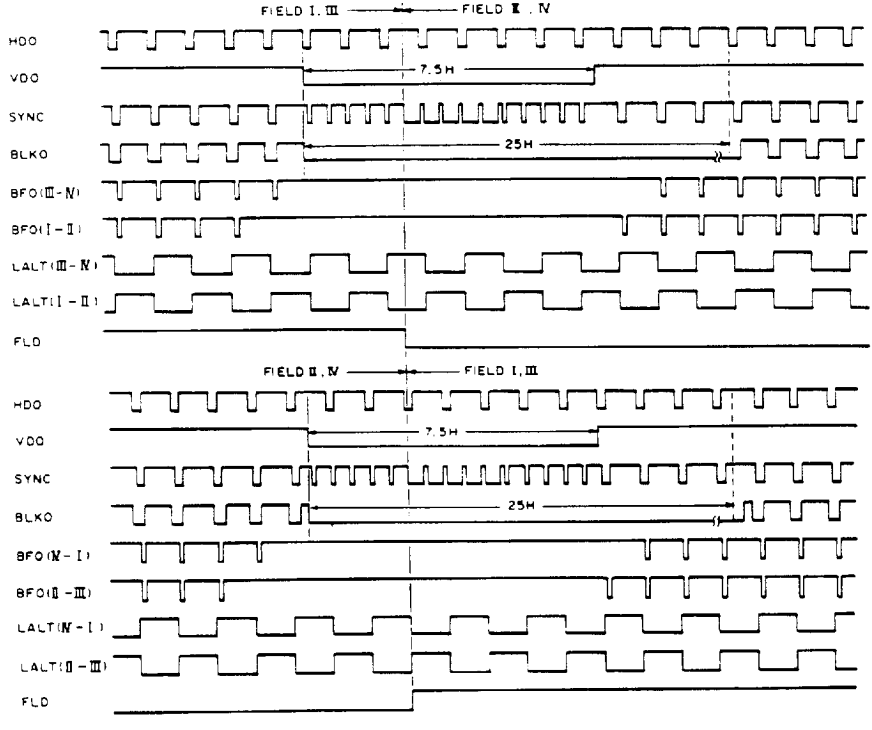
Timing Chart H (PAL)



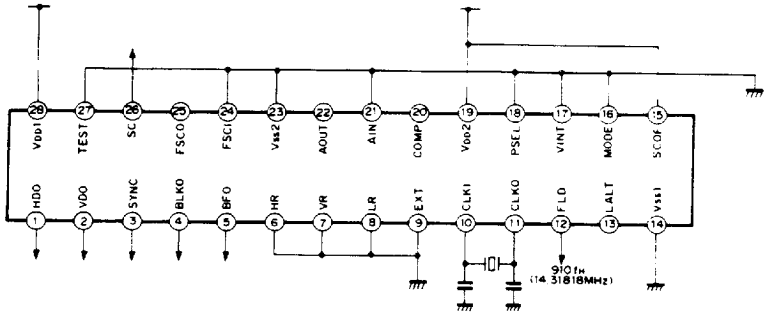
Timing Chart V (NTSC)



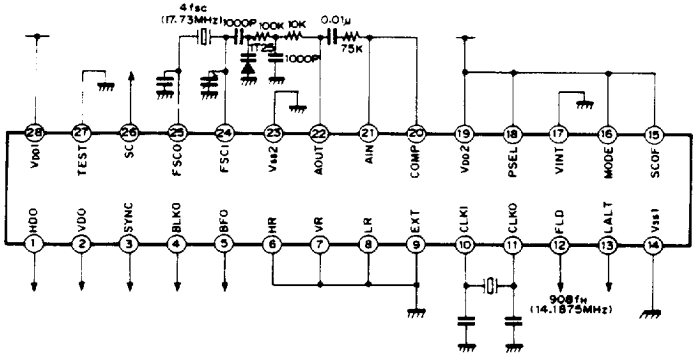
Timing Chart V (PAL)



Application Circuits
NTSC (Internal mode)



PAL (Filter configuration 1, Internal mode)



PAL (Filter configuration 2, Internal mode)