CCD Camera Scanning System Timing Signal Generator

Description

CXD1035BQ is a CMOS type LSI developed for use with the scanning system of both ICX022AK (NTSC) and ICX024AK (PAL).

This IC is employed in conjunction with either CXD1030M or CXD1158M (synchronized signal generator).

Features

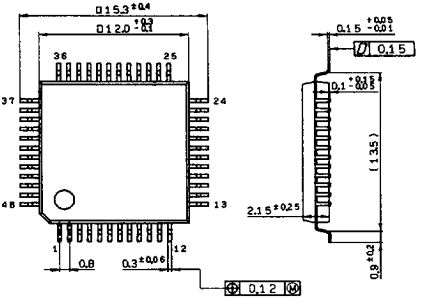
- Generates drive pulses for imagers (ICX022AK, ICX024AK).
- Generates signal processing pulse for color cameras.
- Switchover of NTSC/PAL modes is possible.
- Blemish compensation is possible (through usage of external ROM).

Structure

Silicon gate CMOS IC

Package Outline Unit: mm

48 pin QFP (Plastic)



QFP-48P-L022

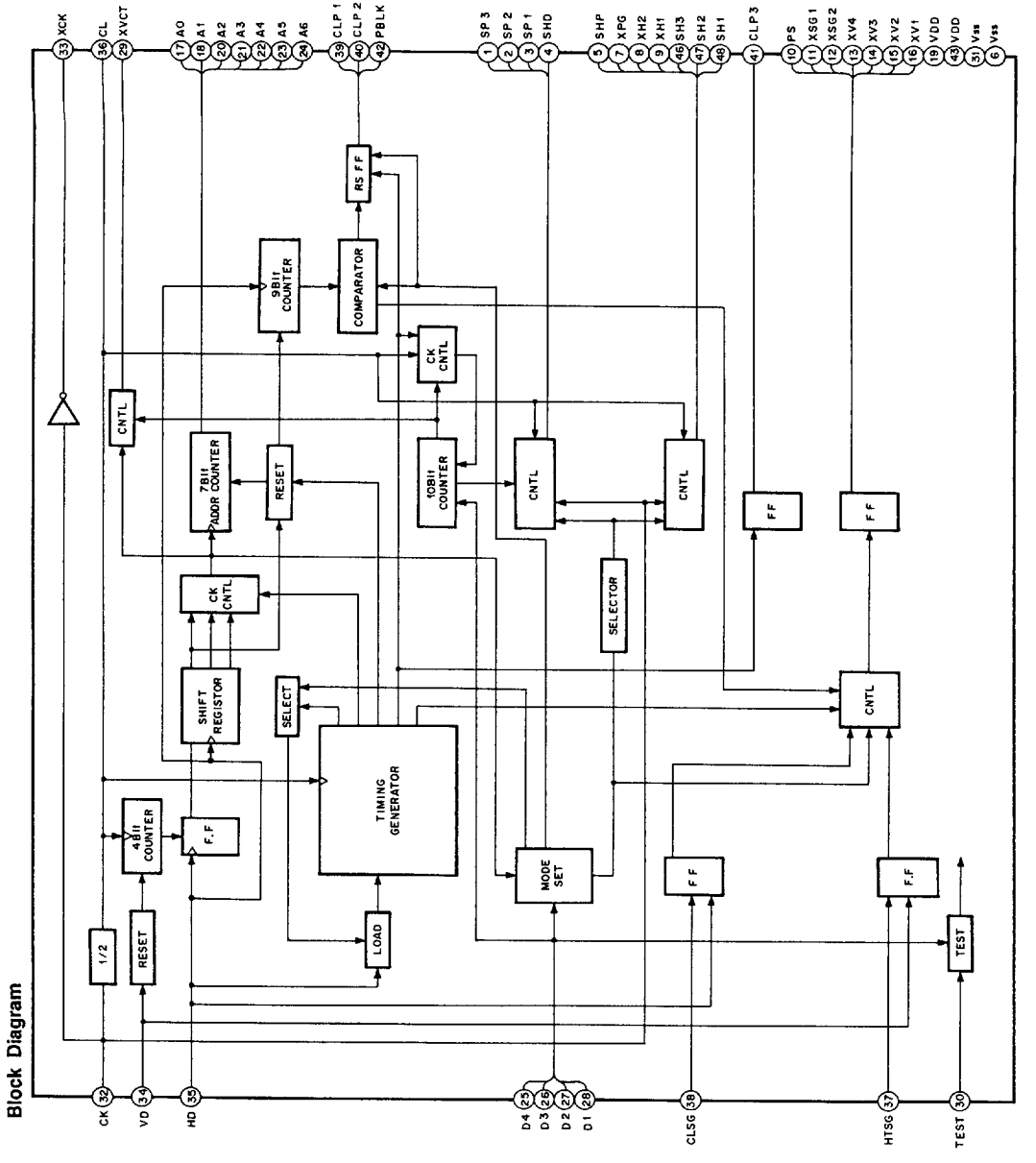
Absolute Maximum Ratings (Ta=25°C, Vss=0V)

• Supply voltage	V_{DD}	Vss −0.5	to	6.0	V
• Input voltage	V_I	Vss −0.5	to	V_{DD}+0.5	V
• Output voltage	V_O	Vss −0.5	to	V_{DD}+0.5	V
• Operating temperature	Topr	−25	to	+85	°C
• Storage temperature	Tstg	−40	to	+125	°C
• Allowable power dissipation	P_D		500		mW

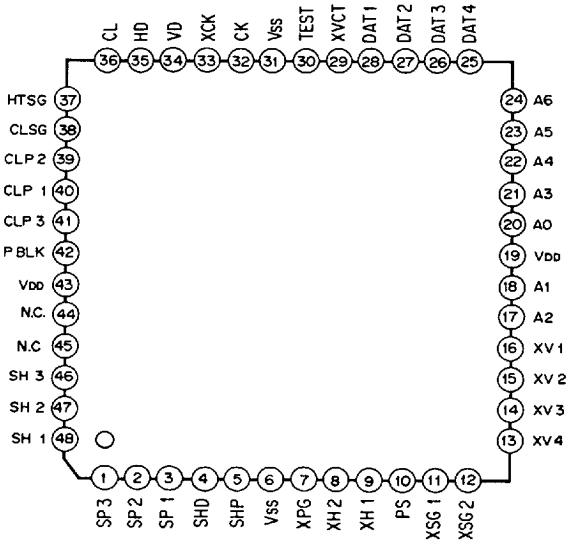
Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75	to	5.25	V
• Operating temperature	Topr	−20	to	+75	°C

Block Diagram



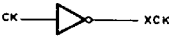
Pin Configuration (Top View)



Pin Name

No.	I/O	Symbol	No.	I/O	Symbol	No.	I/O	Symbol	No.	I/O	Symbol
1	O	SP3	13	O	XV4	25	I	DAT4	37	I	HTSG
2	O	SP2	14	O	XV3	26	I	DAT3	38	I	CLSG
3	O	SP1	15	O	XV2	27	I	DAT2	39	O	CLP2
4	O	SHD	16	O	XV1	28	I	DAT1	40	O	CLP1
5	O	SHP	17	O	A2	29	O	XVCT	41	O	CLP3
6	–	Vss	18	O	A1	30	I	TEST	42	O	PBLK
7	O	XPG	19	–	VDD	31	–	Vss	43	–	VDD
8	O	XH2	20	O	A0	32	I	CK	44	–	N.C.
9	O	XH1	21	O	A3	33	O	XCK	45	–	N.C.
10	O	PS	22	O	A4	34	I	VD	46	O	SH3
11	O	XSG1	23	O	A5	35	I	HD	47	O	SH2
12	O	XSG2	24	O	A6	36	O	CL	48	O	SH1

Pin Description

Symbol	I/O	Description
XV1 to XV4	O	Drive pulses for the imagers (ICX022, ICX024) through CCD drivers.
XSG1, 2	O	
XPG	O	
XH1, 2	O	
A0 to A6	O	Address output for external ROM. A6 is MSB.
D4 to D1	I	External ROM data input pin.
XVCT	O	ROM (MB7144) power supply switching pulse.
TEST	I	Test pin. Normally GND.
CK	I	Clock input. NTSC : 28.6364 MHz PAL : 28.3750 MHz
XCK	O	CK inversion output 
VD, HD	I	Synchronizing signal input. Latched by falling edge of CL (Pin 36).
CL	O	Clock output for synchronized signal generator. Half CK's frequency.
PBLK	O	Horizontal and vertical effective area of CCD imager output. Used for pre-blanking.
PS	O	Power save for V driver IC.
CLP1, 2, 3	O	Clamping pulse.
SH1, 2, 3	O	Sampling pulse for signal processor.
SP1, 2, 3	O	Sampling pulse for color separation.
SHD	O	Sampling pulse for imager output signal.
SHP	O	Sampling pulse for pre-charge level.
HTSG, CLSG	I	Test pin. Nomrally GND.
Vss	I	Ground pin.
V_{DD}	I	+5V power supply pin.

Electrical Characteristics

DC characteristics

V_{DD}=5V±5%, Vss=0V, Topr=−20 to +75°C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current		I_{DDS}	Static state*	0		0.1	mA
Input voltage	H level	V_{OH}	I_{OH} = −0.4 mA	4.2		V_{DD}	V
	L level	V_{OL}	I_{OL} = 3.2 mA	Vss		0.4	V
Output voltage	H level	V_{IH}		2.4			V
	L level	V_{IL}				0.8	V
Input leakage current		I_{LI}	V_I = 0V to V_{DD}	−10		+10	μA

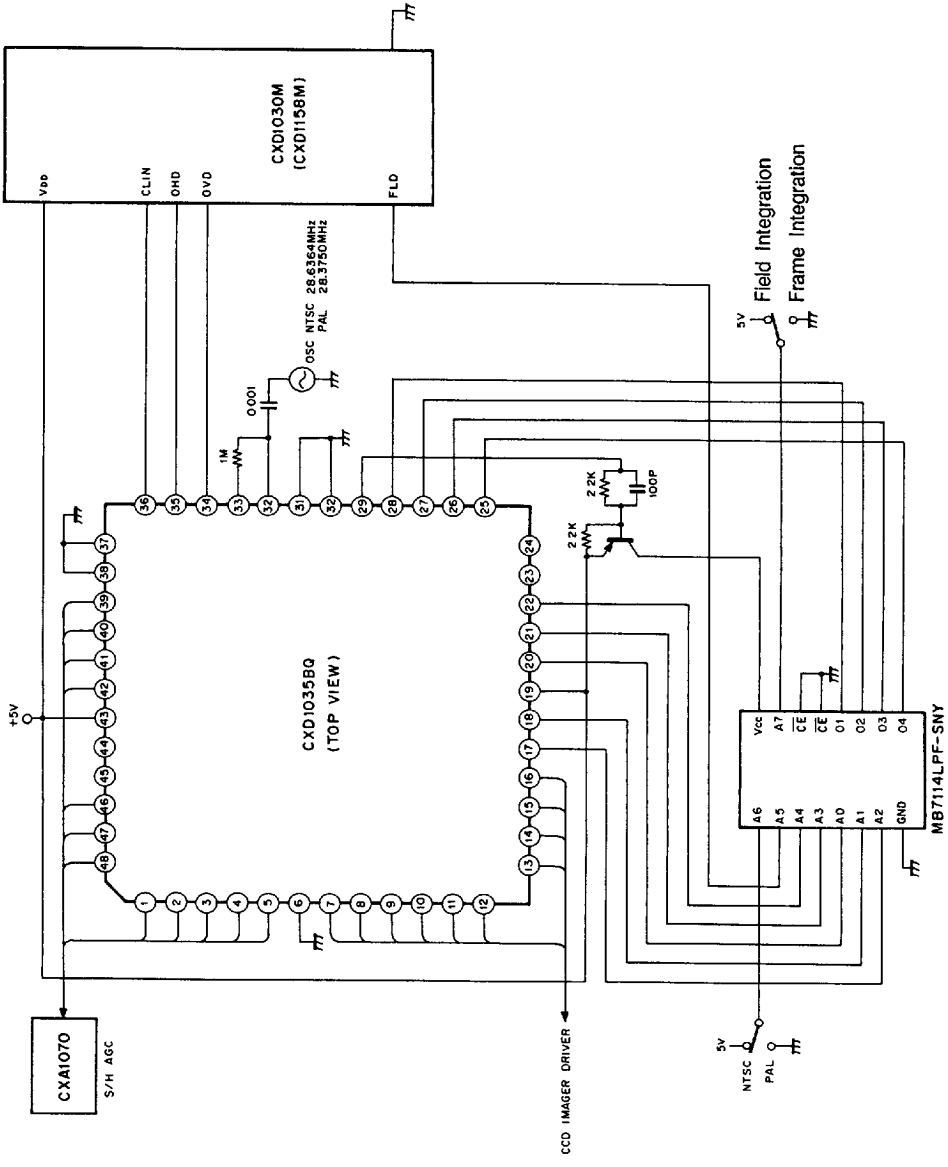
*** Note)** V_{IH} = V_{DD}, V_{IL} = Vss

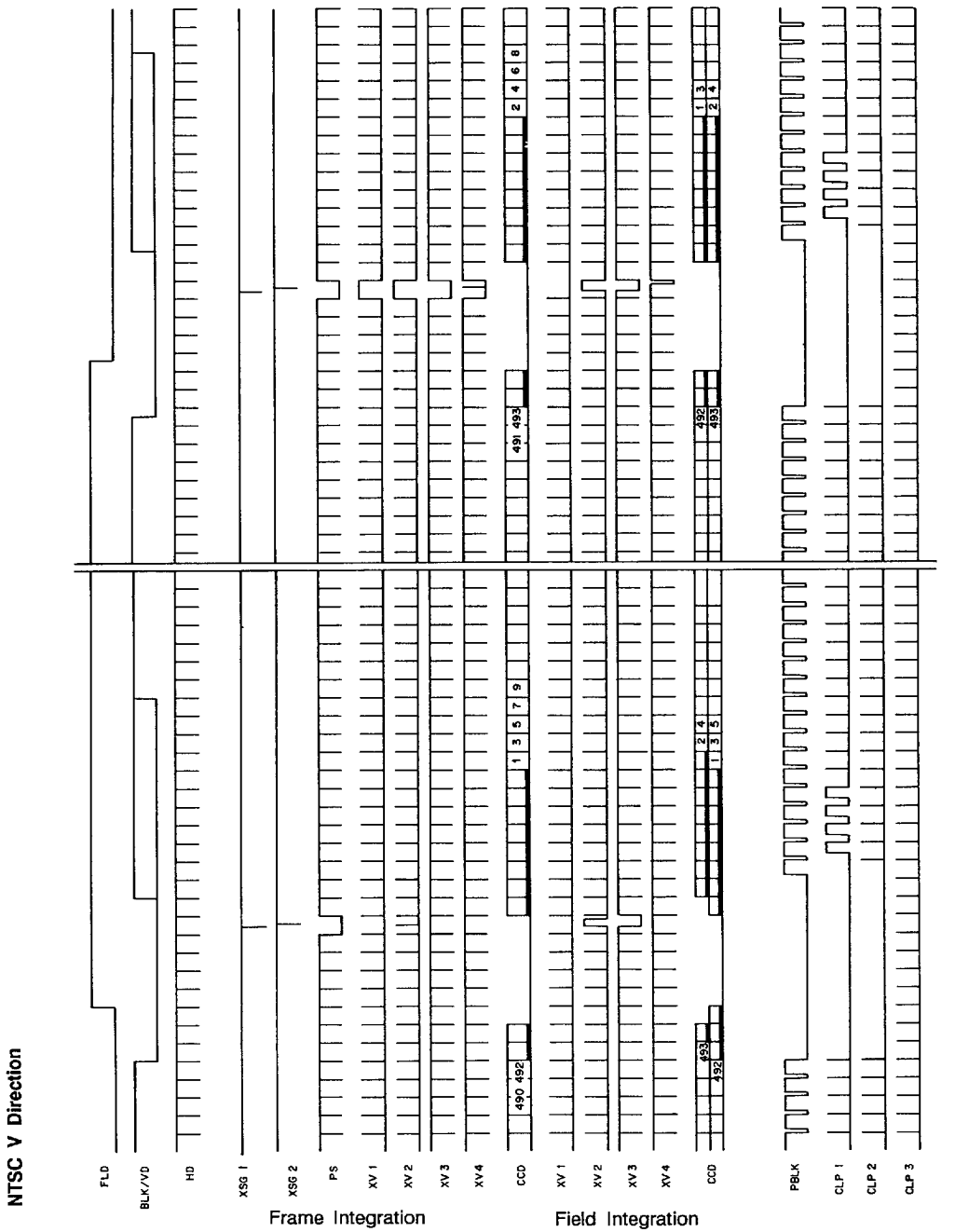
I/O characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
Output pin	C_{OUT}			9	pF

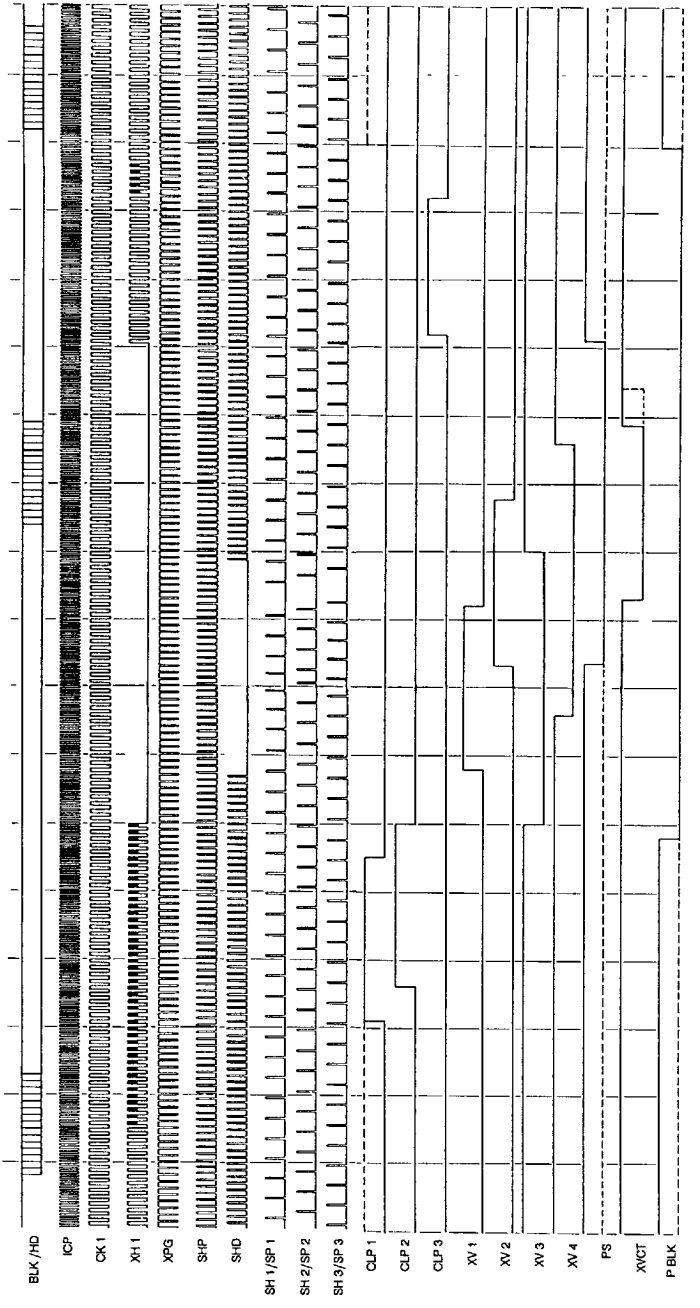
Test condition: V_{DD}=V_I=0V, f_M=1MHz

Application Circuit

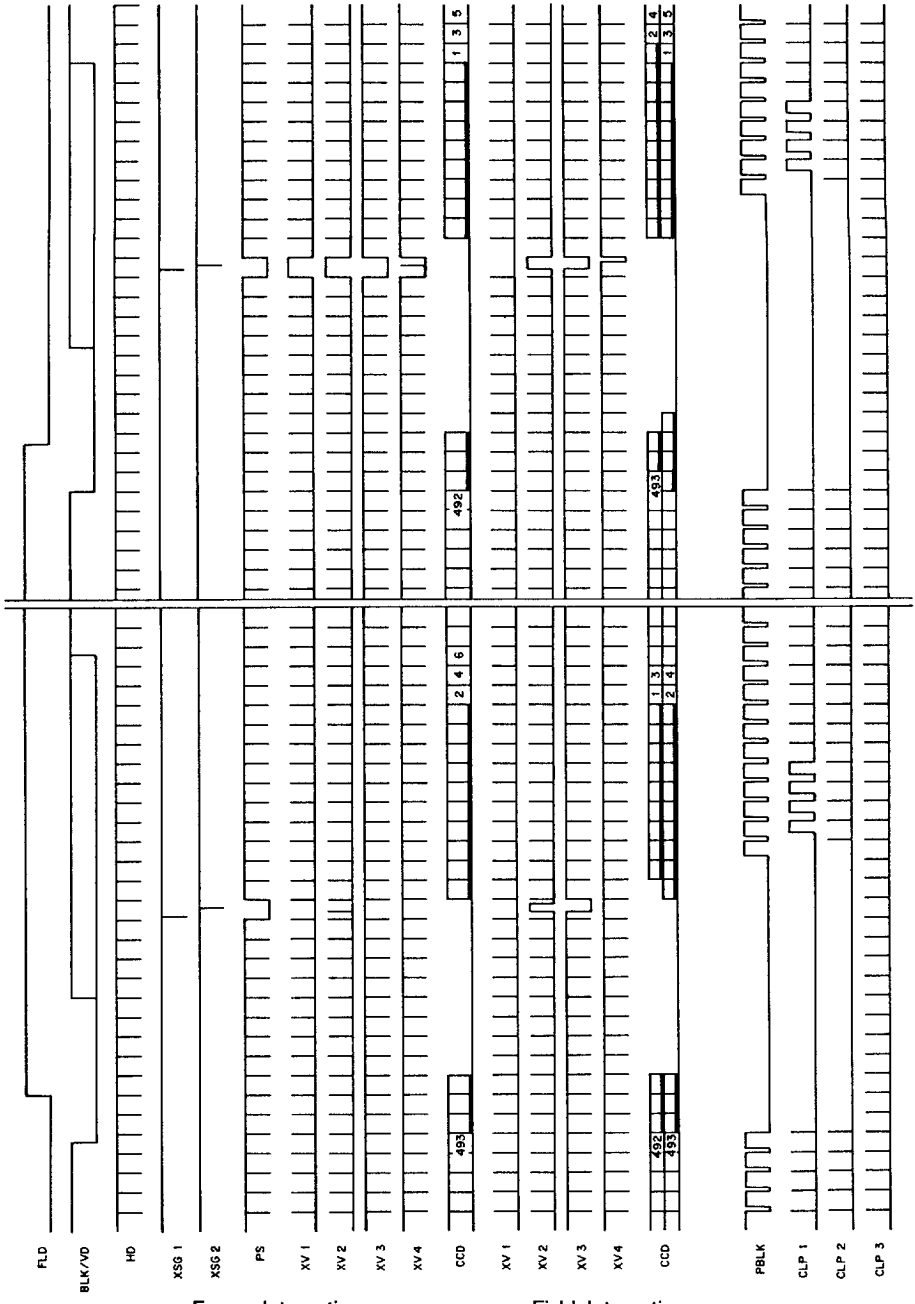



NTSC V Direction
FLD
BLK/VD
HD
XSG 1
XSG 2
PS
XV 1
XV 2
XV 3
XV4
CCD
XV 1
XV 2
XV 3
XV 4
CCD
PBLK
CLP 1
CLP 2
CLP 3
Frame Integration
Field Integration

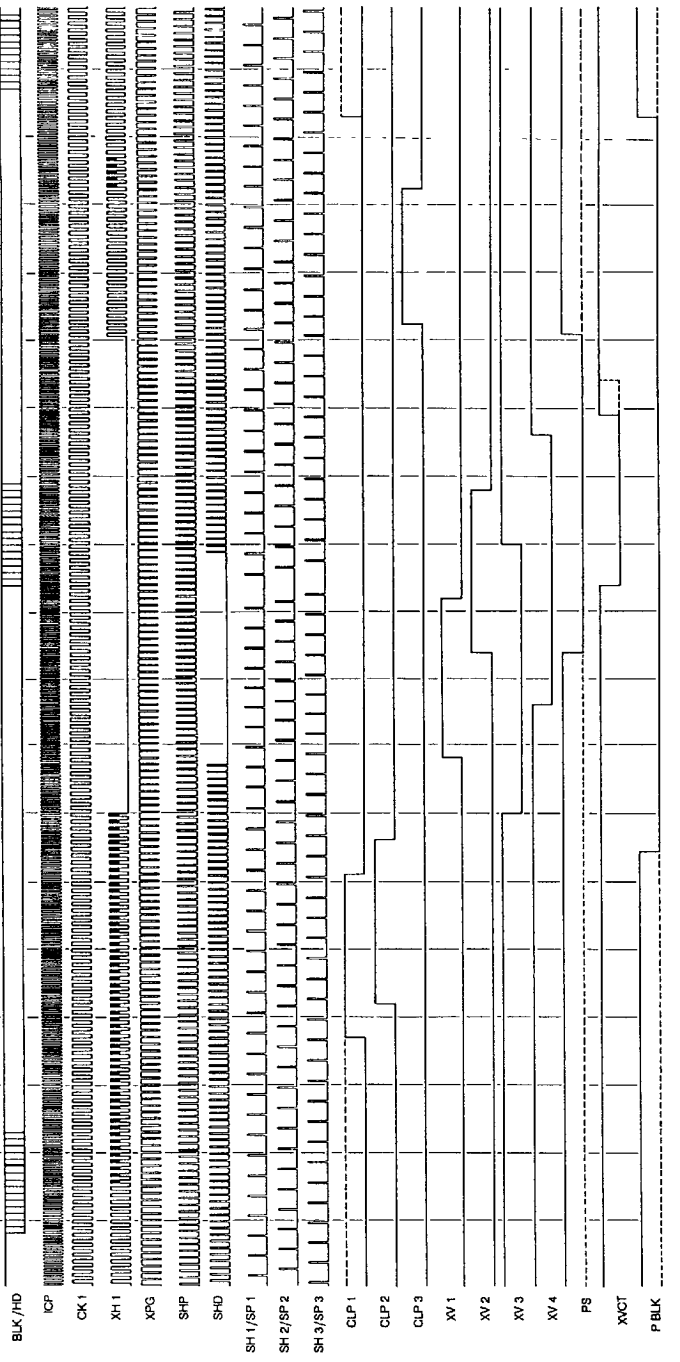
NTSC H Direction



PAL V Direction

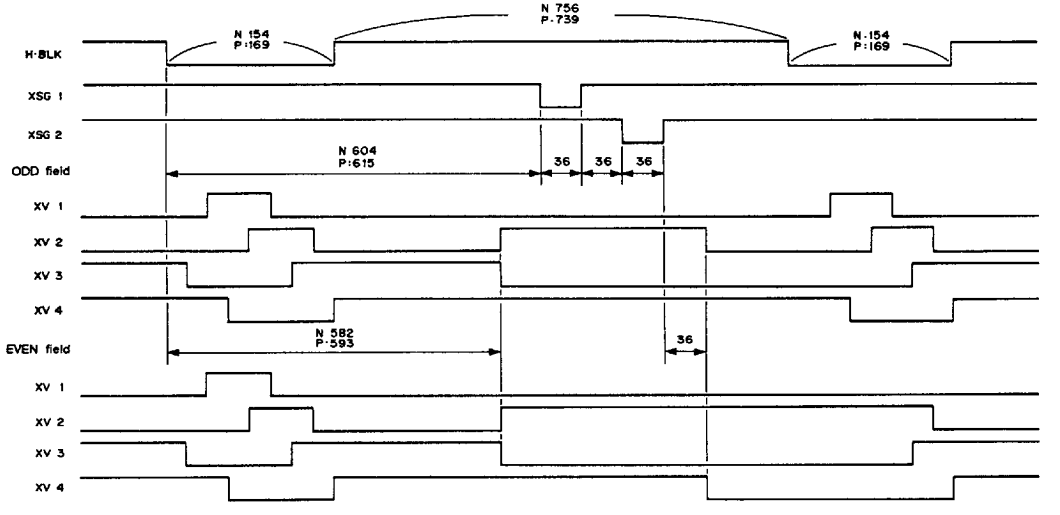


PAL H Direction

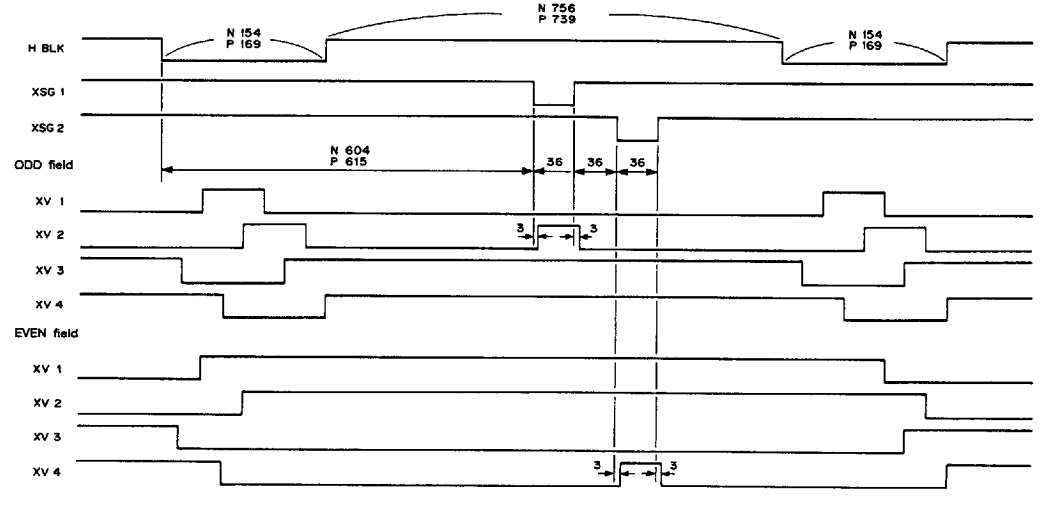


Readout Period

Field Integration mode



Frame Integration mode



Note) Number: Clock (1 clock = 70ns)

N·NTSC
P·PAL

H clock • Signal Processing Pulse Phase