

# Angle Sensor

GMR-Based Angular Sensor

## TLE5012B

## Data Sheet

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Preliminary

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## 1 Product Description

### 1.1 Overview

The TLE5012B is a 360° angle sensor that detects the orientation of a magnetic field. This is achieved by measuring sine and cosine angle components with monolithic integrated **Giant Magneto Resistance (iGMR)** elements.

High precision angle values are achieved over temperature and lifetime using internal autocalibration algorithm.

Data communications are accomplished with a bi-directional SSC Interface that is SPI compatible.

The absolute angle value and other values are transmitted via SSC or via a Pulse-Width-Modulation (PWM) Protocol. Also the sine and cosine raw values can be read out. These raw signals are digitally processed internally to calculate the angle orientation of the magnetic field (magnet).

The TLE5012B is a precalibrated sensor. The calibration parameters are stored in laser fuses. At start-up the values of the fuses are written into Flip-Flops, where these values can be changed by the application specific parameters.

Online diagnostic functions are provided to ensure reliable operation.



Product Type	Marking	Ordering Code	Package
TLE5012B E1000	012B1000	SP000905682	PG-DSO-8
TLE5012B E3005	012B3005	SP000905686	PG-DSO-8
TLE5012B E5000	012B5000	SP000905690	PG-DSO-8
TLE5012B E9000	012B9000	SP000905694	PG-DSO-8



## 1.2 Features

- **Giant Magneto Resistance (GMR)**-based principle
- Integrated magnetic field sensing for angle measurement
- Full calibrated 0 - 360° angle measurement with revolution counter and angle speed measurement
- Two separate highly accurate single bit SD-ADC
- 15 bit representation of absolute angle value on the output (resolution of 0.01°)
- 16 bit representation of sine / cosine values on the interface
- Max. 1.0° angle error over lifetime and temperature with activated auto-calibration
- Bi-directional SSC Interface up to 8Mbit/s
- Supports SIL with diagnostic functions and status information
- Interfaces: SSC, PWM, Incremental Interface (IIF), Hall Switch Mode (HSM), Short PWM Code (SPC)
- 0.25 µm CMOS technology
- Automotive qualified: -40°C to 150°C (Junction Temperature)
- ESD > 4kV (HBM)
- RoHS compliant (Pb-free package)

## 1.3 Application Example

The TLE5012B GMR-based angular sensor is designed for angular position sensing in automotive applications, such as:

- Electrical Commutated Motor (e.g. used in **Electric Power Steering (EPS)**)
- Rotary Switch
- Steering Angle
- General Angular Sensing

## 2 Functional Description

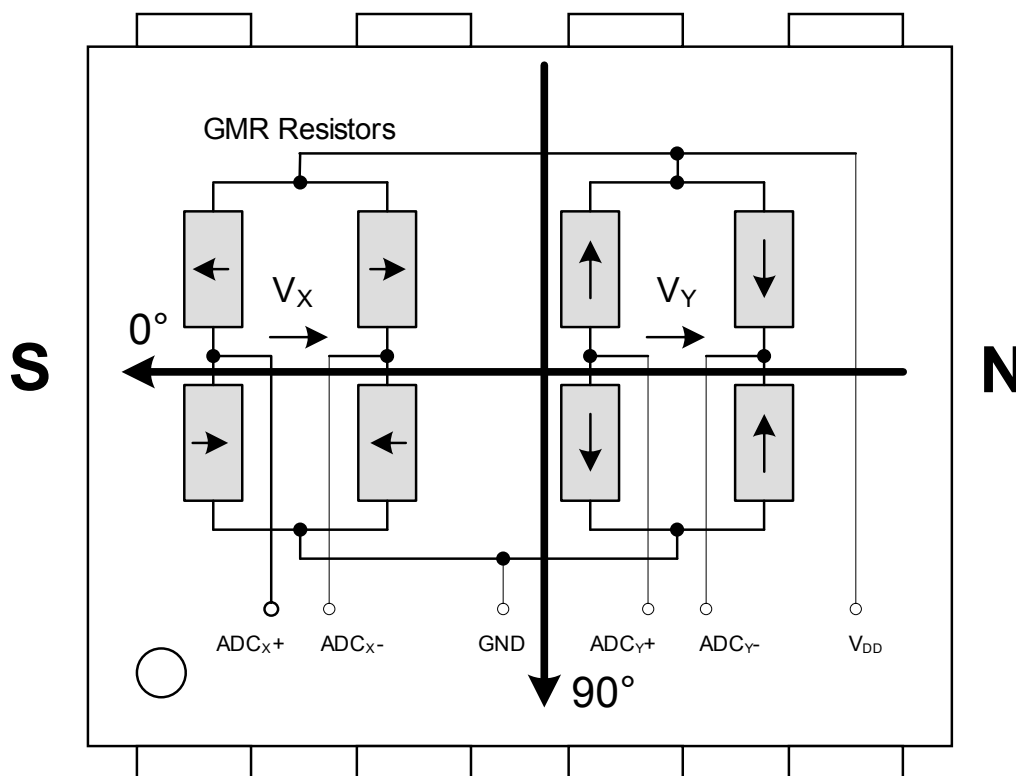
### 2.1 General

The GMR sensor is implemented using vertical integration. This means that the GMR-sensitive areas are integrated above the logic portion of the TLE5012B device. These GMR elements change their resistance depending on the direction of the magnetic field.

Four individual GMR elements are connected to one Wheatstone sensor bridge. These GMR elements sense one of two components of the applied magnetic field:

- X component,  $V_x$  (cosine) or the
- Y component,  $V_y$  (sine)

The advantage of a full-bridge structure is that the amplitude of the GMR signal is doubled and temperature effects cancel out each other.



**Figure 1 Sensitive Bridges of the GMR Sensor**

*Note: In **Figure 1**, the arrows in the resistors represent the magnetic direction which is fixed in the Reference Layer. If the external magnetic field is parallel to the direction of the Reference Layer, the resistance is minimal. If they are anti-parallel, resistance is maximal.*

The output signal of each bridge is only unambiguous over 180° between two maxima. Therefore two bridges are orientated orthogonally to each other to measure 360°.

With the trigonometric function ARCTAN, the true 360° angle value can be calculated, based on the relationship of X and Y signals.

Because only the relative values influence the result, the absolute magnitude of the two signals is of minor importance. Therefore, it is possible to compensate for most external influences on the amplitudes.

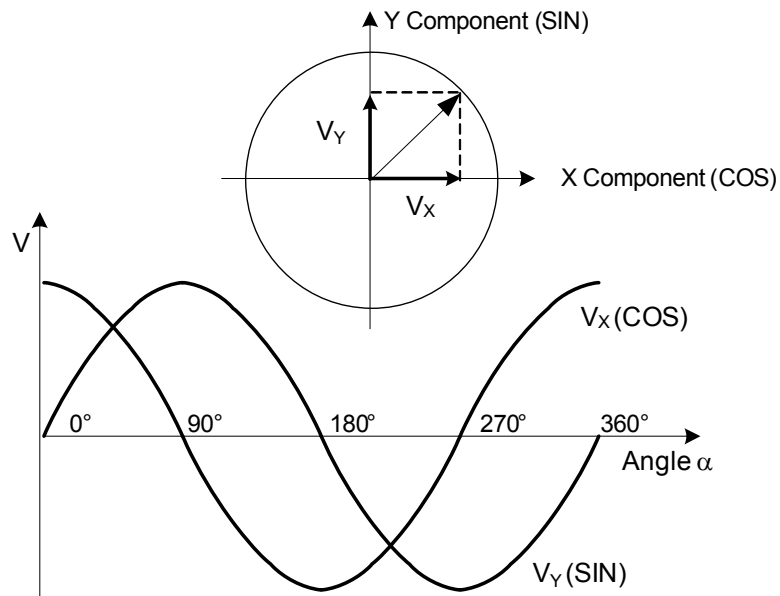


Figure 2 Ideal Output of the GMR Sensor Bridges

## 2.2 Pin Configuration

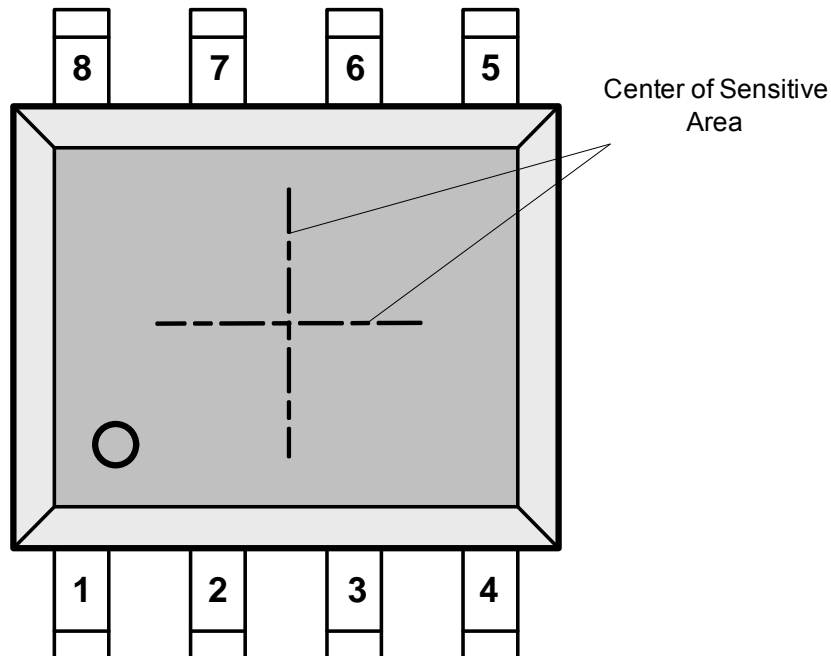


Figure 3 Pin configuration (top view)

## 2.3 Pin Description

Table 1 Pin Description

Pin No.	Symbol	In/Out	Function
1	IFC (CLK / IIF_IDX / HS3)	I/O	Interface C: External Clock / IIF Index / Hall Switch Signal 3
2	SCK	I	SSC Clock
3	CSQ	I	SSC Chip Select
4	DATA	I/O	SSC Data
5	IFA (IIF_A / HS1 / PWM)	O	Interface A: IIF Phase A; Hall Switch Signal 1 or PWM output (depends on external application circuit)
6	V <sub>DD</sub>	-	Supply Voltage
7	GND	-	Ground
8	IFB (IIF_B / HS2)	O	Interface B: IIF Phase B or Hall Switch Signal 2

## 2.4 Block Diagram

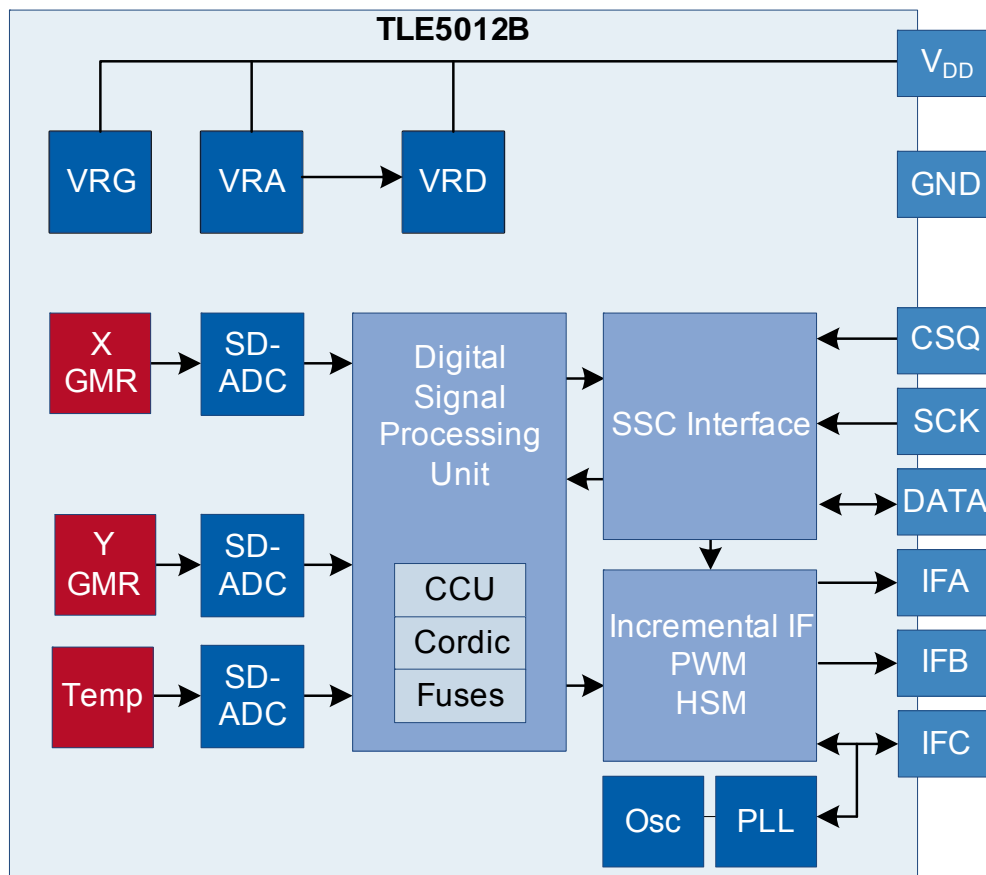


Figure 4 TLE5012B block diagram

## 2.5 Functional Block Description

### 2.5.1 Internal Power Supply

The internal stages of the TLE5012B are supplied with different voltage regulators.

- GMR Voltage Regulator VRG
- Analog Voltage Regulator VRA
- Digital Voltage Regulator VRD (derived from VRA)

These regulators are directly connected to the supply voltage V<sub>DD</sub>.

### 2.5.2 Oscillator and PLL

The internal frequency oscillator feeds the Phase Locked Loop (PLL). Also the external clock (CLK) can be used therefore.

### 2.5.3 SD-ADC

The SD-ADCs transform the analog GMR-voltages and temperature-voltage into the digital domain.

## 2.5.4 Digital Signal Processing Unit

The Digital Signal Processing Unit (DSPU) contains the:

- **C**apture **C**ompare **U**nit (**CCU**), which is used to generate the PWM signal
- **C**oordinate **R**otation **D**igital **C**omputer (**CORDIC**), which contains the trigonometric function for angle calculation
- Fuses, which contain the calibration parameters

## 2.5.5 Interfaces

Different Interfaces can be selected:

- SSC Interface
- PWM
- Incremental Interface
- Hall Switch Mode
- Short PWM Code

## 2.5.6 Safety Features

The TLE5012B offers a multiplicity on safety features to support Safety Integrity Level (SIL). Sensors with this performance are identified by the following logo:



**Figure 5 PRO-SIL™ Logo**

Safety features are:

- Test vectors switchable to ADC- input
- Inversion or combination of filter input streams
- Data transmission check via 8bit **C**yclic **R**edundancy **C**heck (**CRC**)
- Self test routines
- Two independent active interfaces possible
- Overvoltage and undervoltage detection

### Disclaimer

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The PRO-SIL™ Trademark designates Infineon products which contain SIL Supporting Features.

SIL Supporting Features are intended to support the overall System Design to reach the desired SIL (according to IEC61508) or A-SIL (according to ISO26262) level for the Safety System with high efficiency.

SIL respectively A-SIL certification for such a System has to be reached on system level by the System Responsible at an accredited Certification Authority.

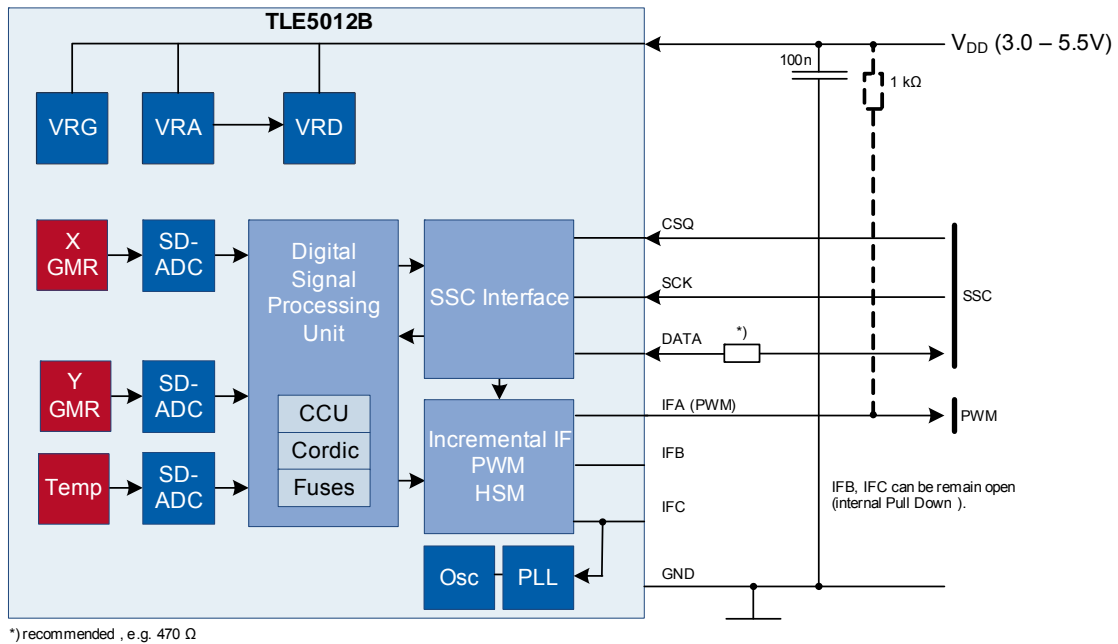
SIL stands for Safety Integrity Level (according to IEC 61508)

A-SIL stands for Automotive-Safety Integrity Level (according to ISO 26262)

### 3 Specification

#### 3.1 Application Circuit

The application circuit in [Figure 6](#), [Figure 7](#), [Figure 8](#) and [Figure 9](#) show the different communication possibilities of TLE5012B.

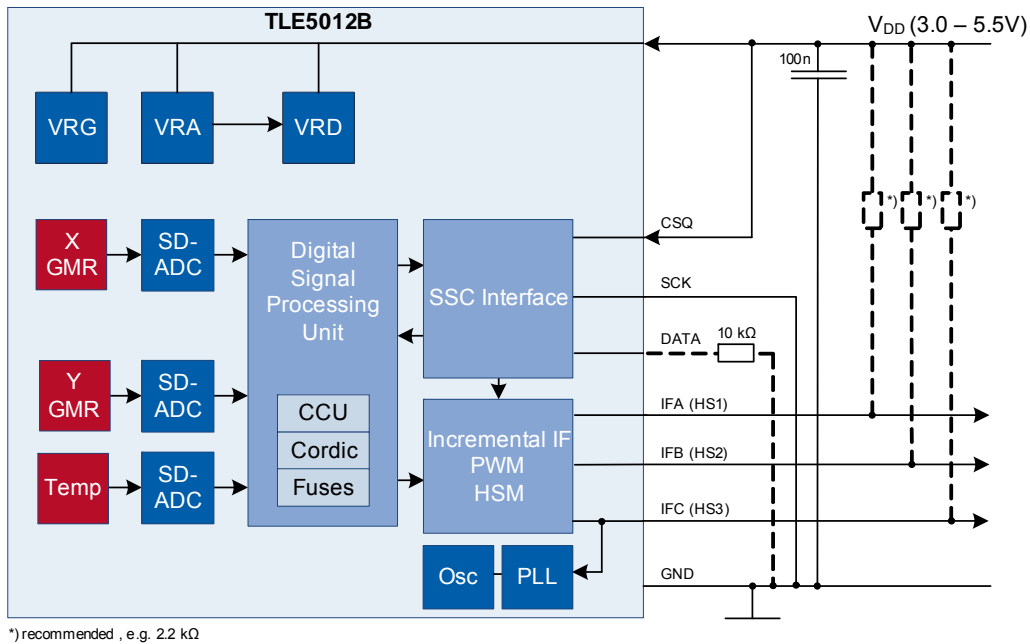


\*) recommended , e.g. 470 Ω

**Figure 6 Application circuit for TLE5012B with SSC and PWM interface (using internal CLK)**

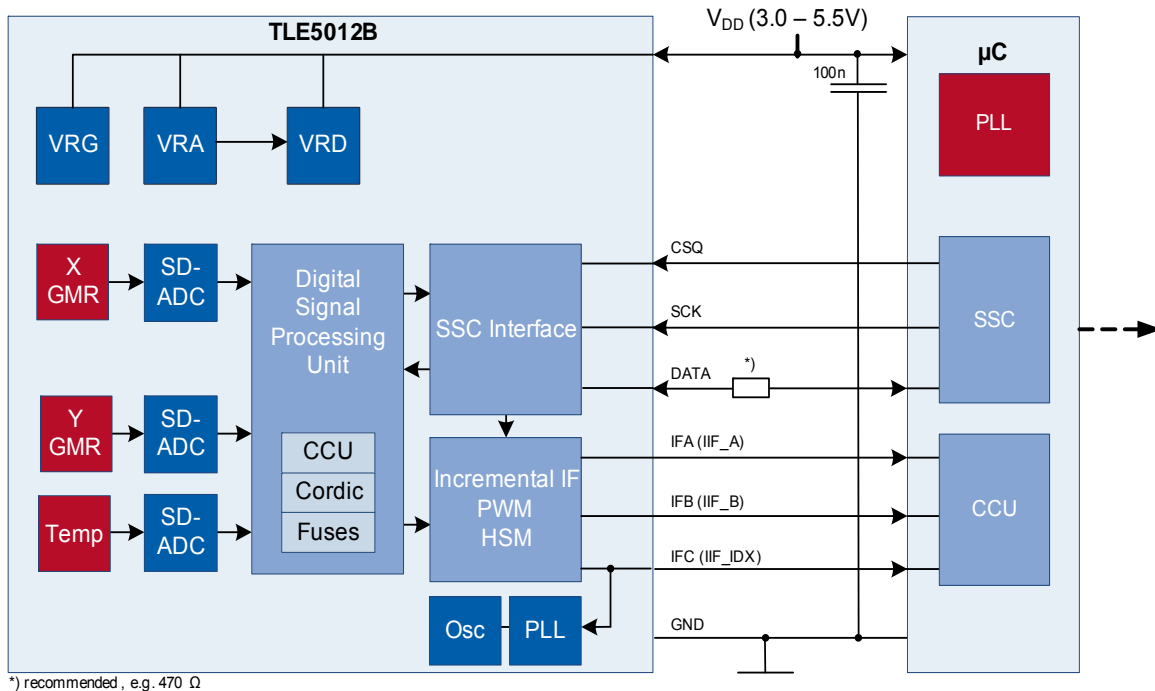
[Figure 6](#) shows a basic block-diagram of the TLE5012B with PWM Interface. Additionally to the PWM the SSC Interface could be used. Within the SSC Interface the PWM mode is selectable between Push-Pull and Open Drain.





**Figure 7 Application circuit for TLE5012B with HS Mode (using internal CLK)**

Figure 7 shows a basic block-diagram of the TLE5012B with HS Mode. Additionally to the HSM the SSC Interface could be used in parallel. Within the SSC- Interface the HS Mode is selectable between Push-Pull and Open Drain.



**Figure 8 Application circuit for TLE5012B with SSC and IIF interface (using external CLK)**

Figure 8 shows a basic block-diagram of an angle sensor system using a TLE5012B and a microcontroller for rotor positioning applications. The depicted Interface-Configuration is needed for High-Speed applications like electrical commutated motor drives. It is possible to connect the TLE5012B to a microcontroller via Incremental Interface and for safety reasons also via SSC-Interface.

The TLE5012B can be configured with PWM only (Figure 9). This is only possible with the TLE5012B-E5000 type.<sup>1)</sup>

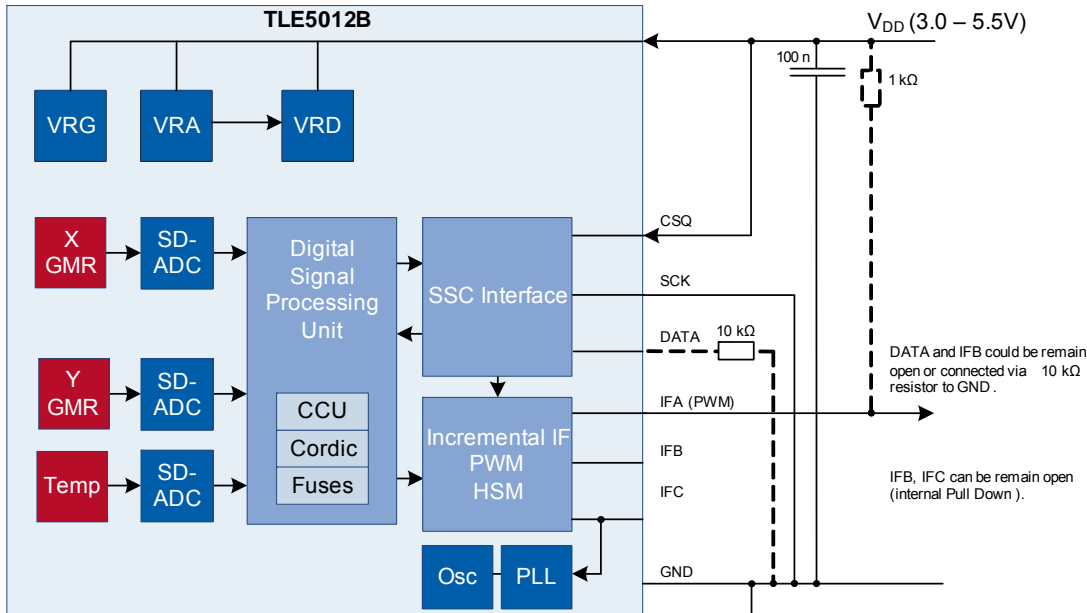


Figure 9 Application circuit for TLE5012B with only PWM interface (using internal CLK)

The TLE5012B can be configured with SPC only (Figure 9). This is only possible with the TLE5012B-E9000 type.<sup>1)</sup>

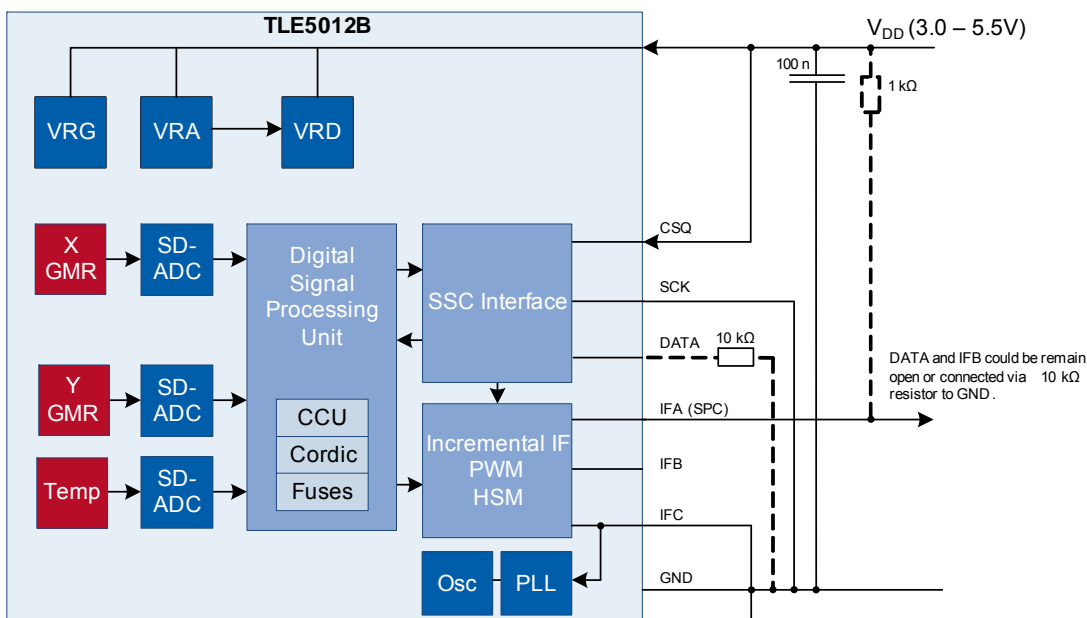


Figure 10 Application circuit for TLE5012B with only SPC interface (S\_NR = 00)

1) For more information get in contact with Infineon

### 3.2 Absolute Maximum Ratings

**Table 2 Absolute maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage on V <sub>DD</sub> pin with respect to ground (V <sub>SS</sub> )	V <sub>DD</sub>	-0.5	-	6.5	V	Max 40 h/Lifetime
Voltage on any pin with respect to ground (V <sub>SS</sub> )	V <sub>IN</sub>	-0.5	-	6.5	V	Additionally V <sub>DD</sub> + 0.5 V may not be exceeded
Junction temperature	T <sub>J</sub>	-40	-	150	°C	
		-	-	150	°C	For 1000h not additive
Magnetic field induction	B	-	-	200	mT	Max. 5 min @ T <sub>A</sub> = 25°C
		-	-	150	mT	Max. 5 h @ T <sub>A</sub> = 25°C
Storage temperature	T <sub>ST</sub>	-40	-	150	°C	Without magnetic field

**Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.**

### 3.3 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE5012B. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed. **Table 3** is valid for -40°C < T<sub>J</sub> < 150°C unless otherwise noticed.

**Table 3 Operating range**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V <sub>DD</sub>	3.0	5.0	5.5	V	1)
Output current (DATA-Pad)	I <sub>Q</sub>	-	-	-25	mA	PAD_DRV = '0x', sink current <sup>2)3)</sup>
		-	-	-5	mA	PAD_DRV = '10', sink current <sup>2)3)</sup>
		-	-	-0.4	mA	PAD_DRV = '11', sink current <sup>2)3)</sup>
Output current (IFA / IFB / IFC - Pad)	I <sub>Q</sub>	-	-	-15	mA	PAD_DRV = '0x', sink current <sup>2)3)</sup>
		-	-	-5	mA	PAD_DRV = '1x', sink current <sup>2)3)</sup>
Input voltage	V <sub>IN</sub>	-0.3	-	5.5	V	V <sub>DD</sub> + 0.3 V may not be exceeded

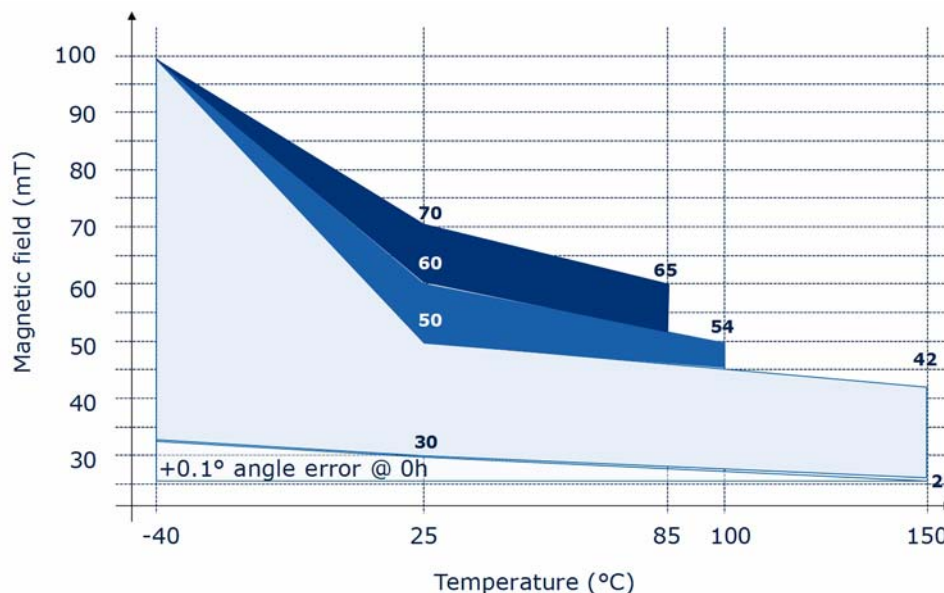
**Table 3 Operating range (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Magnetic induction at $T_A = 25^\circ\text{C}$ 4)5)	$B_{XY}$	30	-	50	mT	$-40^\circ\text{C} < T_J < 150^\circ\text{C}$
	$B_{XY}$	30	-	60	mT	$-40^\circ\text{C} < T_J < 100^\circ\text{C}$
	$B_{XY}$	30	-	70	mT	$-40^\circ\text{C} < T_J < 85^\circ\text{C}$
Expanded magnetic induction at $T_A = 25^\circ\text{C}$ 4)5)6)	$B_{XY}$	25	-	30	mT	Additional angle error of $0.1^\circ$
Angle range	Ang	0	-	360	$^\circ$	

- 1) Directly blocked with 100nF ceramic capacitor
- 2) Max. current to GND over open drain output
- 3) At  $V_{DD} = 5\text{V}$
- 4) Values refer to a homogenous magnetic field ( $B_{XY}$ ) without vertical magnetic induction ( $B_Z = 0\text{mT}$ ).
- 5) See [Figure 11](#)
- 6) 0h

The field strength of a magnet can be selected within the colored area of [Figure 11](#). By limitation of the junction temperature, a higher magnetic field can be applied. In case of a maximum temperature  $T_J=100^\circ\text{C}$  a magnet with up to 60mT at  $T_A=25^\circ\text{C}$  is allowed.

It is also possible to enlarge the magnetic field range for higher temperatures. In that case additional angle errors have to be considered (see Application Note "GMR Angle Error Extension").



**Figure 11 Magnet performance (ambient temperature)**

Note: The thermal resistances listed in [Table 29 "Package Parameters" on Page 46](#) must be used to calculate the corresponding ambient temperature of the sensor.

### Calculation of the Junction Temperature

The total power dissipation  $P_{TOT}$  of the chip increases its temperature above the ambient temperature.

The power multiplied by the total thermal resistance  $R_{thJA}$  (Junction to Ambient) leads to the final junction temperature.  $R_{thJA}$  is the sum of the addition of the values of the two components Junction to Case and Case to Ambient.

$$R_{thJA} = R_{thJC} + R_{thCA} \tag{1}$$

$$T_J = T_A + \Delta T$$

$$\Delta T = R_{thJA} \times P_{TOT} = R_{thJA} \times (V_{DD} \times I_{DD} + V_{OUT} \times I_{OUT}) \quad (I_{DD}, I_{OUT} > 0, \text{ if direction is into IC})$$

Example (assuming no load on  $V_{out}$ ):

$$V_{DD} = 5V \tag{2}$$

$$I_{DD} = 14mA$$

$$\Delta T = 150 \left[ \frac{K}{W} \right] \times (5[V] \times 0.014[A] + 0[VA]) = 10.5K$$

For molded sensors, the calculation with  $R_{thJC}$  is more adequate.

## 3.4 Characteristics

### 3.4.1 Electrical Parameters

The indicated electrical parameters apply to the full operating range, unless otherwise specified. The typical values correspond to a supply voltage  $V_{DD} = 5.0V$  and  $25^\circ C$ , unless individually specified. All other values correspond to  $-40^\circ C < T_J < 150^\circ C$ .

**Table 4 Electrical parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply current	$I_{DD}$	-	14	16	mA	
POR level	$V_{POR}$	2.0	-	2.9	V	Power On Reset
POR hysteresis	$V_{PORhy}$	-	30	-	mV	
Pull-up current	$I_{PU}$	-10	-	-225	$\mu A$	CSQ
		-10	-	-150	$\mu A$	DATA
Pull-down current	$I_{PD}$	10	-	225	$\mu A$	SCK
		10	-	150	$\mu A$	IFA, IFB, IFC
Power on time <sup>1)</sup>	$t_{Pon}$	-	5	7	ms	$V_{DD} > V_{DDmin}$ ; SBIST = 1
		-	-	0.5	ms	$V_{DD} > V_{DDmin}$ ; SBIST = 0

1) Within "Power On Time" write access is not permitted

**Table 5 Electrical parameters for  $4.5V < V_{DD} < 5.5V$**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input signal low level	$V_{L5}$	-	-	$0.3 V_{DD}$	V	
Input signal high level	$V_{H5}$	$0.7 V_{DD}$	-	-	V	
Output signal low level	$V_{OL5}$	-	-	1	V	DATA; $I_Q = - 25 \text{ mA}$ (PAD_DRV='0x'), $I_Q = - 5 \text{ mA}$ (PAD_DRV='10'), $I_Q = - 0.4 \text{ mA}$ (PAD_DRV='11')
		-	-	1	V	IFA,IFB, IFC; $I_Q = - 15 \text{ mA}$ (PAD_DRV='0x'), $I_Q = - 5 \text{ mA}$ (PAD_DRV='1x')

**Table 6 Electrical parameters for  $3.0V < V_{DD} < 3.6V$**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input signal low level	$V_{L3}$	-	-	$0.3 V_{DD}$	V	
Input signal high level	$V_{H3}$	$0.7 V_{DD}$	-	-	V	
Output signal low level	$V_{OL3}$	-	-	0.9	V	DATA; $I_Q = - 15 \text{ mA}$ (PAD_DRV='0x'), $I_Q = - 3 \text{ mA}$ (PAD_DRV='10'), $I_Q = - 0.24 \text{ mA}$ (PAD_DRV='11')
		-	-	0.9	V	IFA,IFB; $I_Q = - 10 \text{ mA}$ (PAD_DRV='0x'), $I_Q = - 3 \text{ mA}$ (PAD_DRV='1x')

### 3.4.2 ESD Protection

**Table 7 ESD protection**

Parameter	Symbol	Values		Unit	Notes
		min.	max.		
ESD voltage	$V_{HBM}$	-	$\pm 4.0$	kV	Human Body Model <sup>1)</sup>
	$V_{SDM}$	-	$\pm 0.5$	kV	Socketed Device Model <sup>2)</sup>

1) Human Body Model (HBM) according to: AEC-Q100-002

2) Socketed Device Model (SDM) according to: ESDA/ANSI/ESD SP5.3.2-2008

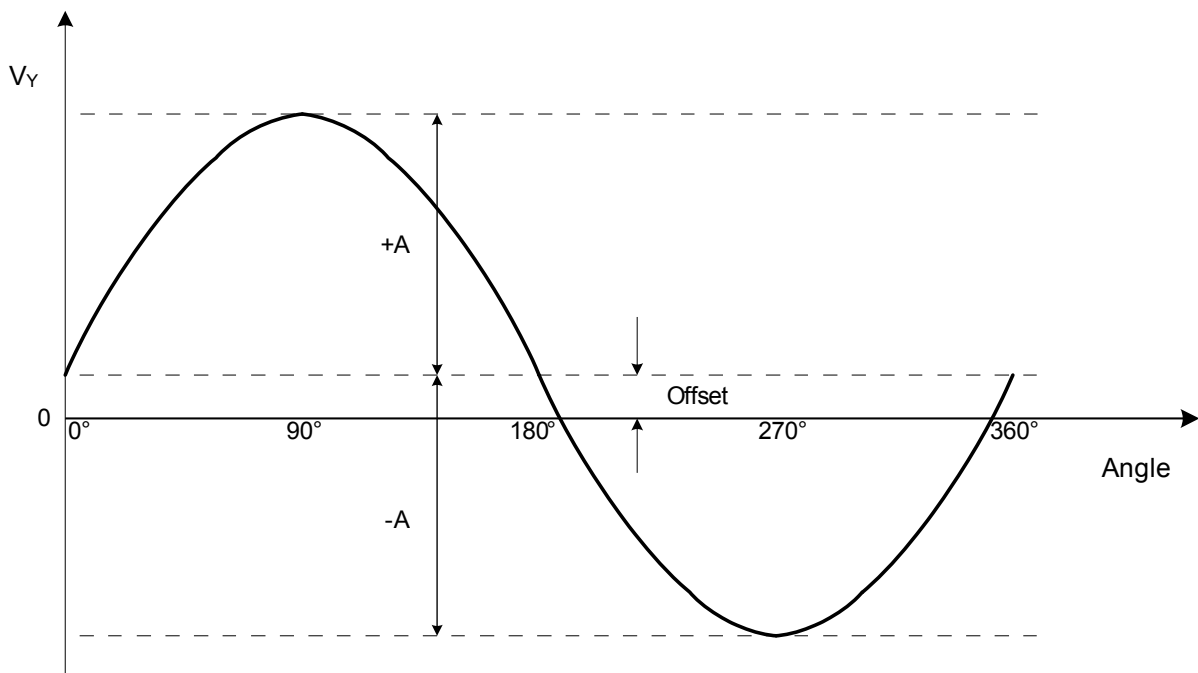
### 3.4.3 GMR Parameters

All parameters apply over  $B_{XY} = 30\text{mT}$  and  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

**Table 8 Basic GMR parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
X, Y output range	$RG_{ADC}$	-	-	$\pm 23230$	digits	Operating range
X, Y amplitude <sup>1)</sup>	$A_X, A_Y$	6000	9500	15781	digits	
		3922	-	20620	digits	Operating range
X, Y synchronism <sup>2)</sup>	k	87.5	100	112.49	%	
X, Y offset <sup>3)</sup>	$O_X, O_Y$	-2048	0	+2047	digits	
X, Y orthogonality error	$\Phi$	-11.25	0	+11.24	$^\circ$	
X, Y without field	$X_0, Y_0$	-5000	-	+5000	digits	Without magnet <sup>4)</sup>

- 1) See [Figure 12](#)
- 2)  $k = 100 \cdot (A_X / A_Y)$
- 3)  $O_Y = (Y_{MAX} + Y_{MIN}) / 2$ ;  $O_X = (X_{MAX} + X_{MIN}) / 2$
- 4) Not subject to production test - verified by design/characterization



**Figure 12 Offset and amplitude definition**



### 3.4.4 Angle Performance

After internal calculation the sensor has a remaining error, as shown in [Table 9](#). The error value refers to  $B_z = 0\text{mT}$  and the operating conditions given in [Table 3 “Operating range” on Page 18](#).

The overall angle error represents the relative angle error. This error describes the deviation to the reference line after zero angle definition.

**Table 9 Angle performance**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overall angle error (with auto-calibration)	$\alpha_{\text{Err}}$	-	0.6 <sup>1)</sup>	1.0	°	Including lifetime and temperature drift <sup>2)3)</sup>
Overall angle error (without auto-calibration)	$\alpha_{\text{Err}}$	-	0.6 <sup>1)</sup>	1.6	°	Including temperature drift <sup>2)3)4)</sup>

1) At 25°C, B = 30 mT

2) Including hysteresis error, caused by revolution direction change.

3) Only with calibrated GMR-compensation parameters of customer setup; Relative error after zero angle definition.

4) 0h

#### Autocalibration

The autocalibration enables online parameter calculation and reduces therefore the angle error due to temperature drifts, lifetime drifts and misalignments.

The TLE5012B is a precalibrated sensor. After start-up the parameters out of the laser fuses get loaded into flip-flops. The TLE5012B needs 1.5 revolutions to generate new autocalibration parameters. The update mode can be chosen within the Interface Mode 2 register (AUTOCAL). The parameters are updated in a smooth way to avoid an angle jump on the output. Therefore only one LSB will be changed within the choosen range or time. The autocalibration is done continuously.

AUTOCAL Modes:

- 00: No autocalibration
- 01: Autocalibration Mode 1. One LSB to final values within the update time  $t_{\text{upd}}$  (depending on FIR\_MD setting).
- 10: Autocalibration Mode 2. Only one LSB update over one full parameter generation (1.5 revolutions). After update of one LSB the autocalibration will calculate the parameters again.
- 11: Autocalibration Mode 3. One LSB to final values within an angle range of 11.25°.

### 3.4.5 Signal Processing

The signal path of the TLE5012B is depicted in [Figure 13](#). It consists of the GMR-bridge, ADC, filter and angle calculation. Depending on the filter configuration a different total delay time is achieved. Additional to this delay time, the delay time of the interface has to be considered. The delay time leads to an additional angle error at higher speeds. By enabling the prediction, the signal delay time can be reduced ([Figure 14](#)). The prediction uses the difference between current and last angle value and calculates the output value by adding this difference to the current value. So a linear prediction is achieved with following equation.

$$\alpha(t + 1) = 2 \cdot \alpha(t) - \alpha(t - 1) \tag{3}$$

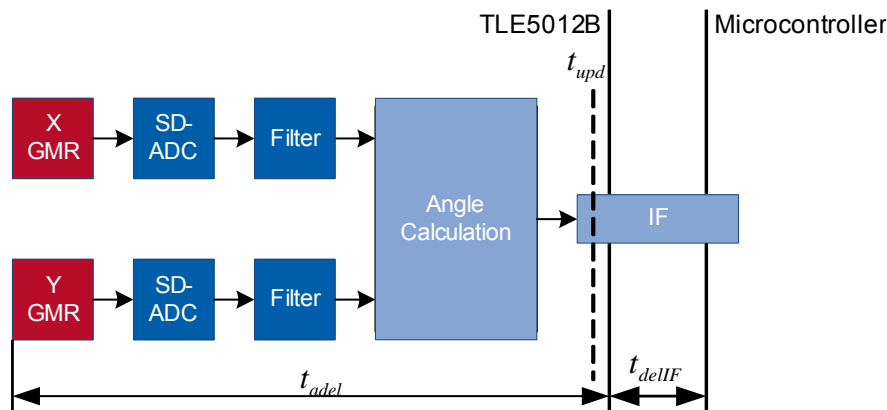


Figure 13 TLE5012B signal path

At FIR\_MD = '00' only raw values can be read out, due to the more time consuming angle calculation.

Table 10 Signal processing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Update rate at interface	$t_{upd}$	-	21.3	-	$\mu s$	FIR_MD = 0 (only raw values) <sup>1)2)</sup>
		-	42.7	-	$\mu s$	FIR_MD = 1 <sup>1)2)</sup>
		-	85.3	-	$\mu s$	FIR_MD = 2 (default) <sup>1)2)</sup>
		-	170.6	-	$\mu s$	FIR_MD = 3 <sup>1)2)</sup>
Angle delay time <sup>3)</sup>	$t_{adel}$	-	60	70	$\mu s$	FIR_MD = 1 <sup>1)2)</sup>
		-	80	95	$\mu s$	FIR_MD = 2 <sup>1)2)</sup>
		-	120	140	$\mu s$	FIR_MD = 3 <sup>1)2)</sup>
Angle delay time with prediction <sup>3)</sup>	$t_{adel}$	-	20	30	$\mu s$	FIR_MD = 1; PREDICT = 1 <sup>1)2)</sup>
		-	5	20	$\mu s$	FIR_MD = 2; PREDICT = 1 <sup>1)2)</sup>
		-	-40	-20	$\mu s$	FIR_MD = 3; PREDICT = 1 <sup>1)2)</sup>
Angle noise	$N_{Angle}$	-	0.11	-	$^{\circ}$	FIR_MD = 0, (1 Sigma) <sup>2)</sup>
		-	0.08	-	$^{\circ}$	FIR_MD = 1, (1 Sigma) <sup>2)</sup>
		-	0.05	-	$^{\circ}$	FIR_MD = 2, (1 Sigma) <sup>2)</sup> (default)
		-	0.04	-	$^{\circ}$	FIR_MD = 3, (1 Sigma) <sup>2)</sup>

1) Without internal oscillator frequency variation (Section 3.4.6)  
 2) Not subject to production test - verified by design/characterization  
 3) Valid at constant rotation speed

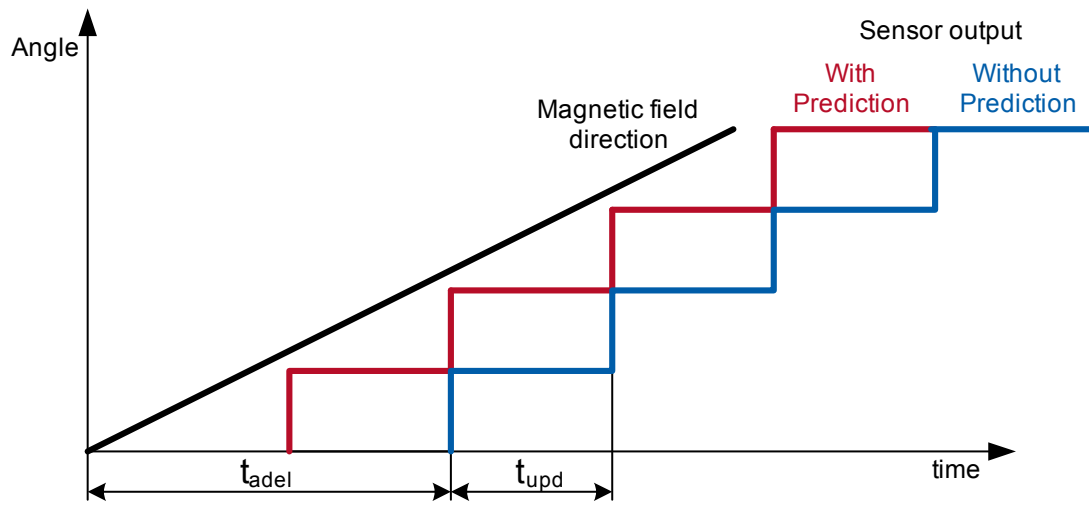


Figure 14 Delay of sensor output

### 3.4.6 Clock Supply (CLK Timing Definition)

If the external clock supply is selected, the clock signal input 'IFC' must fulfill certain requirements which are described in the following:

- The high or low pulse width must not exceed the specified values, because the PLL needs a minimum pulse width and must be spike filtered.
- The duty cycle factor should be 0.5 but can deviate to the values limited by  $t_{CLKh(f_{min})}$  and  $t_{CLKl(f_{min})}$ .
- The PLL is triggered at the positive edge of the clock. If more than 2 edges are missing, a chip reset is generated automatically.

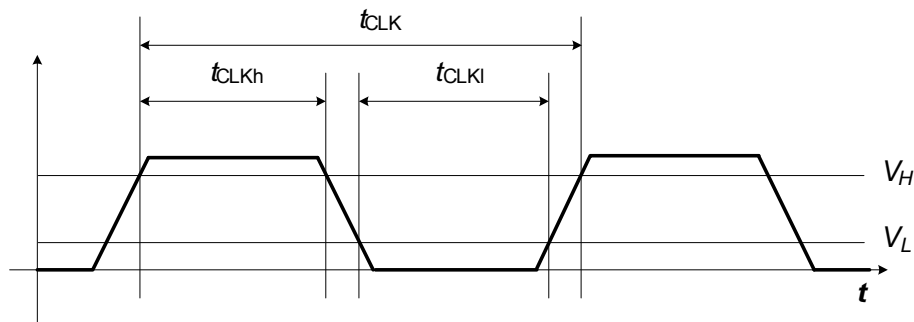


Figure 15 External CLK timing definition

Table 11 CLK timing specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	$f_{CLK}$	3.8	4.0	4.2	MHz	
CLK duty cycle <sup>1)2)</sup>	$CLK_{DUTY}$	30	50	70	%	
CLK rise time	$t_{CLKr}$	-	-	30	ns	From $V_L$ to $V_H$
CLK fall time	$t_{CLKf}$	-	-	30	ns	From $V_H$ to $V_L$
Digital clock	$f_{DIG}$	22.8	24	25.2	MHz	
Internal oscillator frequency	$f_{CLK}$	3.8	4.0	4.2	MHz	

1) Minimum Duty Cycle Factor:  $t_{CLKh(f_{min})} / t_{CLK(f_{min})}$  with  $t_{CLK(f_{min})} = 1 / f_{CLK(f_{min})}$

2) Maximum Duty Cycle Factor:  $t_{CLKh(f_{max})} / t_{CLK(f_{min})}$  with  $t_{CLKh(f_{max})} = t_{CLK(f_{min})} - t_{CLKl(min)}$

### 3.5 Interfaces

Within the register MOD\_3, the driver strength and so the slope for Push-Pull communication can be varied of the sensor output. The driver strength is specified in [Table 3](#) and the slope fall and rise time in [Table 12](#).

**Table 12 PAD characteristic**

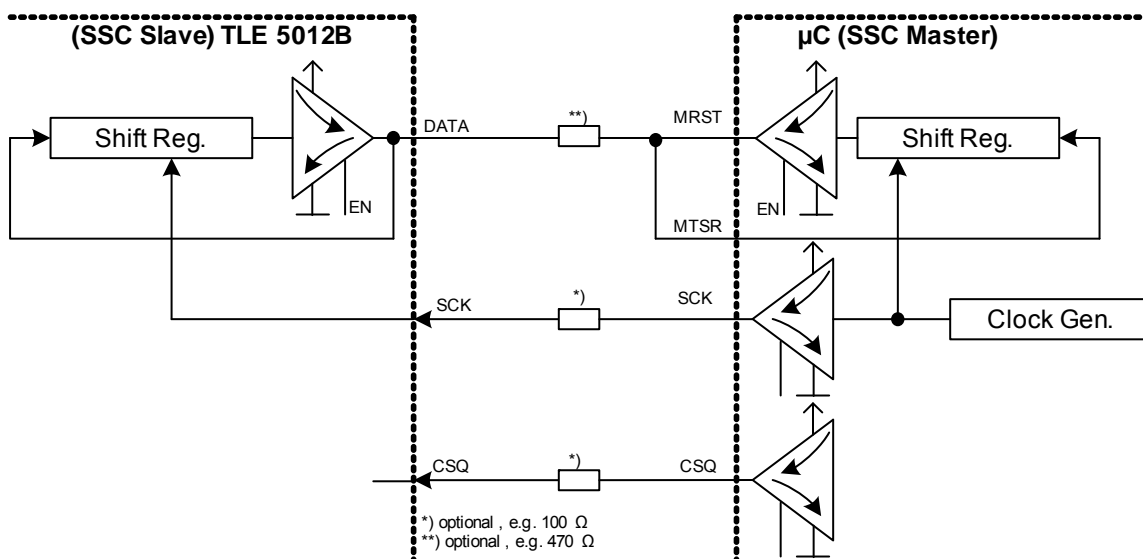
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output fall time	$t_{fall}, t_{rise}$	-	-	8	ns	DATA, 50pF, PAD_DRV='00' <sup>1)2)</sup>
Output rise time		-	-	28	ns	DATA, 50pF, PAD_DRV='01' <sup>1)2)</sup>
		-	-	45	ns	DATA, 50pF, PAD_DRV='10' <sup>1)2)</sup>
		-	-	130	ns	DATA, 50pF, PAD_DRV='11' <sup>1)2)</sup>
		-	-	15	ns	IFA/IFB, 20pF, PAD_DRV='0x' <sup>1)2)</sup>
		-	-	30	ns	IFA/IFB, 20pF, PAD_DRV='1x' <sup>1)2)</sup>

1) Valid for Push-Pull output

2) Not subject to production test - verified by design/characterization

#### 3.5.1 Synchronous Serial Communication (SSC) Interface

The 3-pin SSC Interface has a bi-directional push-pull data line, serial clock signal and chip select. The SSC Interface is designed to communicate with a microcontroller peer to peer for fast applications.



**Figure 16 SSC configuration in sensor-slave mode with push-pull outputs (high speed application)**

Another possibility is a 3-pin SSC Interface with bidirectional open-drain data line, serial clock signal and chip select. This setup is designed to communicate with a microcontroller in a bus system, together with other SSC slaves (e.g. two TLE5012B for redundancy reasons). This mode can be activated using bit SSC\_OD.

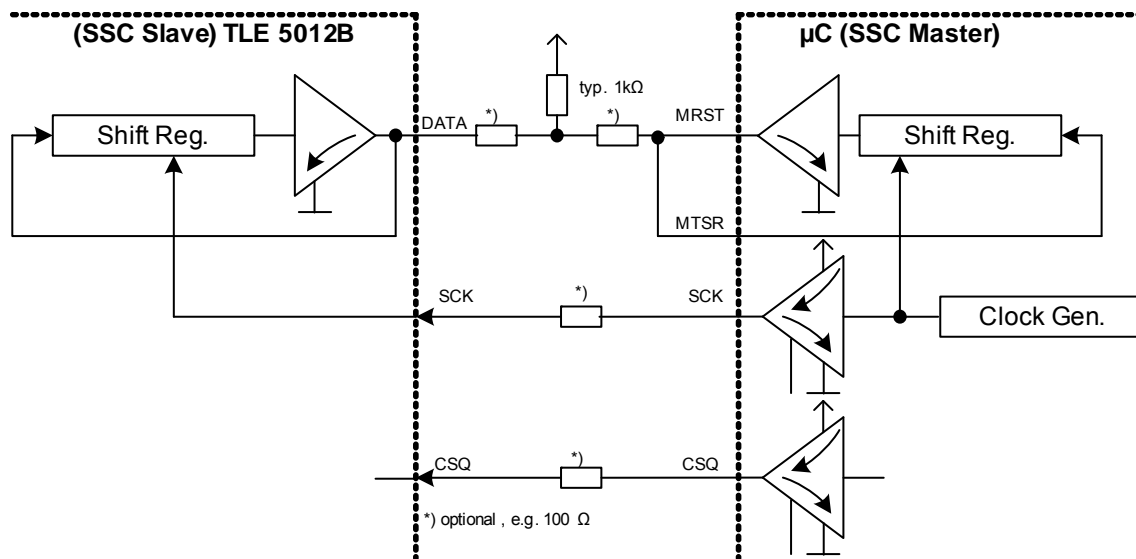


Figure 17 SSC configuration in sensor-slave mode and open drain (safe bus systems)

### 3.5.1.1 SSC Timing Definition

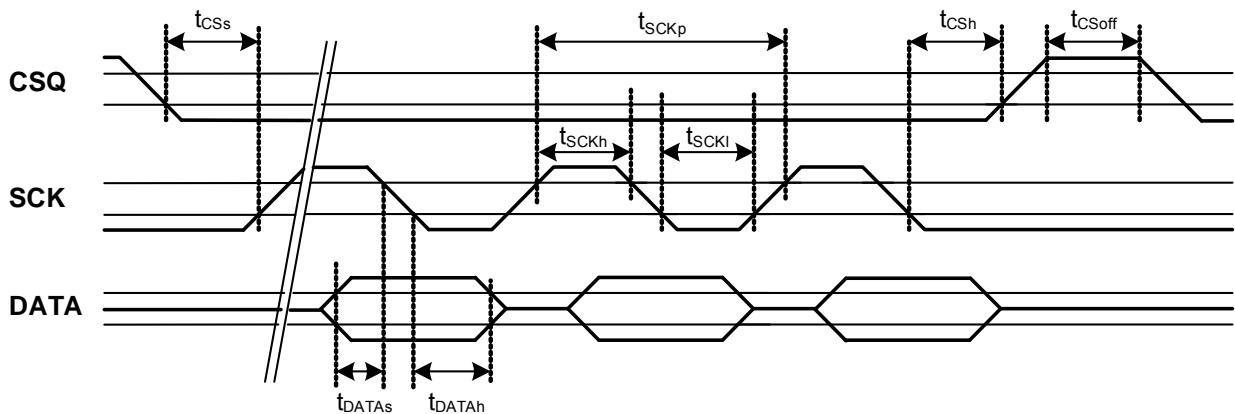


Figure 18 SSC timing

#### SSC Inactive Time ( $CS_{off}$ )

The SSC inactive time defines the delay time after a transfer before the TLE5012B can be selected again.

Table 13 SSC push-pull timing specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SSC baud rate	$f_{SSC}$	-	8.0	-	Mbit/s	
CSQ setup time	$t_{CSS}$	105	-	-	ns	
CSQ hold time	$t_{CSh}$	105	-	-	ns	
CSQ off	$t_{CSoff}$	600	-	-	ns	SSC inactive time
SCK period	$t_{SCKp}$	120	125	-	ns	
SCK high	$t_{SCKh}$	40	-	-	ns	

**Table 13 SSC push-pull timing specification (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCK low	$t_{SCKl}$	30	-	-	ns	
DATA setup time	$t_{DATA_s}$	25	-	-	ns	
DATA hold time	$t_{DATA_h}$	40	-	-	ns	
Write read delay	$t_{wr\_delay}$	130	-	-	ns	
Update time	$t_{CUpdate}$	1	-	-	$\mu$ s	see <a href="#">Figure 22</a>
SCK off	$t_{SCKoff}$	170	-	-	ns	

**Table 14 SSC open drain timing specification**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SSC baud rate	$f_{SSC}$	-	2.0	-	Mbit/s	Pull-up Resistor = 1k $\Omega$
CSQ setup time	$t_{CS_s}$	300	-	-	ns	
CSQ hold time	$t_{CS_h}$	400	-	-	ns	
CSQ off	$t_{CSoff}$	600	-	-	ns	SSC inactive time
SCK period	$t_{SCKp}$	500	-	-	ns	
SCK high	$t_{SCKh}$	-	190	-	ns	
SCK low	$t_{SCKl}$	-	190	-	ns	
DATA setup time	$t_{DATA_s}$	25	-	-	ns	
DATA hold time	$t_{DATA_h}$	40	-	-	ns	
Write read delay	$t_{wr\_delay}$	130	-	-	ns	
Update time	$t_{CUpdate}$	1	-	-	$\mu$ s	see <a href="#">Figure 22</a>
SCK off	$t_{SCKoff}$	170	-	-	ns	



### 3.5.1.2 SSC Data Transfer

The SSC data transfer is word aligned. The following transfer words are possible:

- Command word (to access and change operating modes of the TLE5012B)
- Data words (any data transferred in any direction)
- Safety word (confirms the data transfer and provide status information)

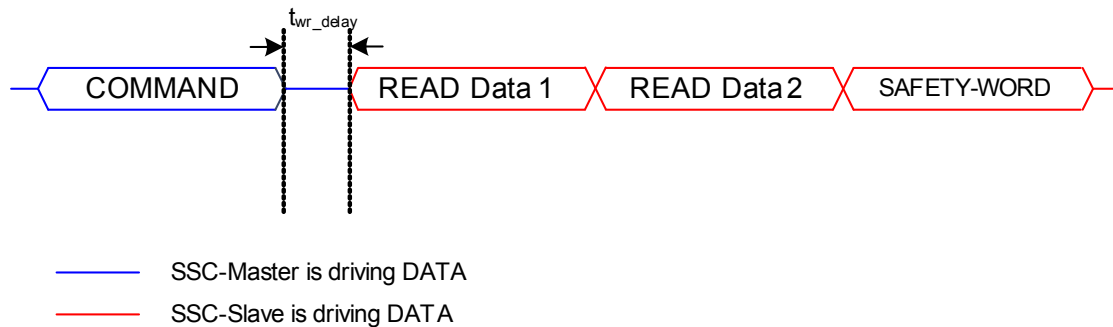


Figure 19 SSC data transfer (data read example)

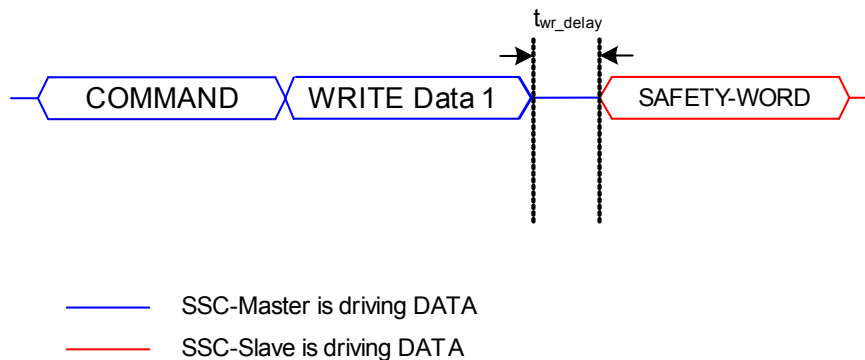


Figure 20 SSC data transfer (data write example)

#### Command Word

The TLE5012B is controlled by a command word. It is sent first at every data transmission. The structure of the command word is shown in [Table 15](#), where the UPD-bit allows the access to current values or updated values. If an update command is issued and the update bit (UPD) is set, the immediate values are stored in the update buffer simultaneously. This enables a snapshot of all necessary system parameters at the same time. Bits with an update buffer are marked by an “u” in type of register description. The initialization of such an update is described on page [32](#).

Table 15 Structure of the Command Word

Name	Bits	Description
RW	[15]	Read - Write 0:Write 1:Read
Lock	[14..11]	4 bit Lock Value 0000 <sub>B</sub> : Default Operating Access for addresses 0x00:0x04 1010 <sub>B</sub> : Config- Access for addresses 0x05:0x11

**Table 15 Structure of the Command Word**

Name	Bits	Description
UPD	[10]	Update-Register Access 0: Access to current values 1: Access to updated values
ADDR	[9..4]	6-bit Address
ND	[3..0]	4-bit Number of Data-Words

**Safety Word**

The safety word contains following bits:

**Table 16 Structure of the Safety Word**

Name	Bits	Description
STAT	Chip and Interface Status	
	[15]	Indication of Chip-Reset (resets after readout) via SSC 0: Reset occurred 1: No reset Reset: 1 <sub>B</sub>
	[14]	System Error (e.g. Overvoltage; Undervoltage; V <sub>DD-</sub> , GND- off; ROM;...) 0: Error occurred (S_VR; S_DSPU; S_OV; S_XYOL: S_MAGOL; S_ADCM; S_FUSE) 1: No error
	[13]	Interface Access Error (access to wrong address; wrong lock) 0: Error occurred 1: No error
	[12]	Valid Angle Value (no system error; no interface error; NO_GMR_A = '0'; NO_GMR_XY='0') 0: Angle value invalid 1: Angle value valid
RESP	[11..8]	Sensor Number Response Indicator The sensor no. bit is pulled low and the other bits are high.
CRC	[7..0]	Cyclic Redundancy Check (CRC)

**Bit Types**

The types of bits used in the registers are listed here:

**Table 17 Bit Types**

Abbreviation	Function	Description
R	Read	Read-only registers
W	Write	Read and write registers
U	Update	Update buffer for this bit is present. If an update is issued and the Update-Register Access bit (UPD in Command Word) is set, the immediate values are stored in this update buffer simultaneously. This enables a snapshot of all necessary system parameters at the same time.

Data communication via SSC

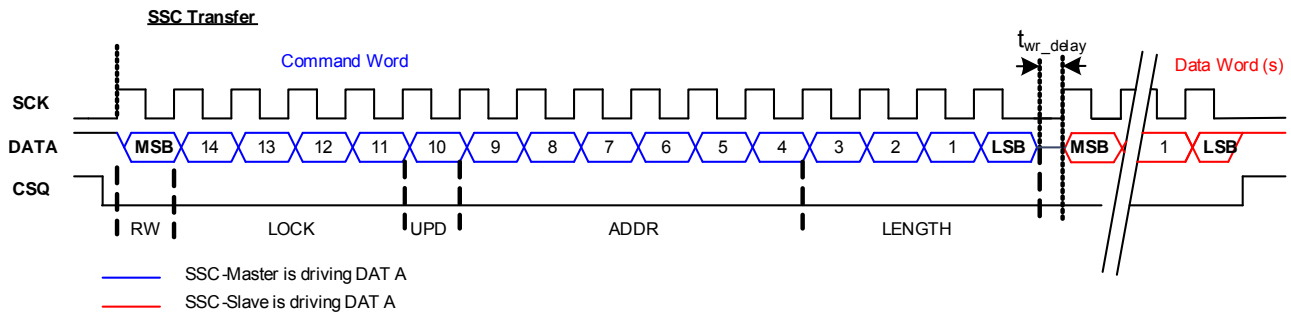


Figure 21 SSC bit ordering (read example)

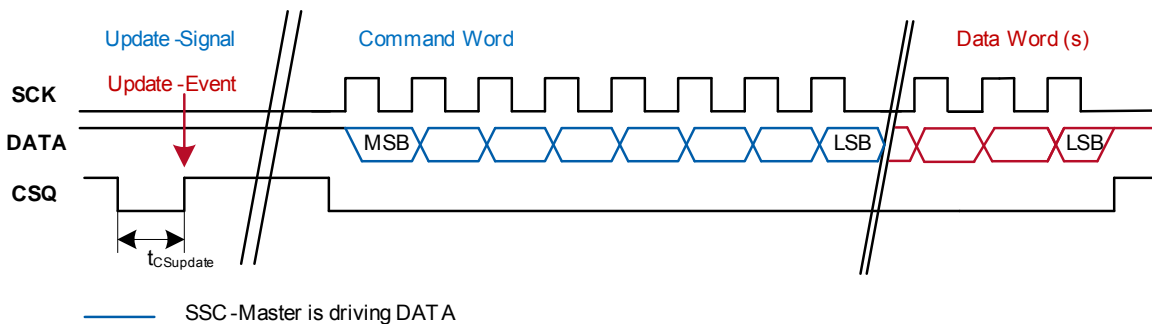


Figure 22 Update of update-registers

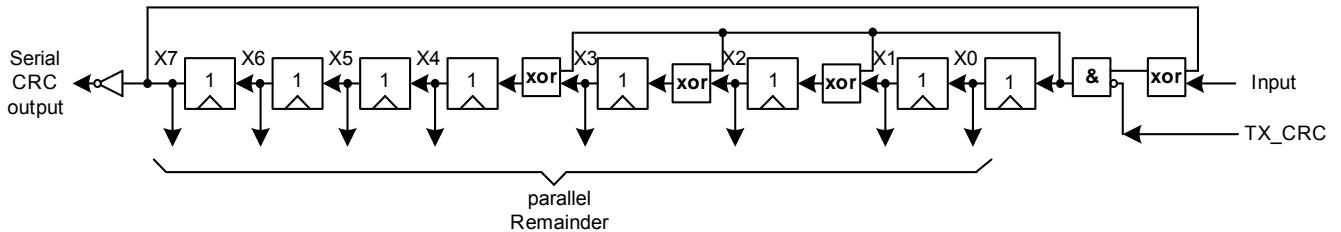
The data communication via SSC interface has the following characteristic:

- The data transmission order is “Most Significant Bit (MSB) first”.
- Data is put on the data line with the rising edge on SCK and read with the falling edge on SCK.
- The SSC Interface is word-aligned. All functions are activated after each transmitted word.
- A “high” condition on the negated Chip Select pin (CSQ) of the selected TLE5012B interrupts the transfer immediately. The CRC calculator is automatically reset.
- After changing the data direction, a delay ( $t_{wr\_delay}$ ) has to be considered before continuing the data transfer. This is necessary for internal register access.
- Every access to the TLE5012B with the number of data (ND)  $\geq 1$  is performed with address auto-increment.
- At an overflow at address  $3F_H$  the transfer continues at address  $00_H$ .
- With ND = 0 no auto-increment is done and a continuously readout of the same address can be realized. Afterwards no Safety Word is send and the transfer ends with high condition on CSQ.
- After every data transfer with ND  $\geq 1$  the 16 bit Safety Word will be appended by the selected TLE5012B.
- At a rising edge of CSQ without data transfer before (no SCK-pulse), the update-registers are updated with according values (Figure 22).
- After sending the Safety Word the transfer ends. To start another data transfer, the CSQ has to be deselected once for  $t_{CSoff}$ .
- The SSC is default Push-Pull. The Push-Pull driver is only active, if the TLE5012B has to send data, otherwise the Push-Pull is disabled for receiving data from the microcontroller.

Cyclic Redundancy Check (CRC)

- This CRC is according to the J1850 Bus-Specification.
- Every new transfer resets the CRC generation.
- Every Byte of a transfer will be taken into account to generate the CRC (also the sent command(s)).

- Generator-Polynomial:  $X^8+X^4+X^3+X^2+1$ , but for the CRC generation the fast-CRC generation circuit is used (see [Figure 23](#))
- The remainder of the fast CRC circuit is initial set to '11111111<sub>B</sub>'.
- Remainder is inverted before transmission.



**Figure 23 Fast CRC polynomial division circuit**

### 3.5.1.3 Registers Chapter

The registers of the TLE5012B are described within the application note "Register Setting of TLE5012B".

### 3.5.2 Pulse Width Modulation Interface

The **Pulse Width Modulation (PWM)** Interface can be selected via SPI (IF\_MD = '001').

The PWM update rate can be programmed within the register 0E<sub>H</sub> (IFAB\_RES) in following steps:

- ~0.25 kHz with 12 bit resolution
- ~0.5 kHz with 12 bit resolution
- ~1.0 kHz with 12 bit resolution
- ~2.0 kHz with 12 bit resolution

PWM uses a square wave with constant frequency whose duty cycle is modulated resulting in an average value of the waveform.

[Figure 24](#) shows the principle behavior of a PWM with different duty cycles and the definition of timing values. The duty cycle of a PWM is defined by following general formulas:

$$Duty\ Cycle = \frac{t_{on}}{t_{PWM}}$$

$$t_{PWM} = t_{on} + t_{off}$$

$$f_{PWM} = \frac{1}{t_{PWM}}$$

(4)

The range between 0 - 6.25% and 93.75 - 100% is used only for diagnostic purposes. More details are given in [Table 18](#).

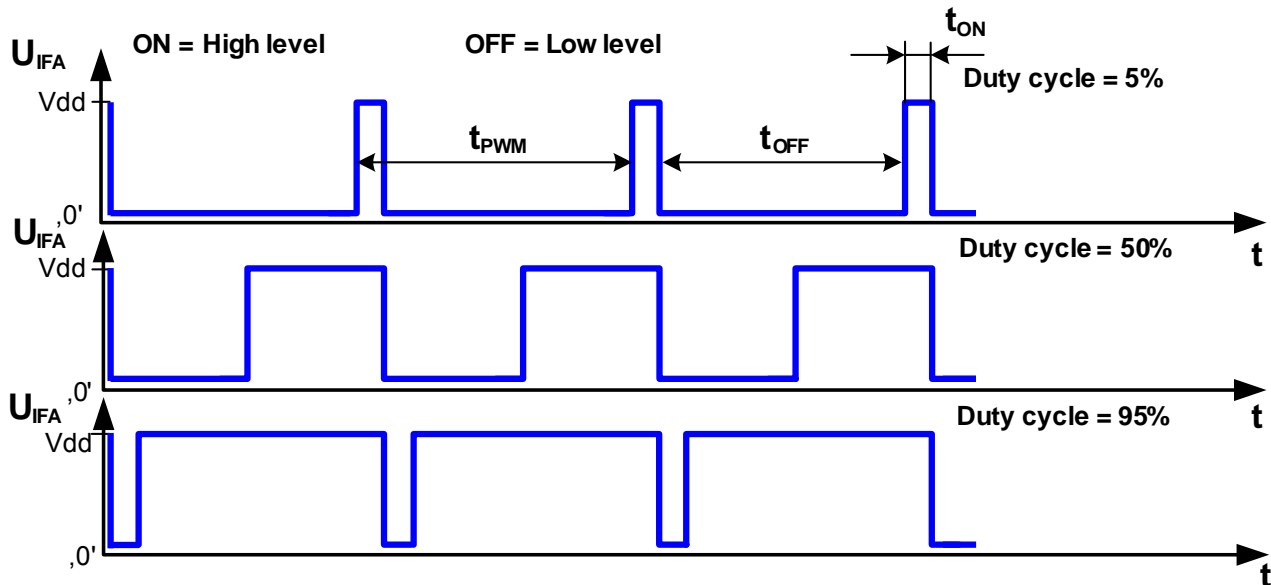


Figure 24 Typical example for a PWM signal

Table 18 PWM interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PWM output frequency	$f_{PWM}$	244	-	1953	Hz	Selectable by IFAB_RES <sup>1)</sup>
Output duty cycle range	$DY_{PWM}$	6.25	-	93.75	%	Absolute Angle
		-	2	-	%	Electrical Error (S_RST; S_VR)
		-	98	-	%	System Error (S_FUSE; S_OV; S_XYOL; S_MAGOL; S_ADCT)
		0	-	1	%	Short to GND
		99	-	100	%	Short to V <sub>DD</sub> , Power-Loss
PWM period variation	$t_{PWMvar}$	-5	-	5	%	<sup>2)</sup>

1)  $f_{PWM} = (f_{DIG} * 2^{IFAB\_RES}) / (24 * 4096)$

2) Depends on internal oscillator frequency variation (Section 3.4.6)

### 3.5.3 Short PWM Code

The Short PWM Code (SPC) is a synchronized data transmission based on the SENT protocol (Single Edge Nibble Transmission) defined by SAE J2716. SPC enables the use of enhanced protocol functionality due to the ability to select between different sensor slaves (ID selection). The slave number (S\_NR) can be given by the external circuit of SCK and IFC pin. In case of V<sub>DD</sub> on SCK the S\_NR[0] can be set to “1” and in the case of GND on SCK the S\_NR[0] is equal “0”. S\_NR[1] can be adjusted in the same way by IFC pin.

As in SENT, the time between two consecutive falling edges defines the value of a four bit nibble, thus representing numbers between 0 and 15. The transmission time therefore depends on the transmitted data values. The single edge is defined by a 3 unit time (UT) low pulse on the output, followed by the high time defined in the protocol (nominal values, may vary by tolerance of internal oscillator and influence by external circuitry). All values are multiples of a unit time frame concept. A transfer consists of the following parts (Figure 25):

- A trigger pulse by the master, which initiates the data transmission
- A synchronization period of 56 UT (in parallel, a new sample is calculated)
- A status nibble of 12-27 UT
- Between 3 and 6 data nibbles of 12-27 UT
- A CRC nibble of 12-27 UT
- An end pulse to terminate the SPC transmission

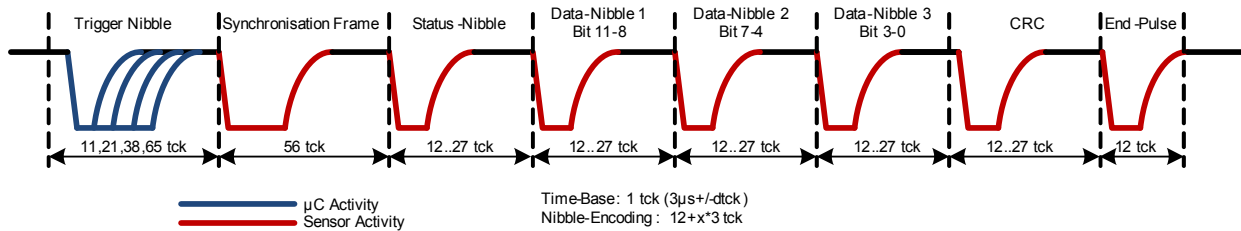


Figure 25 SPC frame example

The CRC checksum includes the status nibble and the data nibbles and can be used to check the validity of the decoded data. The sensor is available for next sample 90µs after the falling edge of the end pulse.

In parallel to the SPC, the SPI can be used for individual configuration. The number of transmitted SPC nibbles can be changed to customize the amount of information sent by the sensor. The frame contains a 16bit angle value and a 8bit temperature value in the full configuration.

Table 19 Frame configuration

Frame type	IFAB_RES	Data nibbles
12bit angle	00	3 nibbles
16bit angle	01	4 nibbles
12bit angle, 8bit temperature	10	5 nibbles
16bit angle, 8bit temperature	11	6 nibbles

The status nibble allows to check internal states and conditions of the sensor.

**Table 20 Structure of Status Nibble**

Name	Bits	Description
SYS_ERR	[3]	Indication of system error (S_FUSE, S_OV, S_XYOL, S_MAGOL, S_ADCT) 0: No system error 1: System error occurred
ELEC_ERR	[2]	Indication of electrical error (S_RST, S_VR) 0: No electrical error 1: Electrical error occurred
S_NR	[1]	Slave number bit 1 (level on IFC)
	[0]	Slave number bit 0 (level on SCK)

### 3.5.3.1 Unit Time Setup

The basic SPC protocol unit time granularity is defined as 3µs. Every timing is a multiple of this basic time unit. To achieve more flexibility, trimming of the unit time can be done within IFAB\_HYST. This enables a setup of different unit times.

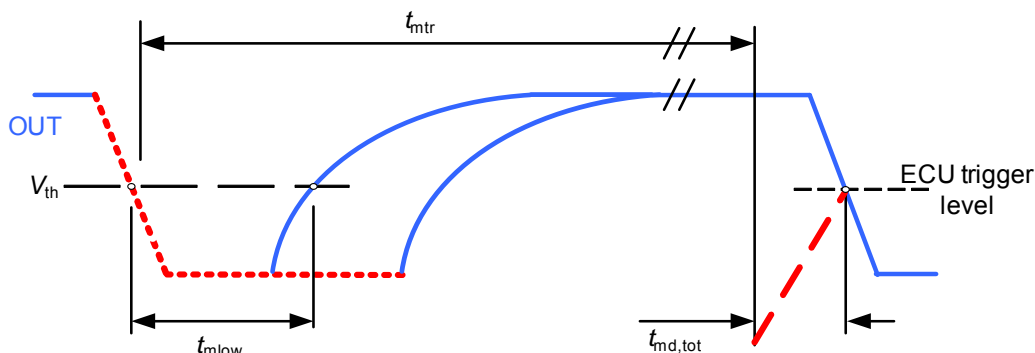
**Table 21 Predivider setting**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Unit time	$t_{Unit}$	-	3.0	-	µs	IFAB_HYST = 00
		-	2.5	-		IFAB_HYST = 01
		-	2.0	-		IFAB_HYST = 10
		-	1.5	-		IFAB_HYST = 11

### 3.5.3.2 Master Pulse Requirements

An SPC transmission is initiated by a master pulse on the IFA pin. To detect a low level on the IFA pin, the voltage must be below a threshold  $V_{thr}$ . The sensor detects that the IFA line has been released as soon as  $V_{thr}$  is crossed. **Figure 26** shows the timing definitions for the master pulse. The master low time  $t_{m\text{low}}$  as well as the total trigger time  $t_{m\text{tr}}$  are given in **Table 22**.

If the master low time exceeds the maximum low time, the sensor does not respond and is available for a next triggering 30µs after the master pulse crosses  $V_{thr}$ .  $t_{md,tot}$  is the delay between internal triggering of the falling edge in the sensor and the triggering of the ECU.



**Figure 26 SPC Master pulse timing**



**Table 22 Master pulse parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Threshold	$V_{th}$	-	50	-	% of $V_{DD}$	
Threshold hysteresis	$V_{thhyst}$	-	8	-	% of $V_{DD}$	$V_{DD} = 5V$
		-	3	-	$V_{DD}$	$V_{DD} = 3V$
Total trigger time	$t_{mtr}$	-	90	-	UT	SPC_Trigger = 0; <sup>1)</sup>
		-	$t_{mlow} + 12$	-	UT	SP_Trigger = 1
Master low time	$t_{mlow}$	8	12	14	UT	S_NR = 00
		16	22	27		S_NR = 01
		29	39	48		S_NR = 10
		50	66	81		S_NR = 11
Master delay time	$t_{md,tot}$	-	5.8	-	$\mu s$	

1) Trigger time in the sensor is fixed to the number of units specified in the “typ.” column, but the effective trigger time varies due to the sensor’s clock variation

### 3.5.3.3 Checksum nibble details

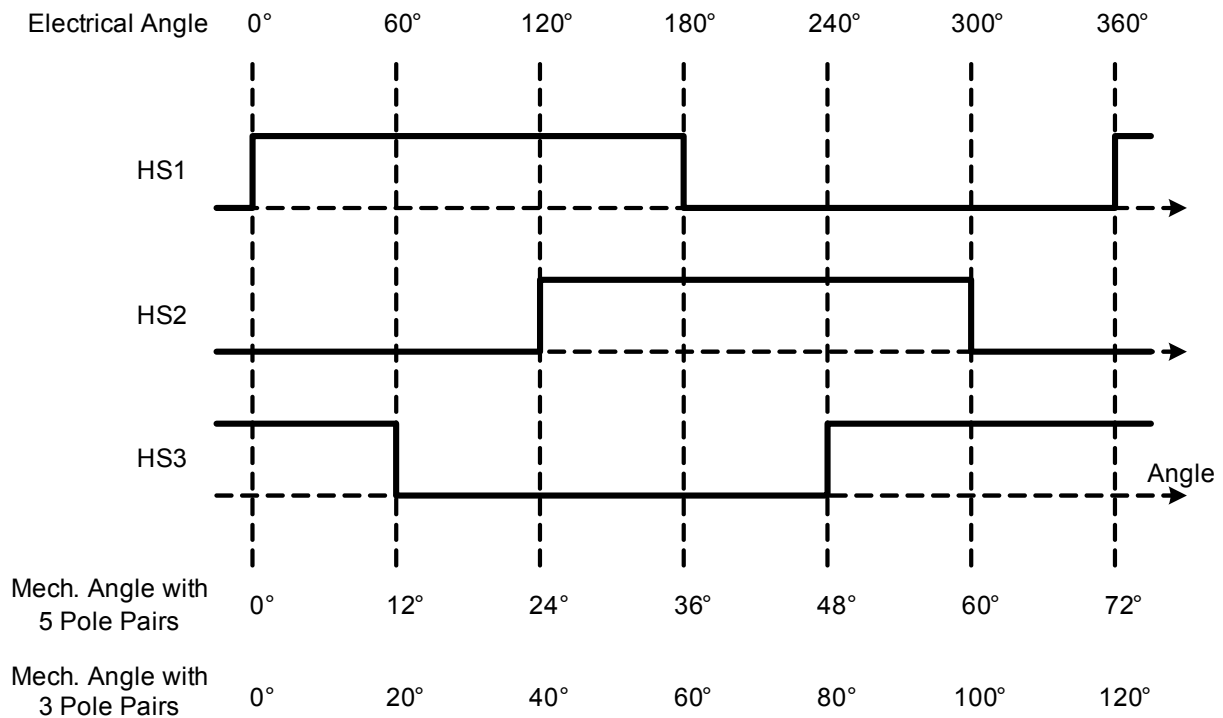
The checksum nibble is a 4-bit CRC of the data nibbles including the status nibble. The CRC is calculated using a polynomial  $x^4+x^3+x^2+1$  with a seed value of 0101. The remainder after the last Data-nibble is used are transferred as CRC.

### 3.5.4 Hall Switch Mode

The **Hall Switch Mode (HSM)** within the TLE5012B allows to emulate the output of three Hall switches. Hall switches are often used in electrical commutated motors to get information of the rotor position. With these three output signals the motor will be commutated in the right way. Depending on the used pole pairs of the rotor, different amount of electrical periods have to be realized. This is selectable within  $0E_H$  (HSM\_PLP). **Figure 27** depicts the three output signals with the relationship between electrical angle and mechanical angle. The mechanical  $0^\circ$  point is always used as reference.

The HSM is generally used with Push -Pull output, but it can be changed to Open- Drain within IFAB\_OD.

**Hall-Switch-Mode: 3phase Generation**



**Figure 27 Hall Switch Mode**

The HSM Interface can be selected via SPI (IF\_MD = '010').

**Table 23 Hall Switch Mode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rotation speed	n	-	-	10000	rpm	Mechanical

Table 23 Hall Switch Mode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Electrical angle accuracy	$\alpha_{\text{elect}}$	-	0.6	1	°	1 polepairs with autocalibration <sup>1)2)</sup>
		-	1.2	2		2 polepairs with autocal. <sup>1)2)</sup>
		-	1.8	3		3 polepairs with autocal. <sup>1)2)</sup>
		-	2.4	4		4 polepairs with autocal. <sup>1)2)</sup>
		-	3.0	5		5 polepairs with autocal. <sup>1)2)</sup>
		-	3.6	6		6 polepairs with autocal. <sup>1)2)</sup>
		-	4.2	7		7 polepairs with autocal. <sup>1)2)</sup>
		-	4.8	8		8 polepairs with autocal. <sup>1)2)</sup>
		-	5.4	9		9 polepairs with autocal. <sup>1)2)</sup>
		-	6.0	10		10 polepairs with autocal. <sup>1)2)</sup>
		-	6.6	11		11 polepairs with autocal. <sup>1)2)</sup>
		-	7.2	12		12 polepairs with autocal. <sup>1)2)</sup>
		-	7.8	13		13 polepairs with autocal. <sup>1)2)</sup>
		-	8.4	14		14 polepairs with autocal. <sup>1)2)</sup>
-	9.0	15	15 polepairs with autocal. <sup>1)2)</sup>			
-	9.6	16	16 polepairs with autocal. <sup>1)2)</sup>			
Mechanical angle switching hysteresis	$\alpha_{\text{HShystm}}$	0	-	0.703	°	Selectable by IFAB_HYST <sup>3)4)</sup>

**Table 23 Hall Switch Mode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Electrical angle switching hysteresis <sup>5)</sup>	$\alpha_{HShystel}$	-	0.70	-	°	1 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	1.41	-		2 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	2.11	-		3 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	2.81	-		4 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	3.52	-		5 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	4.22	-		6 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	4.92	-		7 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	5.62	-		8 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	6.33	-		9 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	7.03	-		10 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	7.73	-		11 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	8.44	-		12 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	9.14	-		13 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	9.84	-		14 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	10.55	-		15 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
		-	11.25	-		16 polepairs; IFAB_HYST=11 <sup>1)2)</sup>
Fall time	$t_{HSfall}$	-	0.02	1	$\mu s$	$R_L = 2.2k\Omega; C_L < 50pF$
Rise time	$t_{HSrise}$	-	0.4	1	$\mu s$	$R_L = 2.2k\Omega; C_L < 50pF$

- 1) Depends on internal oscillator frequency variation ([Section 3.4.6](#))
- 2) Not subject to production test - verified by design/characterization
- 3) GMR hysteresis not considered
- 4) Minimum hysteresis without switching
- 5) The hysteresis has to be considered only at change of rotation direction

To avoid switching on mechanical vibrations of the rotor, a hysteresis is recommended ([Figure 28](#)).

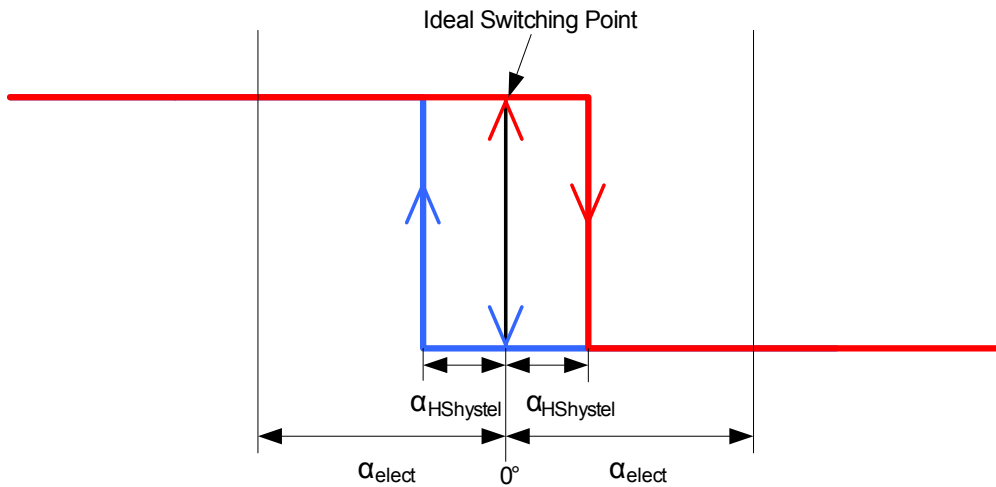


Figure 28 HS hysteresis

### 3.5.5 Incremental Interface

The Incremental Interface (IIF) uses an up/down counter of a microcontroller for the angle transmission. The synchronization is done by the parallel active SSC-Interface. The angle value read out by the SSC-Interface can be compared with the stored counter value. In case of a non-synchronization, the microcontroller add the difference to the actual counter value to synchronize the TLE5012B with the microcontroller. The resolution of the IIF can be selected within the interface mode4 register (MOD\_4) under IFAB\_RES.

After startup the IIF pulses out the actual absolute angle value. So the microcontroller gets the information of the absolute position. The Index-Signal which indicates the zero crossing is available on IFC pin.

In register MOD\_1 the incremental interface can be chosen between A/B mode and Step/Direction mode (IIF\_MOD).

Within the TLE5012B the incremental interface is implemented like a quadratur encoder with 50% duty cycle.

#### A/B Mode

The phase shift between phase A and B indicates a clockwise (A follows B) or a counterclockwise (B follows A) rotation of the magnet.

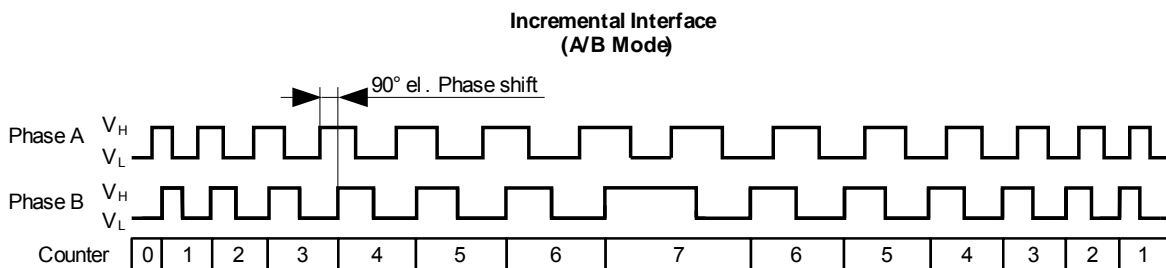
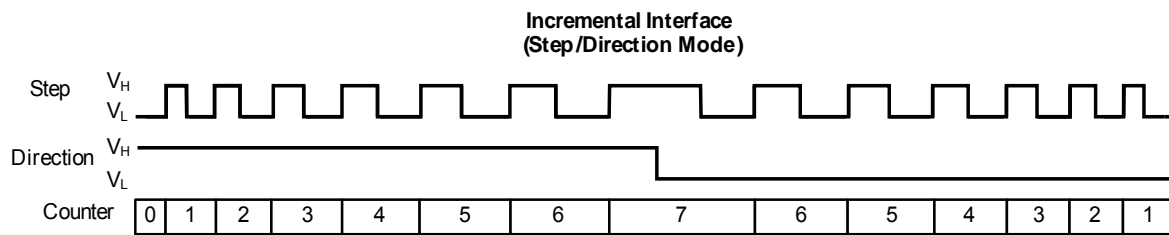


Figure 29 Incremental interface with A/B mode

#### Step/Direction Mode

Phase A pulses out the increments and phase B indicates the direction (Figure 30).



**Figure 30** Incremental interface with Step/Direction mode

**Table 24** Incremental Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Incremental output frequency	$f_{inc}$	-	-	1.0	MHz	Frequency of phase A and phase B
Index	$t_{0^\circ}$	-	5	-	$\mu s$	$0^\circ$

### 3.6 Test Structure

#### 3.6.1 ADC Test Vectors

It is possible to feed the ADCs with appropriate values to simulate a certain magnet position and other GMR effects. This test can be activated within SIL register (ADCTV\_EN). With ADCTV\_Y and ADCTV\_X the vector length can be adjusted like [Figure 31](#).

The values are generated with resistors on the chip.

The following X/Y ADC values can be programmed:

- 4 points, circle amplitude = 70% ( $0^\circ, 90^\circ, 180^\circ, 270^\circ$ )
- 8 points, circle amplitude = 100% ( $0^\circ, 45^\circ, 90^\circ, 135^\circ, 180^\circ, 225^\circ, 270^\circ, 315^\circ$ )
- 8 points, circle amplitude = 122.1% ( $35.3^\circ, 54.7^\circ, 125.3^\circ, 144.7^\circ, 215.3^\circ, 234.7^\circ, 305.3^\circ, 324.7^\circ$ )
- 4 points, circle amplitude = 141.4% ( $45^\circ, 135^\circ, 225^\circ, 315^\circ$ )

*Note: The 100% values typically correspond to 21700 digits and the 70% values to 15500 digits.*

**Table 25** ADC test vectors

Register bits	X/Y values (decimal)		
	min.	typ.	max.
000		0	
001		15500	
010		21700	
011		32767	
100 <sup>1)</sup>		0	
101		-15500	
110		-21700	
111		-32768	

1) Not allowed to use.

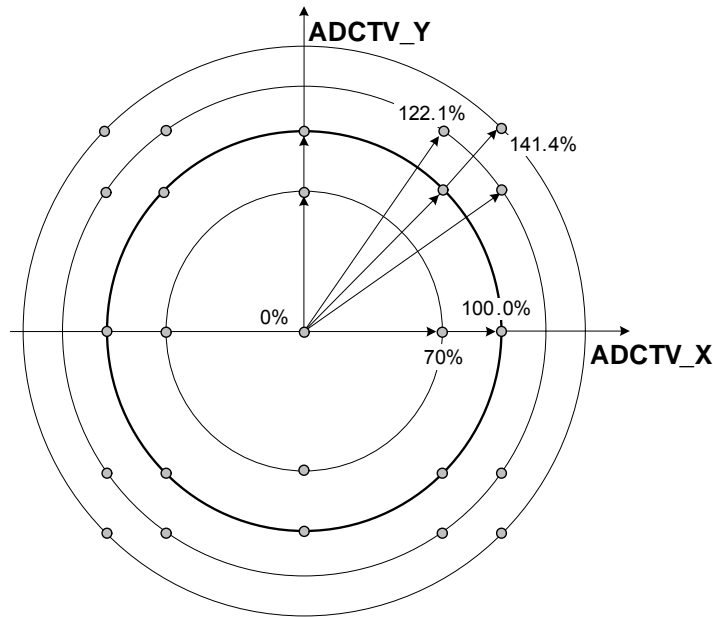


Figure 31 ADC test vectors

**Examples for ADC test vector check**

The sensor has to be selected first via CSQ and also SCK must be available for the communication. [Table 26](#) shows the structure of the communication to enable the ADC test vector for 54.7°.

Table 26 SSC Command to enable ADC test vector check

SSC Word No.	Description	Master transmitting	TLE5012 transmitting	Note
1	Command	0_1010_0_000111_0001		
2	Write Data	0_0_000_0_000_1_010_001		Check of 54.7°
3	Safety Word		1_1_1_0_XXXX_XXXXXXXXXX	

Table 27 Structure of Write Data for some different test vectors

SSC Word No.	Description	Master transmitting	TLE5012 transmitting	Note
1	Write Data	0_0_000_0_000_1_001_101		~135°
2	Write Data	0_0_000_0_000_1_010_110		~135°
3	Write Data	0_0_000_0_000_1_101_110		~215.3°
4	Write Data	0_0_000_0_000_1_101_000		~270°
5	Write Data	0_0_000_0_000_1_101_010		~324.7°

### 3.7 Overvoltage Comparators

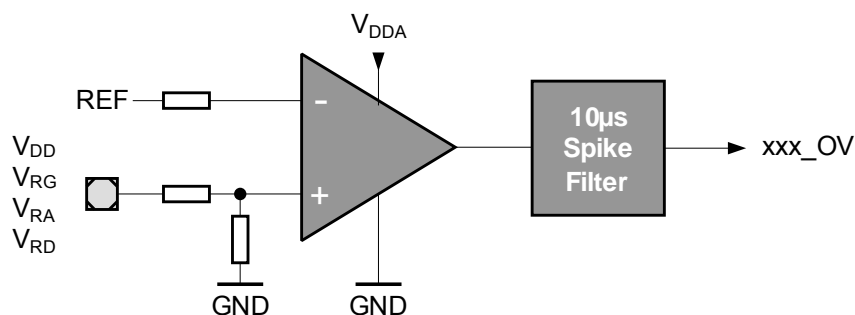
Various comparators monitor the voltage in order to ensure error free operation. The overvoltages must be active at least 256 periods of  $t_{DIG}$  to set the test comparator bits in the SSC Interface registers. This works as digital spike suppression.

**Table 28 Test comparators**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overvoltage detection	$V_{OVG}$	-	2.80	-	V	
	$V_{OVA}$	-	2.80	-	V	
	$V_{OVD}$	-	2.80	-	V	
$V_{DD}$ overvoltage	$V_{DDOV}$	-	6.05	-	V	
$V_{DD}$ undervoltage	$V_{DDUV}$	-	2.70	-	V	
GND - off voltage	$V_{GNDoff}$	-	-0.55	-	V	
$V_{DD}$ - off voltage	$V_{VDDoff}$	-	0.55	-	V	
Spike filter delay	$t_{DEL}$	-	10	-	$\mu$ s	

#### 3.7.1 Internal Supply Voltage Comparators

Every voltage regulator has an overvoltage comparator to detect a malfunction. If the nominal output voltage of 2.5 V is larger than  $V_{OVG}$ ,  $V_{OVA}$  and  $V_{OVD}$ , then this overvoltage comparator is activated.



**Figure 32 OV comparator**

#### 3.7.2 $V_{DD}$ Overvoltage Detection

The Overvoltage Detection Comparator monitors the external supply voltage at the  $V_{DD}$  pin. It activates the  $S_{VR}$  bit. (Figure 32)

#### 3.7.3 GND - Off Comparator

The GND - Off Comparator is used to detect a voltage difference between the GND pin and SCK. It activates the  $S_{VR}$  bit of the SSC - Interface. This circuit can detect a disconnection of the Supply GND Pin.



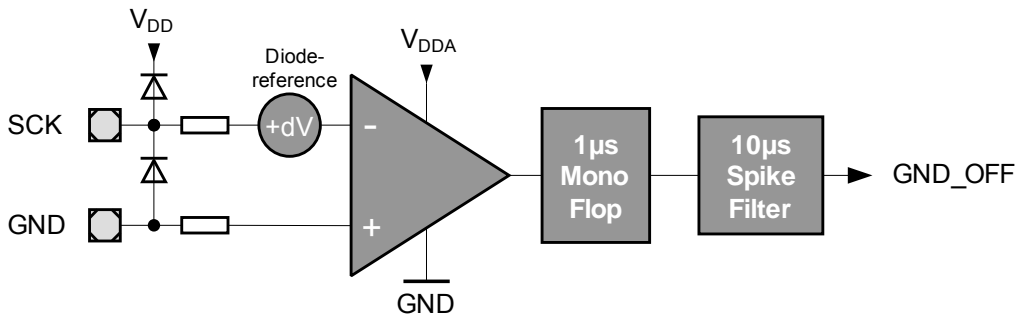


Figure 33 GND - off comparator

### 3.7.4 V<sub>DD</sub> - Off Comparator

The V<sub>DD</sub> - Off Comparator detects a disconnection of the VDD pin supply voltage. In this case, the TLE5012B is supplied by the SCK and CSQ input pins via the ESD structures. It activates the S\_VR bit.

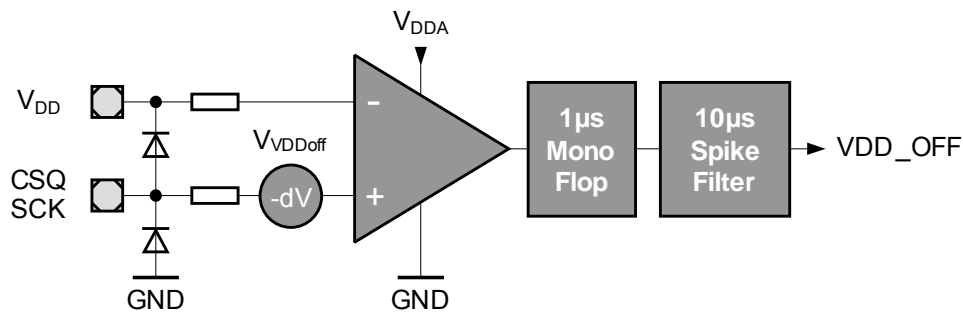


Figure 34 V<sub>DD</sub> - off comparator

## 4 Package Information

### 4.1 Package Parameters

Table 29 Package Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Thermal Resistance	$R_{thJA}$	-	150	200	K/W	Junction to Air <sup>1)</sup>
	$R_{thJC}$	-	-	75	K/W	Junction to Case
	$R_{thJL}$	-	-	85	K/W	Junction to Lead
Soldering Moisture Level		MSL 3				260°C
Lead Frame		Cu				
Plating		Sn 100%				> 7 $\mu$ m

1) according to Jecdec JESD51-7

### 4.2 Package Outline

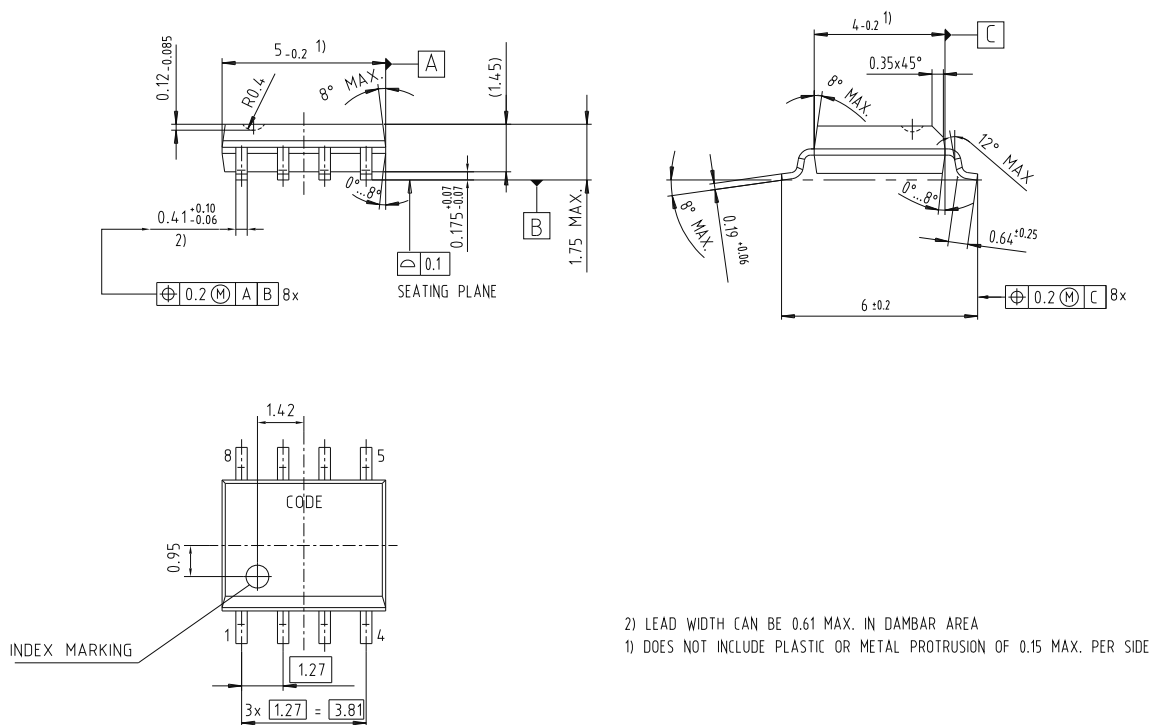


Figure 34 PG-DSO-8 package dimension

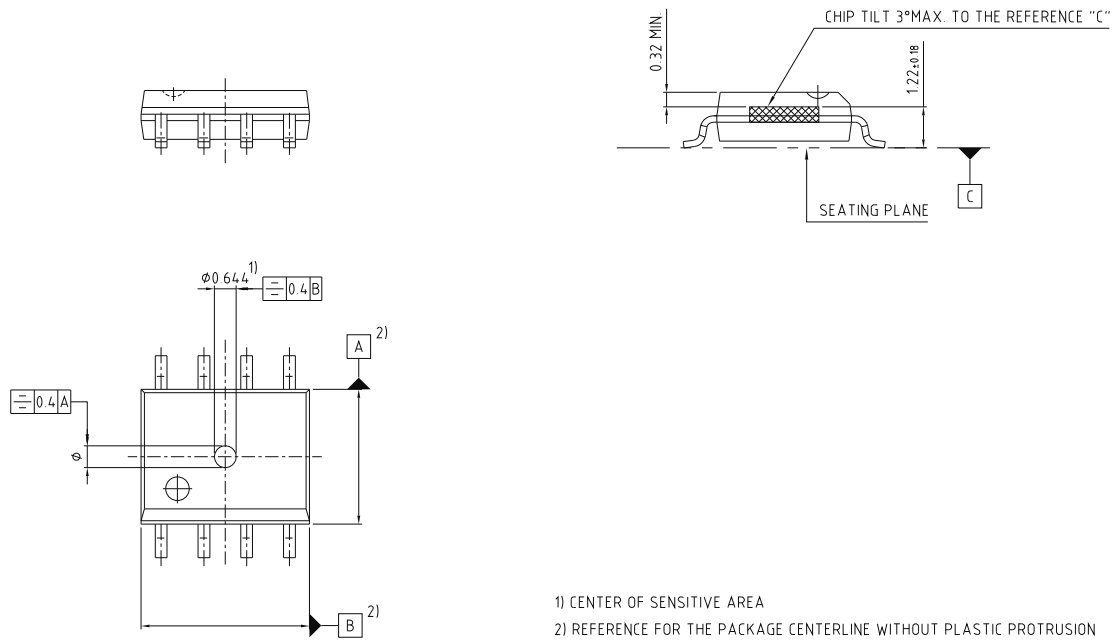


Figure 35 Position of sensing element

### 4.3 Footprint

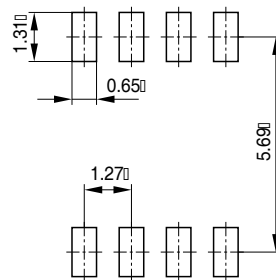


Figure 36 Footprint PG-DSO-8

### 4.4 Packing

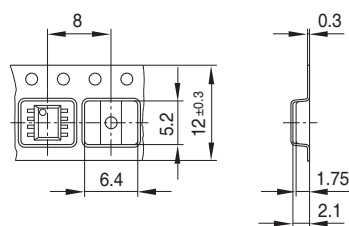


Figure 37 Tape and Reel

## 4.5 Marking

Position	Marking	Description
1st Line	012Bxxxx	See ordering table on <a href="#">Page 8</a>
2nd Line	xxx	Lot code
3rd Line	Gxxxx	G..green, 4-digit..date code

### Processing

*Note: For processing recommendations, please refer to Infineon's Notes on processing*

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