

# STM32F10xxx TIM1 application examples

# Introduction

This application note is intended to provide practical application examples of the STM32F10xxx TIM1 peripheral use.

This document, its associated firmware, and other such application notes are written to accompany the STM32F10xxx firmware library. These are available for download from the STMicroelectronics website: *www.st.com*.

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# 1 Generating 6 complementary PWM signals with dead time insertion using TIM1

## 1.1 Overview

This section provides a description of how to configure the TIM1 peripheral to generate three complementary TIM1 signals, to insert a determined dead-time value, to use the break feature and to lock the desired parameters.

# 1.2 Firmware description

The provided firmware includes the TIM1 driver that supports all TIM1 functionalities through a set of functions. An example of use for most of these functions is provided.

TIM1CLK is fixed to 72 MHz, the TIM1 prescaler is equal to 0x0, so the TIM1 counter clock operates at 72 MHz.

TIM1 is running at the TIM1 frequency, defined as follows:

TIM1 frequency = TIM1 counter clock / (TIM1\_Period + 1) = 1.098 KHz.

The three duty cycles are computed as shown below:

TIM1\_CH1 duty cycle = TIM1\_CCR1 / (TIM1\_Period + 1) = 50%

TIM1\_CH1N duty cycle = (TIM1\_Period – TIM1\_CCR1) / (TIM1\_Period + 1) = 50%

TIM1\_CH2 duty cycle = TIM1\_CCR2 / (TIM1\_Period + 1) = 25%

TIM1\_CH2N duty cycle = (TIM1\_Period - TIM1\_CCR2) / (TIM1\_Period + 1) = 75%

TIM1\_CH3 duty cycle = TIM1\_CCR3 / (TIM1\_Period + 1) = 12.5%

TIM1\_CH3N duty cycle = (TIM1\_Period - TIM1\_CCR3) / (TIM1\_Period + 1) = 87.5%

A dead time of  $1.62 \ \mu s$  is inserted between the different complementary signals, and LOCK level 1 is selected. The break input polarity is set to active high. The TIM1 waveform can be displayed using an oscilloscope.

This firmware is provided as *TIM1* example 1 in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

# 1.3 TIM1 output signal behavior

Connect the TIM1 pins to an oscilloscope:

- TIM1\_CH1 pin (PA8)
- TIM1\_CH1N pin (PB13)
- TIM1\_CH2 pin (PA9)
- TIM1\_CH2N pin (PB14)
- TIM1\_CH3 pin (PA10)
- TIM1\_CH3N pin (PB15)

Connect the TIM1 break pin, TIM1\_BKIN (PB12), to ground. To generate a break event, change the TIM1\_BKIN level from 0 V to 3.3 V. *Figure 1*, *Figure 2* and *Figure 3* show the output signals and *Figure 4* shows the dead-time insertion.





TIM1\_CH1 and TIM1\_CH1N output signals Figure 1.

Figure 2. TIM1\_CH2 and TIM1\_CH2N output signals







Figure 3. TIM1\_CH3 and TIM1\_CH3N output signals







# 2 Generating seven PWM signals using TIM1

### 2.1 Overview

This section provides a description of how to configure the TIM1 peripheral to generate seven PWM signals with four different duty cycles.

# 2.2 Firmware description

The provided firmware includes the TIM1 driver that supports all TIM1 functionalities through a set of functions. An example of use for most of these functions is provided.

TIM1CLK is fixed to 72 MHz, TIM1 prescaler is equal to 0x0, so the TIM1 counter clock frequency is 72 MHz.

TIM1 is running at the TIM1 frequency, defined as follows:

TIM1 frequency = TIM1CLK/(TIM1\_Period + 1) = 17.57 KHz.

The TIM1 CC1 register value is equal to 0x7FF, so TIM1\_CH1 and TIM1\_CH1N generate a PWM signal with a frequency of 17.57 KHz and a duty cycle equal to:

TIM1\_CH1 duty cycle = TIM1\_CCR1 /(TIM1\_Period + 1) = 50%.

The TIM1 CC2 register value is equal to 0x5FF, so TIM1\_CH2 and TIM1\_CH2N generate a PWM signal with a frequency of 17.57 KHz and a duty cycle equal to:

TIM1\_CH2 duty cycle = TIM1\_CCR2 / (TIM1\_Period + 1)= 37.5%.

The TIM1 CC3 register value is equal to 0x3FF, so TIM1\_CH3 and TIM1\_CH3N generate a PWM signal with a frequency of 17.57 KHz and a duty cycle equal to:

TIM1\_CH3 duty cycle = TIM1\_CCR3 / (TIM1\_Period + 1) = 25%.

The TIM1 CC4 register value is equal to 0x1FF, so TIM1\_CH4 generate a PWM signal with a frequency of 17.57 KHz and a duty cycle equal to:

TIM1\_CH4 duty cycle = TIM1\_CCR4 /  $(TIM1_Period + 1) = 12.5\%$ .

The TIM1 waveform can be displayed using an oscilloscope.

This firmware is provided as *TIM1 example 2* in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

## 2.3 TIM1 output signal behavior

Connect the TIM1 pins to an oscilloscope:

- TIM1\_CH1 pin (PA8)
- TIM1\_CH1N pin (PB13)
- TIM1\_CH2 pin (PA9)
- TIM1\_CH2N pin (PB14)
- TIM1\_CH3 pin (PA10)
- TIM1\_CH3N pin (PB15)
- TIM1\_CH4 pin (PA11)

		<b>,</b> 0.0s	20.0볼/ <b>Stop</b>	<b>₹ 2</b> 1.65V
0 <sub>6</sub> <b>DH4</b>				
05 <mark>0HBN</mark>				
13 CH2N				
D7		i l		
Duty(0 <sub>6</sub> ): 12.5%	Duty(04): 2	5.0%	) [Freq(0 <sub>0</sub> ): 1	7.57kHz
CH1 Free	Freq	Meas	Sectings	Thresholds

Figure 5. TIM1 output signals



# 3 Six-step PWM signal generation using TIM1

## 3.1 Overview

This section provides a description of how to configure the TIM1 peripheral to generate 6-steps of PWM signals.

# 3.2 Firmware description

The provided firmware includes the TIM1 driver that supports all TIM1 functionalities through a set of functions. An example of use for most of these functions is provided.

The STM32F10xxx TIM1 peripheral offers the possibility to program in advance the configuration for the next TIM1 output behavior (step) and change the configuration of all the channels at the same time. This operation is possible when the COM (commutation) event is used.

The COM event can be generated by software by setting the COM bit in the TIM1\_EGR register or by hardware (on TRGI rising edge).

In this example, a software COM event is generated every 100 ms: using the SysTick interrupt.

TIM1 is configured in Timing mode, each time a COM event occurs, a new TIM1 configuration is set in advance. *Table 1* describes the TIM1\_CHx channel states.

Channel	States					
Channel	Step1	Step2	Step3	Step4	Step5	Step6
TIM1_CH1	1	0	0	0	0	1
TIM1_CH1N	0	0	1	1	0	0
TIM1_CH2	0	0	0	1	1	0
TIM1_CH2N	1	1	0	0	0	0
TIM1_CH3	0	1	1	0	0	0
TIM1_CH3N	0	0	0	0	1	1

Table 1. TIM1\_CHx states

This firmware is provided as *TIM1 example 3* in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

# 3.3 TIM1 output signal behavior

Connect the TIM1 pins to an oscilloscope:

- TIM1\_CH1 pin (PA8)
- TIM1\_CH1N pin (PB13)
- TIM1\_CH2 pin (PA9)
- TIM1\_CH2N pin (PB14)
- TIM1\_CH3 pin (PA10)
- TIM1\_CH3N pin (PB15)

Connect the TIM1 break pin, TIM1\_BKIN (PB12), to ground. To generate a break event, change the TIM1\_BKIN pin level from 0 V to 3.3 V.

Figure 6. TIM1 output channel behavior

	. <sup>D</sup> 7 **	💶 🕞 💡 🕞 🕞	s 2.00s/ 3	Stop <b>£ 2</b> 1.65V
		-		
		-		
2 <b>CH2</b>		<u> </u>		
5 <mark>CH3N</mark>		-		
301211				
* <mark>2</mark> Measurement I	Menu	Į		
	Salaati Maa		Saddin	Thrachalda
CHEN	Period Per	ind Mea	s Settin	in resholds



# 4 TIM1 and TIMx synchronization in parallel mode

### 4.1 Overview

This section provides a description of how to synchronize TIM1 and timers TIMx (TIM3 and TIM4) in parallel mode.

# 4.2 Firmware description

The provided firmware includes the TIM1 driver that supports all TIM1 functionalities through a set of functions. An example of use for most of these functions is provided.

Timer synchronization in parallel mode:

- 1. TIM1 is configured as the master timer:
  - PWM mode is used
  - The TIM1 update event is used as the Trigger Output
- 2. TIM3 and TIM4 are slaves for TIM1,
  - PWM mode is used
  - ITR0 (internal trigger for TIM1) is used as the input trigger for both slaves
  - Gated mode is used, so starts and stops of slaves counters are controlled by the master trigger output signal (update event).

TIM1CLK is fixed to 72 MHz, the TIM1 Prescaler is equal to 0x0 so the TIM1 counter clock frequency is 72 MHz.

The master timer TIM1 is running at:

```
TIM1 frequency = TIM1 counter clock / (TIM1_Period + 1) = 281.250 KHz
```

and the duty cycle is equal to:

 $TIM1\_CCR1/(TIM1\_ARR + 1) = 50\%$ 

TIM3 is running at:

(TIM1 frequency)/ ((TIM3 period +1) × (Repetion\_Counter+1)) = 18.750 KHz

and the duty cycle is equal to:

TIM3\_CCR1/(TIM3\_ARR + 1) = 33.3%

The TIM4 is running at:

(TIM1 frequency)/ ((TIM4 period +1) × (Repetion\_Counter+1)) = 28.125 KHz

and the duty cycle equal to:

 $TIM4\_CCR1/(TIM4\_ARR + 1) = 50\%$ 

This firmware is provided as *TIM1* example 4 in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.



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#### 4.3 **TIM1** output signal behavior

To display the waveforms on the oscilloscope, connect the pins as follows:

- TIM1\_CH1 (PA8) •
- TIM3\_CH1 (PA6)
- TIM4\_CH1 (PB6)



#### Figure 7. TIM1\_CH1, TIM3\_CH1 and TIM1\_CH1 signals



# 5 Using DMA requests with TIM1

#### 5.1 Overview

This section provides a description of how to use DMA with TIM1 update request to transfer data from memory to TIM1 capture/compare register 3 (TIM\_CCR3).

# 5.2 Firmware description

The provided firmware includes the TIM1 driver that supports all TIM1 functionalities through a set of functions. An example of use for most of these functions is provided.

TIM1CLK is fixed to 72 MHz, the TIM1 prescaler is equal to 0x0 so the TIM1 counter clock frequency is 72 MHz.

The TIM1\_CH3 is configured to generate a complementary PWM signal with a frequency equal to:

TIM1 counter clock / (TIM1\_Period + 1) = 17.57 KHz

TIM1\_CH3 is configured to generate a complementary PWM signal with a frequency equal to 17.578 KHz and a variable duty cycle that is transferred from memory to the corresponding register after a specific number of update events.

The number of repetitive requests is defined by the TIM1 Repetition Counter, every 3 update requests, the TIM1\_CH3 duty cycle changes to the next new value defined by the SRC\_Buffer variable.

This firmware is provided as *TIM1 example 5* in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

# 5.3 TIM1 output signal behavior

To display the waveforms, connect the pins to an oscilloscope:

- TIM1\_CH3 (PA10)
- TIM1\_CH3N (PB15)





Figure 8. TIM1\_CH3 and TIM1\_CH3N output signal

# 6 Revision history

#### Table 2. Document revision history

Date	Revision	Changes
26-Jun-2007	1	Initial release.



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