Table 43: VLIO Timing

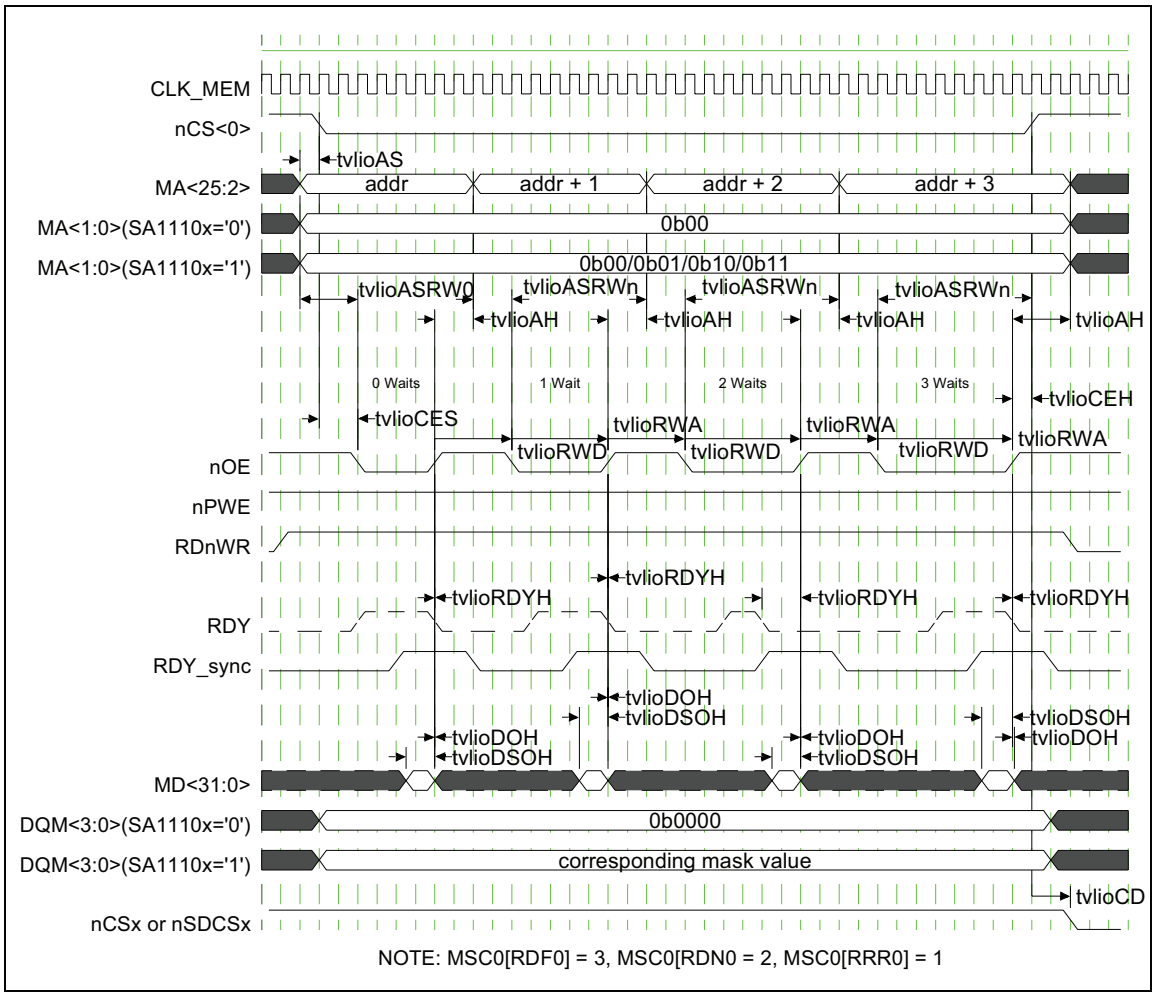
Symbols	Parameters	MIN	TYP	MAX[2]	Units[1]	Notes
tvlioAS	Address setup to nCS asserted	1	—	1	clk_mem	—
tvlioAH	Address hold from nPWE/nOE de-asserted	2	MSCx[RDN]	30	clk_mem	—
tvlioASRW0	Address setup to nPWE/nOE asserted (1st access)	3	—	3	clk_mem	—
tvlioASRWn	Address setup to nPWE/nOE asserted (next access(es))	2	MSCx[RDN]	30	clk_mem	—
tvlioCES	nCS setup to nPWE/nOE asserted	2	—	2	clk_mem	—
tvlioCEH	nCS hold from nPWE/nOE de-asserted	1	—	1	clk_mem	—
tvlioDSWH	MD/DQM setup (minimum) to nPWE de-asserted	5	MSCx[RDF]+2	32	clk_mem	—
tvlioDH	MD/DQM hold from nPWE de-asserted	2	MSCx[RDN]	30	clk_mem	—
tvlioDSOH	MD setup to address changing	1.5		—	clk_mem	—
tvlioDOH	MD hold from address changing	0		—	ns	—
tvlioRDYH	RDY hold from nPWE/nOE de-asserted	0	—	—	ns	—
tvlioRWA	nPWE/nOE assert period between writes	4	MSC[RDF]+1 + Waits	31 + Waits	clk_mem	—
tvlioRWD	nPWE/nOE de-asserted period between writes	4	MSCx[RDN*2]	60	clk_mem	3
tvlioCD	nCS de-asserted after a read/write to next nCS or nSDCS asserted (minimum)	1	MSCx[RRR]*2 + 1	15	clk_mem	—

NOTES:
1. Numbers shown as integer multiples of the CLK_MEM period are ideal. Actual numbers vary with pin-to-pin differences in loading and transition direction (rise or fall).
2. Maximum values reflect the register dynamic ranges.
3. Depending on the programmed value of MSC[RDN] and the clk_mem speed, this can be a significant amount of time. Processor does not drive the data bus during this time between transfers. If the VLIO does not drive the data bus during this time between transfers, the data bus is not driven for this period of time. If MSC[RDN] is programmed to 60 (which equals 60 CLK_MEM cycles), then the data bus could potentially not be driven for 30*2 = 60 CLK_MEM cycles.

6.4.6.1 Variable Latency I/O Read Timing

Figure 45 shows the timing for 32-bit variable-latency I/O (VLIO) memory reads. Table 43 lists the timing parameters used in these diagrams.

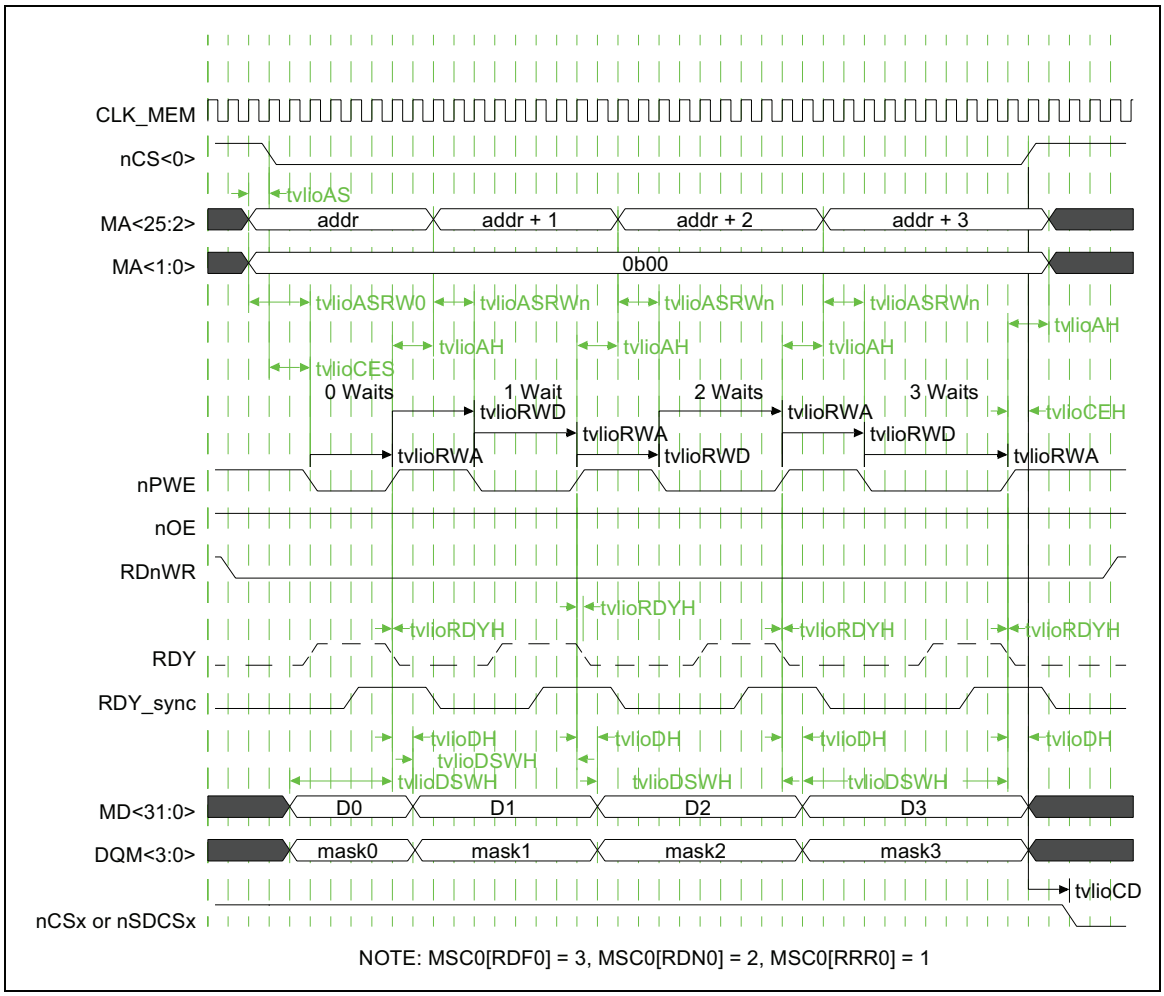
Figure 45: 32-Bit VLIO Read Timing



6.4.6.2 Variable-Latency I/O Write Timing

Figure 46 shows the timing for 32-bit VLIO memory writes. Table 43 list the timing parameters used in Figure 46.

Figure 46: 32-Bit VLIO Write Timing



6.4.7 Expansion-Card Interface Parameters and Timing Diagrams

The following sections describe the read/write parameters and timing diagrams for CompactFlash* and PC Card* (expansion card) memory interfaces with the memory controller.

Table 44 shows the timing parameters used in the timing diagrams, Figure 47 and Figure 48.

Note

Table 44 lists programmable register items. See the “Memory Controller” chapter in the *Marvell® PXA27x Processor Family Developer’s Manual* for register configurations for more information on these items.