ES_LPC4350/30/20/10 Rev A

Errata sheet LPC4350, LPC4330, LPC4320, LPC4310 Rev A

Rev. 1.2 — 1 February 2012 **Errata sheet**

Document information

Info	Content
Keywords	LPC4350FET256, LPC4350FET180, LPC4350FBD208, LPC4330FET256, LPC4330FET180, LPC4330FET100, LPC4330FBD144, LPC4320FET100, LPC4320FBD144, LPC4320FBD100, LPC4310FET100, LPC4310FBD144, Rev A errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
1.2	20120201	• Added OTP.1.
1.1	20120123	• Added ADC.1.
1	20120103	• Initial version.

Contact information

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1. Product identification

The LPC4350/30/20/10 devices (hereafter referred to as ‘LPC43x0’) typically have the following top-side marking:

LPC43x0xxxxxx

xxxxxxxx

xxxYYWWxR[x]

The last/second to last letter in the last line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC43x0:

Table 1. Device revision table

Revision identifier (R)	Revision description
‘A’	Initial device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
ADC.1	A/D Global Data register should not be used with burst mode or hardware triggering.	‘A’	Section 3.1
AES.1	AES decryption is not functional	‘A’	Section 3.2
BOOT.1	USB1 boot is not functional	‘A’	Section 3.3
MCPWM.1	MCPWM abort pin not functional	‘A’	Section 3.4
OTP.1	OTP ROM driver may not program boot source.	‘A’	Section 3.5
SPIFI.1	The ROM driver does not properly re-initialize the external flash device	‘A’	Section 3.6
USB0.1	USB0 and USB1 VBUS lines are not 5 V tolerant if part is unpowered	‘A’	Section 3.7

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Product version(s)	Detailed description
PWR.1	Deep sleep and Power-down mode consume more current than expected	‘A’	Section 4.1

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

3. Functional problems detail

3.1 ADC.1: A/D Global Data register should not be used with burst mode or hardware triggering

Introduction:

On the LPC4350/30/20/10, the START field and the BURST bit in the A/D control register specify whether A/D conversions are initiated via software command, in response to some hardware trigger, or continuously in burst ("hardware-scan") mode. Results of the ADC conversions can be read in one of two ways. One is to use the A/D Global Data Register to read all data from the ADC. Another is to use the individual A/D Channel Data Registers.

Problem:

If the burst mode is enabled (BURST bit set to ‘1’) or if hardware triggering is specified, the A/D conversion results read from the A/D Global Data register could be incorrect. If conversions are only launched directly by software command (BURST bit = '0' and START = ‘001’), the results read from the A/D Global Data register will be correct provided the previous result is read prior to launching a new conversion.

Work-around:

When using either burst mode or hardware triggering, the individual A/D Channel Data registers should be used instead of the A/D Global Data register to read the A/D conversion results.

3.2 AES.1: AES decryption is non-functional

Introduction:

The LPC43x0 contains a hardware-based AES security engine programmable through an on-chip API. This engine implements AES decryption with 128 bit keys.

Problem:

The hardware-based AES security engine is non-functional at this time.

Work-around:

We can produce parts with functional AES decryption engines for export to a limited number of countries. There is also an LPC43x0-S version product with fully functional AES encryption and decryption. Please contact sales for more information.

3.3 BOOT.1: USB1 boot is not functional

Introduction:

The internal ROM memory is used to store the boot code of the LPC43x0. After a reset, the ARM processor will start its code execution from this memory. The boot ROM memory includes the following features:

- …Boot from USB1….

Problem:

Boot from USB1 is not functional. This does not affect use of USB1 after bootup.

Work-around:

USB0 can be used to boot the part.

3.4 MCPWM.1: MCPWM Abort pin is not functional

Introduction:

The Motor Control PWM engine is optimized for three-phase AC and DC motor control applications, but can be used in many other applications that need timing, counting, capture, and comparison. The MCPWM contains a global Abort input that can force all of the channels into a passive state and cause an interrupt.

Problem:

The MCPWM Abort input is not functional.

Work-around:

The MCPWM Abort function can be emulated in software with the use of a non-maskable interrupt combined with an interrupt handler that shuts down the PWM. This will result in a small delay on the order of 50 main clock cycles or about 1/3 of a microsecond at 150 MHz. Alternatively, the State Configurable Timer (SCT) can be configured to implement MCPWM functionality including an Abort input. The SCT can respond to external inputs in one clock cycle.

3.5 OTP.1: OTP ROM driver may not program boot source

Introduction:

The LPC43x0 contains OTP memory which can configure the boot source, as well as a set of routines in ROM to program the boot source into OTP memory.

Problem:

There is a problem in the OTP boot source programming code in ROM which requires registers to be initialized in order to ensure successful boot source OTP programming.

Work-around:

1. Add this function to your program.

```
void OTP_fix(volatile unsigned dummy0,volatile unsigned dummy1,volatile unsigned
dummy2,volatile unsigned dummy3)
{
}
```

2. Call this function before calling otp_ProgBootSrc.

```
rval = otp_Init();
OTP_fix(0,0,0,0);
rval = otp_ProgBootSrc(OTP_BOOTSRC_SPIFI);
```

This will be fixed in the next boot ROM revision.

3.6 SPIFI.1: The ROM driver does not properly re-initialize the external serial flash device

Introduction:

The SPI Flash Interface (SPIFI) allows low-cost serial flash memories to be connected to the ARM Cortex-M3 processor with little performance penalty compared to parallel flash devices with higher pin count. SPIFI provides a memory-mapped area where the contents of the external serial flash memory appear.

Problem:

The ROM driver does not properly re-initialize the external serial flash device if it is already set up for no opcode mode. This affects use after a hardware reset, software reset, or watchdog timer reset. Booting from SPIFI is also affected.

Work-around:

Remove the external QSPI flash from no opcode mode before resetting the CPU. In addition, the driver will initialize the flash device if it is called a second time.

3.7 USB0.1: USB0 and USB1 VBUS lines are not 5 V tolerant if part is unpowered

Introduction:

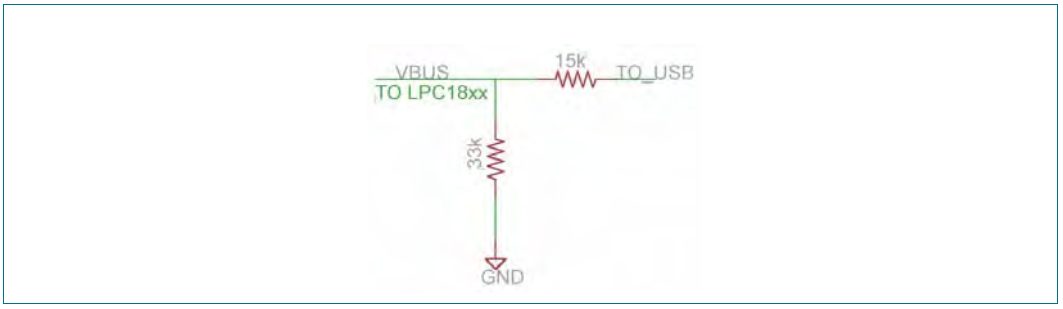
Universal Serial Bus (USB) is a standard protocol developed to connect several types of devices to each other in order to exchange data or for other purposes. USB hosts include a 5 V power supply for use by connected devices. One use case is for the LPC43x0 to implement a USB-powered USB device.

Problem:

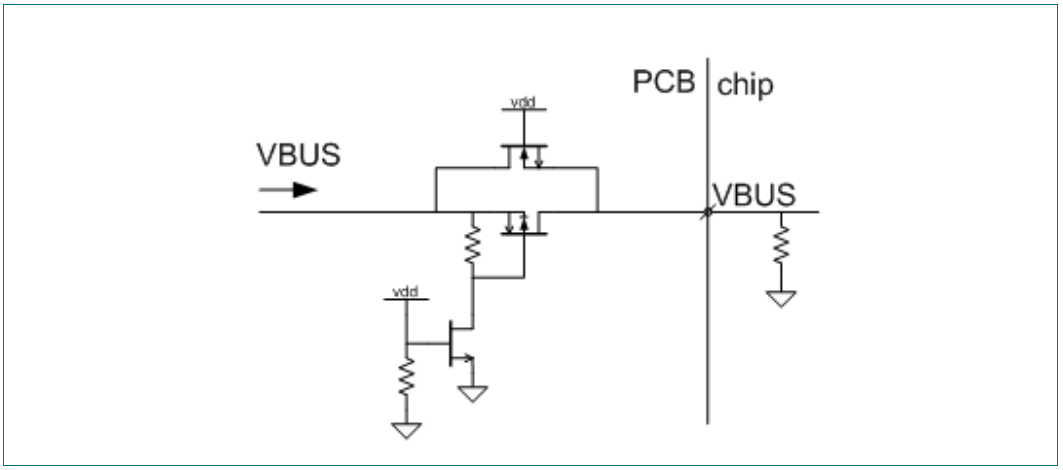
If USB0 or USB1 is used to implement a USB-powered USB device or OTG product, 5 V would be applied to the VBUS line on the LPC43x0 before the LPC43x0 was powered up. However, the VBUS line on the LPC43x0 5 V tolerant only when VDDIO is present.

Work-around:

For a simple USB device-only product, an external voltage divider is enough to prevent excess voltage from appearing on the VBUS line when USB is connected to an unpowered board. A schematic of a recommended voltage divider is shown below.



For a USB On-The-Go product, it is important to be able to detect the VBUS level and to charge and discharge VBUS. This requires adding active devices that disconnect the link when VDD is off.



4. AC/DC deviations detail

4.1 PWR.1: Deep sleep and Power-down modes consume more current than expected

Introduction:

The LPC43x0 contains several low-power modes. The PMC implements the control sequences to enable transitioning between different power modes and controls the power state of each peripheral.

Problem:

A design error results in about 15 µA higher current consumption during Deep Sleep and Power Down mode.

Work-around:

None.

5. Errata notes detail

5.1 n/a

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