DESCRIPTION

The 82S136 and 82S137 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S136 and 82S137 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

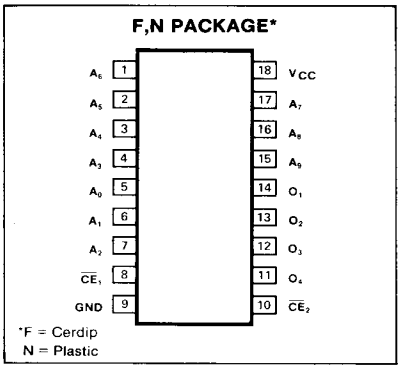
These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S136 and 82S137 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S136/137, F or N, and for the military temperature range (-55°C to +125°C) specify S82S136/137, F.

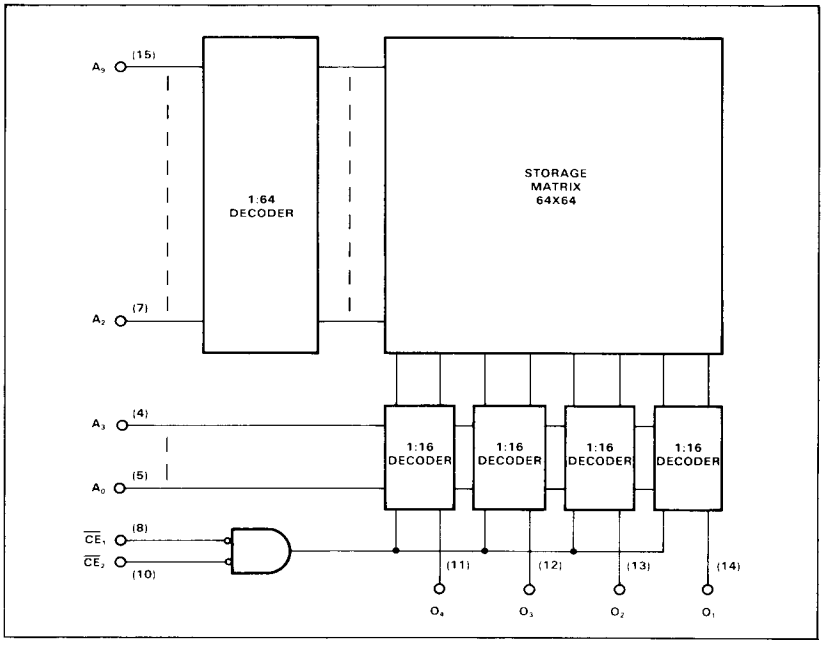
FEATURES

- **Address access time:**
  - **N82S136A/137A: 45ns max**
  - **N82S136/137: 60ns max**
  - **S82S136/137: 80ns max**
- **Power dissipation: .13mW/bit typ**
- **Input loading:**
  - **N82S136/137: -100μA max**
  - **S82S136/137: -150μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S136: Open collector**
  - **82S137: Tri-state**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S136)	+5.5	
V_O	Off-state (82S137)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S136/137	0 to +75	
	S82S136/137	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S136/137; N82S136A/137A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S136/137; S82S136A/137A: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1]	N82S136/137 N82S136A/137A			S82S136/137 S82S136A/137A			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S137)	$\overline{CE}$ = Low, I_{OUT} = -2mA, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S136)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Off-state (82S137)	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit (82S137)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			105	140		105	140	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

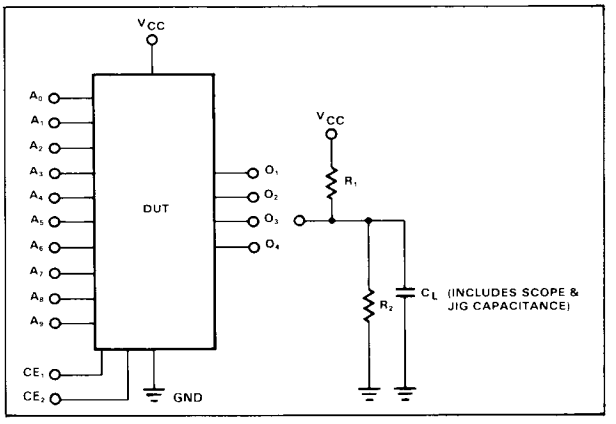
AC ELECTRICAL CHARACTERISTICS

R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF[1]
N82S136/137; N82S136A/137A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S136/137; S82S136A/137A: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

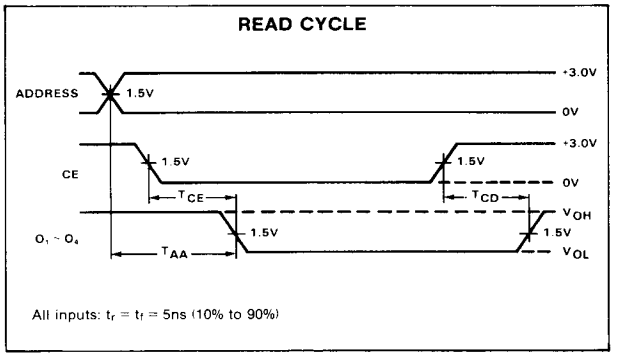
PARAMETER	TO	FROM	N82S136/137			S82S136/137			N82S136A/137A			S82S136A/137A			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time															ns
T_{AA}	Output	Address		40	60		40	80		30	45		30	70	
T_{CE}	Output	Chip enable		20	30		20	40		20	30		20	40	
Disable time															ns
T_{CD}	Output	Chip disable		20	30		20	40		20	30		20	40	

NOTES
1. Positive current is defined as into the terminal referenced.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 425 ± 75mA, Transient or steady state	8.5		9.0	V
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					µA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OPF}	Forced Output Voltage[3] (program)	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced Output Current (program)	V_{OPF} = +17 ± 1V	180		220	mA
T_R	Output pulse rise time		10			µs
t_p	$\overline{CE}$ programming pulse width		100		125	µs
t_D	Pulse sequence delay		5			µs
t_V	$\overline{CE}$ verify pulse width		1			µs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

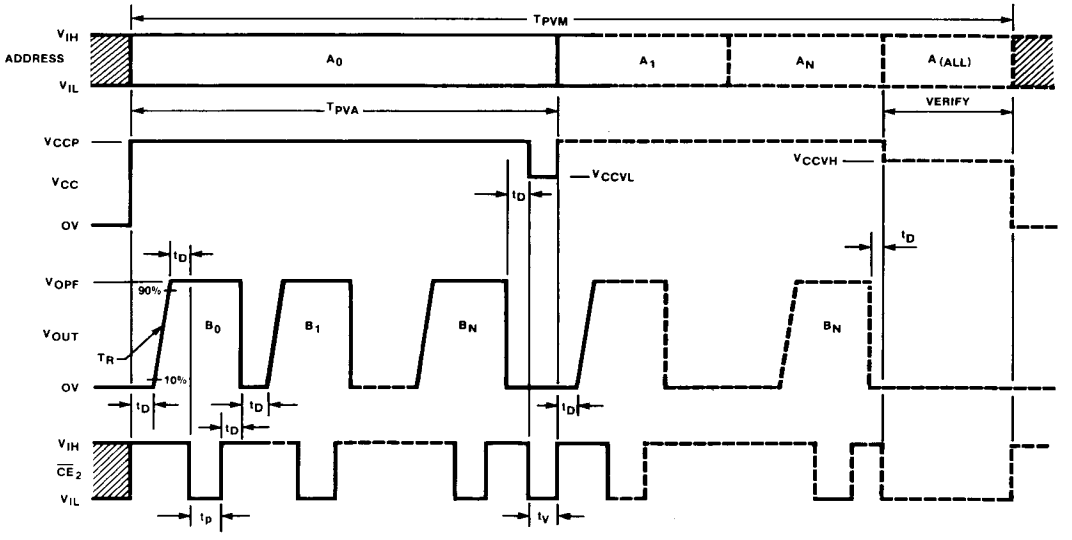
PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01µF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/µs, and 10µs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}_1$ = Low, $\overline{CE}_2$ = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.
4. After t_D delay, pulse the $\overline{CE}_2$ input to logic low for a time t_p.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}_2$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program, and verify all other address locations.
9. After t_D delay raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE}_2$, and cycling through all device addresses.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.