CIRCUIT DESCRIPTION

Frequency Configuration

Figure. 1 shows the frequency configuration of this transceiver. All modes operate in a double conversion while transmitting FM mode operates in a triple conversion and other modes operate in a double conversion while receiving

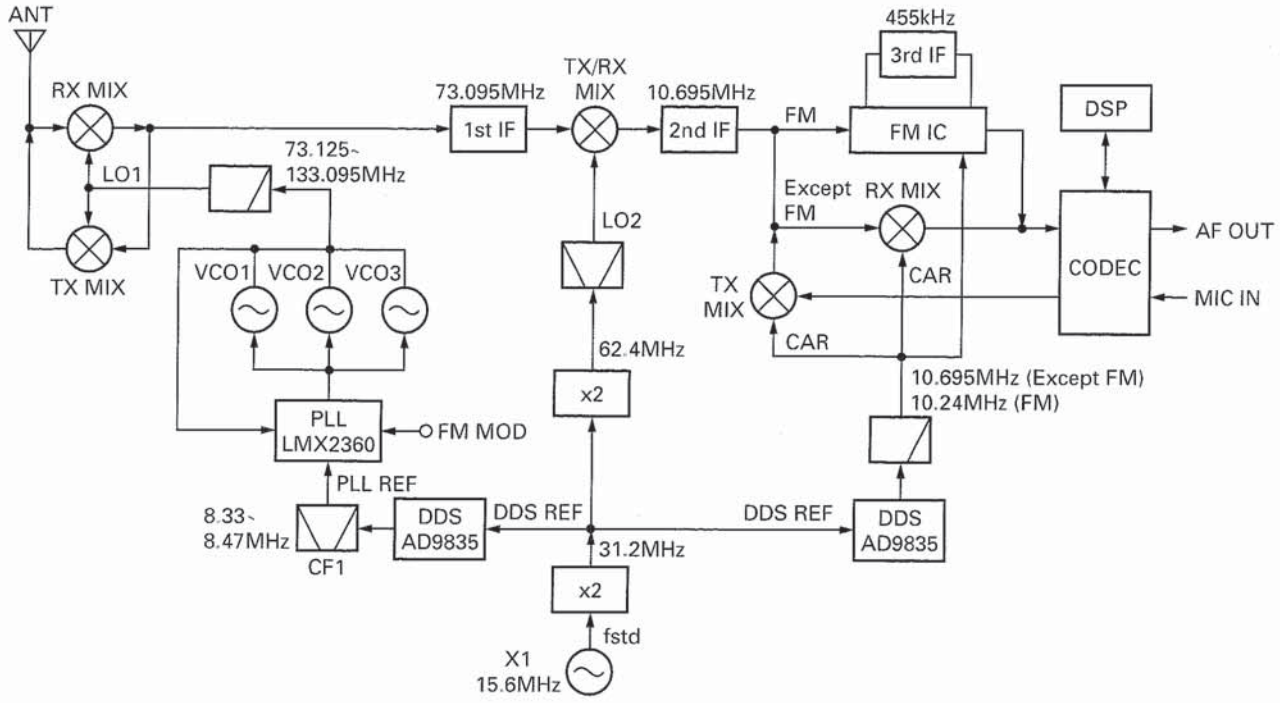

Fig. 1 Frequency configuration

Reference Signal Generator

The reference frequency (fstd), which is used to control the PLL frequency, oscillates at 15.6MHz in a crystal oscillation circuit (X1, Q1). This 15.6MHz signal passes through a buffer amplifier (Q4) and is doubled in a multiplier (Q5) to generate a 31.2 MHz signal. The 31.2MHz signal is used as the reference signal for the DDS (IC1) for the PLL reference signal of the first local oscillator (LO1) and the DDS (IC2) for a carrier (CAR).

The SO-3 (TCXO unit) is configured as an option in this transceiver, so that you can replace the crystal oscillation circuit (X1, Q1) with the SO-3. However, you must cut the R103 (0Ω) and R104 (0Ω) jumper wires to stop the operation of the crystal oscillation circuit (X1, Q1) when using the SO-3.

LO1/LO2/CAR

■ LO1 (the 1st local oscillator)

A frequency between 8.33MHz and 8.47MHz is output using the 31.2MHz signal as the reference signal in the DDS (IC1). The output signal passes through a ceramic filter (CF1) and enters into a PLL (IC3). This signal is divided into 1/8 (1/R) in the PLL and becomes the comparison frequency fø for the frequency between 1.041MHz and 1.058MHz

The VCOs (Q451, Q452, Q456) of LO1 oscillate between 73.125MHz and 133.095MHz. The oscillation output of these VCOs enter pin 6 of the PLL (IC3), then divides into 1/N in the PLL. The comparison frequency fø is compared with the frequency divided into 1/N by a phase comparator in the PLL, then locks the frequency to use it as the output frequency of LO1.

In the DDS (IC1), the output frequency (8.33MHz to 8.47MHz) is swept with $f_{DDS\ STEP}$ [Hz]=10 x R/N when the step is 10Hz or $f_{DDS\ STEP}$ [Hz]=1 x R/N when the step is 1Hz. Therefore, LO1 covers the frequency range of 73.125MHz to 133.095MHz with 10Hz or 1Hz steps.

The PLL output generated by the above-mentioned method is amplified at Q15 and passes through a band-pass filter with a cutoff switching circuit, an attenuator, and a low-pass filter, and is then sent to the RF unit (X44-327) as LO1.

■ LO2 (the 2nd local oscillator)

The 15.6MHz (reference frequency) signal passes through a buffer amplifier (Q4) and is doubled in a multiplier (Q5) to generate a 31.2MHz signal. The resistance of the 31.2MHz signal is distributed since it is used as the reference signal for each DDS (IC1, IC2). The 31.2MHz signal is doubled in a multipler (Q8, Q12) to generate a 62.4MHz signal.

The band-pass filter cuts the high harmonic of the 62.4MHz signal and the signal is sent to the RF unit (X44-327) as LO2.