OPERATION

1. Initialize the PEC to 000000000010000 (PEC is a 15-bit register group)
2. For each bit DIN coming into the PEC register group, set

   IN0 = DIN XOR PEC [14]

   IN3 = IN0 XOR PEC [2]

   IN4 = IN0 XOR PEC [3]

   IN7 = IN0 XOR PEC [6]

   IN8 = IN0 XOR PEC [7]

   IN10 = IN0 XOR PEC [9]

   IN14 = IN0 XOR PEC [13]
3. Update the 15-bit PEC as follows

   PEC [14] = IN14,

   PEC [13] = PEC [12],

   PEC [12] = PEC [11],

   PEC [11] = PEC [10],

   PEC [10] = IN10,

   PEC [9] = PEC [8],

   PEC [8] = IN8,

   PEC [7] = IN7,

   PEC [6] = PEC [5],

   PEC [5] = PEC [4],

   PEC [4] = IN4,

   PEC [3] = IN3,

   PEC [2] = PEC [1],

   PEC [1] = PEC [0],

   PEC [0] = IN0
4. Go back to step 2 until all the data is shifted. The final PEC (16 bits) is the 15-bit value in the PEC register with a 0 bit appended to its LSB

Figure 22 illustrates the algorithm described above. An example to calculate the PEC for a 16-bit word (0x0001) is listed in Table 24. The PEC for 0x0001 is computed as 0x3D6E after stuffing a 0 bit at the LSB. For longer data streams, the PEC is valid at the end of the last bit of data sent to the PEC register.

LTC6804 calculates PEC for any command or data received and compares it with the PEC following the command or data. The command or data is regarded as valid only if the PEC matches. LTC6804 also attaches the calculated PEC at the end of the data it shifts out. Table 25 shows the format of PEC while writing to or reading from LTC6804.

While writing any command to LTC6804, the command bytes CMD0 and CMD1 (See Table 32 and Table 33) and the PEC bytes PEC0 and PEC1 are sent on Port A in the following order:

CMD0, CMD1, PEC0, PEC1

After a broadcast write command to daisy-chained LTC6804-1 devices, data is sent to each device followed by the PEC. For example, when writing the configuration register group to two daisy-chained devices (primary device P, stacked device S), the data will be sent to the primary device on Port A in the following order:

CFGR0(S), … , CFGR5(S), PEC0(S), PEC1(S), CFGR0(P), …, CFGR5(P), PEC0(P), PEC1(P)

After a read command for daisy-chained devices, each device shifts out its data and the PEC that it computed for its data on Port A followed by the data received on Port B. For example, when reading status register group B from

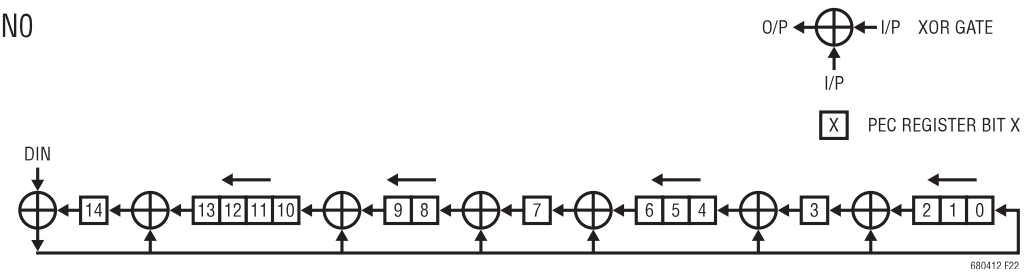

Figure 22. 15-Bit PEC Computation Circuit