Place & Route TRACE Report

```
Loading design for application trce from file top_impl1.ncd.
Design name: top
NCD version: 3.2
Vendor:      LATTICE
Device:      LFE3-35EA
Package:     FTBGA256
Performance: 7
Loading device for application trce from file 'ec5a71x74.nph' in environment: D:/Diamond2_0/diamond/2.0/ispfpga.
Package Status:                     Final          Version 1.60
Performance Hardware Data Status:   Final          Version 31.22
Setup and Hold Report

--------------------------------------------------------------------------------
```

Lattice TRACE Report - Setup, Version Diamond Version 2.0.0.154

```
Thu Feb 27 11:57:18 2014

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```

Report Information

```
------------------
Command line:    trce -v 10 -gt -sethld -sp 7 -sphld m -o top_impl1.twr top_impl1.ncd top_impl1.prf
Design file:     top_impl1.ncd
Preference file: top_impl1.prf
Device,speed:    LFE3-35EA,7
Report level:    verbose report, limited to 10 items per preference
--------------------------------------------------------------------------------
```

Preference Summary

- FREQUENCY NET "clk_125_c" 125.000000 MHz (0 errors)

```
            4096 items scored, 0 timing errors detected.
Report:  125.960MHz is the maximum frequency for this preference.
```

- FREQUENCY NET "can_clk_c" 25.000000 MHz (0 errors)

```
            4096 items scored, 0 timing errors detected.
Report:   34.524MHz is the maximum frequency for this preference.
```

- FREQUENCY NET "uart_clk_c" 25.000000 MHz (0 errors)

```
            4096 items scored, 0 timing errors detected.
Report:   34.341MHz is the maximum frequency for this preference.
```

- FREQUENCY NET "pcie/pclk" 250.000000 MHz (0 errors)

```
            987 items scored, 0 timing errors detected.
Report:  279.174MHz is the maximum frequency for this preference.
```

- FREQUENCY NET "pcie/u1_pcs_pipe/ff_rx_fclk_0" 250.000000 MHz (0 errors)

```
            1 item scored, 0 timing errors detected.
Report:  412.201MHz is the maximum frequency for this preference.
```

- BLOCK PATH FROM PORT "rstn" (0 errors)

```
            119 items scored, 0 timing errors detected.
```

- BLOCK PATH TO PORT "OUT*" (0 errors)

```
            0 items scored, 0 timing errors detected.
```

- BLOCK PATH FROM PORT "INP*" (0 errors)

```
            16 items scored, 0 timing errors detected.
```

- BLOCK PATH FROM PORT "SRAM_A*" (0 errors)

```
            0 items scored, 0 timing errors detected.
```

- BLOCK PATH TO PORT "LED*" (0 errors)

```
            8 items scored, 0 timing errors detected.
```

- BLOCK PATH FROM CELL "*ctc_reset_chx*" (0 errors)

```
            14 items scored, 0 timing errors detected.
```

- MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*cnt_done_nfts_rx*" 2.000000 X (0 errors)

```
            214 items scored, 0 timing errors detected.
```

- MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*ltssm_nfts_rx_skp*" 2.000000 X (0 errors)

```
            244 items scored, 0 timing errors detected.
```

- MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr*" 6.000000 ns (0 errors)

```
            33 items scored, 0 timing errors detected.
Report:  535.619MHz is the maximum frequency for this preference.
```

- MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr*" 6.000000 ns (0 errors)

```
            147 items scored, 0 timing errors detected.
Report:  279.877MHz is the maximum frequency for this preference.
```

- MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr*" 6.000000 ns (0 errors)

```
            14 items scored, 0 timing errors detected.
Report:  739.098MHz is the maximum frequency for this preference.
```

- MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr*" 6.000000 ns (0 errors)

```
            18 items scored, 0 timing errors detected.
Report:  536.769MHz is the maximum frequency for this preference.
```

- MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data*" 6.000000 ns (0 errors)

```
            16 items scored, 0 timing errors detected.
Report:  416.320MHz is the maximum frequency for this preference.
```

- MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl*" 6.000000 ns (0 errors)

```
            2 items scored, 0 timing errors detected.
Report:  410.846MHz is the maximum frequency for this preference.

34 potential circuit loops found in timing analysis.
BLOCK ASYNCPATHS
BLOCK RESETPATHS
BLOCK JTAG PATHS
--------------------------------------------------------------------------------



================================================================================
Preference: FREQUENCY NET "clk_125_c" 125.000000 MHz ;
            4096 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.061ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_tlc/intf/wb_adr_o_1[10]  (from clk_125_c +)
   Destination:    FF         Data in       gpio_led_out_1io[7]  (to clk_125_c +)

   Delay:               7.797ns  (14.0% logic, 86.0% route), 6 logic levels.

 Constraint Details:

     7.797ns physical path delay wb_tlc/intf/SLICE_4258 to LED1Gn_MGIOL meets
     8.000ns delay constraint less
    -0.044ns skew and
     0.186ns CE_SET requirement (totaling 7.858ns) by 0.061ns

IOL_T68A attributes: FINE=FDEL0

 Physical Path Details:

     Data path wb_tlc/intf/SLICE_4258 to LED1Gn_MGIOL:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R40C29B.CLK to     R40C29B.Q0 wb_tlc/intf/SLICE_4258 (from clk_125_c)
ROUTE         5     0.673     R40C29B.Q0 to     R40C30C.A0 pcie_adr[10]
CTOF_DEL    ---     0.164     R40C30C.A0 to     R40C30C.F0 wb_arb/SLICE_8881
ROUTE         1     0.577     R40C30C.F0 to     R39C29B.D1 wb_arb/un4_s5_sellto23_0_0_a2_1_4
CTOF_DEL    ---     0.164     R39C29B.D1 to     R39C29B.F1 wb_arb/SLICE_7326
ROUTE         4     1.037     R39C29B.F1 to     R33C25D.C1 wb_arb/N_844
CTOF_DEL    ---     0.164     R33C25D.C1 to     R33C25D.F1 SLICE_7317
ROUTE        12     0.350     R33C25D.F1 to     R33C25D.D0 N_846
CTOF_DEL    ---     0.164     R33C25D.D0 to     R33C25D.F0 SLICE_7317
ROUTE        10     1.227     R33C25D.F0 to     R31C43D.C1 gpio/N_855
CTOF_DEL    ---     0.164     R31C43D.C1 to     R31C43D.F1 gpio/SLICE_7315
ROUTE         8     2.838     R31C43D.F1 to    IOL_T68A.CE gpio.led_out_1_sqmuxa (to clk_125_c)
                  --------
                    7.797   (14.0% logic, 86.0% route), 6 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4258:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R40C29B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.
```

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to LED1Gn_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.459 *FF_TX_H_CLK_0 to   IOL_T68A.CLK clk_125_c
                    ----
                     1.459   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.061ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   wb_tlc/intf/wb_adr_o_1[10] (from clk_125_c +)
   Destination: FF   Data in   gpio_led_out_1io[6] (to clk_125_c +)

   Delay: 7.797ns (14.0% logic, 86.0% route), 6 logic levels.

 Constraint Details:

     7.797ns physical path delay wb_tlc/intf/SLICE_4258 to LED1Rn_MGIOL meets
     8.000ns delay constraint less
    -0.044ns skew and
     0.186ns CE_SET requirement (totaling 7.858ns) by 0.061ns

IOL_T68B attributes: FINE=FDEL0

 Physical Path Details:

     Data path wb_tlc/intf/SLICE_4258 to LED1Rn_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R40C29B.CLK to   R40C29B.Q0 wb_tlc/intf/SLICE_4258 (from clk_125_c)
ROUTE   5   0.673   R40C29B.Q0 to   R40C30C.A0 pcie_adr[10]
CTOF_DEL   ---   0.164   R40C30C.A0 to   R40C30C.F0 wb_arb/SLICE_8881
ROUTE   1   0.577   R40C30C.F0 to   R39C29B.D1 wb_arb/un4_s5_sellto23_0_0_a2_1_4
CTOF_DEL   ---   0.164   R39C29B.D1 to   R39C29B.F1 wb_arb/SLICE_7326
ROUTE   4   1.037   R39C29B.F1 to   R33C25D.C1 wb_arb/N_844
CTOF_DEL   ---   0.164   R33C25D.C1 to   R33C25D.F1 SLICE_7317
ROUTE   12   0.350   R33C25D.F1 to   R33C25D.D0 N_846
CTOF_DEL   ---   0.164   R33C25D.D0 to   R33C25D.F0 SLICE_7317
ROUTE   10   1.227   R33C25D.F0 to   R31C43D.C1 gpio/N_855
CTOF_DEL   ---   0.164   R31C43D.C1 to   R31C43D.F1 gpio/SLICE_7315
ROUTE   8   2.838   R31C43D.F1 to   IOL_T68B.CE gpio.led_out_1_sqmuxa (to clk_125_c)

                     7.797   (14.0% logic, 86.0% route), 6 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4258:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R40C29B.CLK clk_125_c
                    ----
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to LED1Rn_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.459 *FF_TX_H_CLK_0 to   IOL_T68B.CLK clk_125_c
                    ----
                     1.459   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.108ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   wb_tlc/intf/wb_adr_o_1[7] (from clk_125_c +)
   Destination: FF   Data in   gpio_led_out_1io[7] (to clk_125_c +)

   Delay: 7.750ns (14.1% logic, 85.9% route), 6 logic levels.

 Constraint Details:

     7.750ns physical path delay wb_tlc/intf/SLICE_4256 to LED1Gn_MGIOL meets
     8.000ns delay constraint less
    -0.044ns skew and
     0.186ns CE_SET requirement (totaling 7.858ns) by 0.108ns

IOL_T68A attributes: FINE=FDEL0

 Physical Path Details:

     Data path wb_tlc/intf/SLICE_4256 to LED1Gn_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R40C32B.CLK to   R40C32B.Q1 wb_tlc/intf/SLICE_4256 (from clk_125_c)
ROUTE   5   0.626   R40C32B.Q1 to   R40C30C.B0 pcie_adr[7]
CTOF_DEL   ---   0.164   R40C30C.B0 to   R40C30C.F0 wb_arb/SLICE_8881
ROUTE   1   0.577   R40C30C.F0 to   R39C29B.D1 wb_arb/un4_s5_sellto23_0_0_a2_1_4
CTOF_DEL   ---   0.164   R39C29B.D1 to   R39C29B.F1 wb_arb/SLICE_7326
ROUTE   4   1.037   R39C29B.F1 to   R33C25D.C1 wb_arb/N_844
CTOF_DEL   ---   0.164   R33C25D.C1 to   R33C25D.F1 SLICE_7317
ROUTE   12   0.350   R33C25D.F1 to   R33C25D.D0 N_846
CTOF_DEL   ---   0.164   R33C25D.D0 to   R33C25D.F0 SLICE_7317
ROUTE   10   1.227   R33C25D.F0 to   R31C43D.C1 gpio/N_855
CTOF_DEL   ---   0.164   R31C43D.C1 to   R31C43D.F1 gpio/SLICE_7315
ROUTE   8   2.838   R31C43D.F1 to   IOL_T68A.CE gpio.led_out_1_sqmuxa (to clk_125_c)

                     7.750   (14.1% logic, 85.9% route), 6 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4256:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R40C32B.CLK clk_125_c
                    ----
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to LED1Gn_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.459 *FF_TX_H_CLK_0 to   IOL_T68A.CLK clk_125_c
                    ----
                     1.459   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.108ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   wb_tlc/intf/wb_adr_o_1[7] (from clk_125_c +)
   Destination: FF   Data in   gpio_led_out_1io[6] (to clk_125_c +)

   Delay: 7.750ns (14.1% logic, 85.9% route), 6 logic levels.

 Constraint Details:

     7.750ns physical path delay wb_tlc/intf/SLICE_4256 to LED1Rn_MGIOL meets
     8.000ns delay constraint less
    -0.044ns skew and
     0.186ns CE_SET requirement (totaling 7.858ns) by 0.108ns

IOL_T68B attributes: FINE=FDEL0

 Physical Path Details:

     Data path wb_tlc/intf/SLICE_4256 to LED1Rn_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R40C32B.CLK to   R40C32B.Q1 wb_tlc/intf/SLICE_4256 (from clk_125_c)
ROUTE   5   0.626   R40C32B.Q1 to   R40C30C.B0 pcie_adr[7]
CTOF_DEL   ---   0.164   R40C30C.B0 to   R40C30C.F0 wb_arb/SLICE_8881
ROUTE   1   0.577   R40C30C.F0 to   R39C29B.D1 wb_arb/un4_s5_sellto23_0_0_a2_1_4
CTOF_DEL   ---   0.164   R39C29B.D1 to   R39C29B.F1 wb_arb/SLICE_7326
ROUTE   4   1.037   R39C29B.F1 to   R33C25D.C1 wb_arb/N_844
CTOF_DEL   ---   0.164   R33C25D.C1 to   R33C25D.F1 SLICE_7317
ROUTE   12   0.350   R33C25D.F1 to   R33C25D.D0 N_846
CTOF_DEL   ---   0.164   R33C25D.D0 to   R33C25D.F0 SLICE_7317
ROUTE   10   1.227   R33C25D.F0 to   R31C43D.C1 gpio/N_855
CTOF_DEL   ---   0.164   R31C43D.C1 to   R31C43D.F1 gpio/SLICE_7315
ROUTE   8   2.838   R31C43D.F1 to   IOL_T68B.CE gpio.led_out_1_sqmuxa (to clk_125_c)

                     7.750   (14.1% logic, 85.9% route), 6 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4256:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R40C32B.CLK clk_125_c
                    ----

                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to LED1Rn_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.459 *FF_TX_H_CLK_0 to   IOL_T68B.CLK clk_125_c
                    ----
                    1.459   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.178ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   wb_tlc/intf/wb_adr_o_1[9] (from clk_125_c +)
   Destination: FF   Data in   gpio_led_out_1io[7] (to clk_125_c +)

   Delay: 7.680ns (14.3% logic, 85.7% route), 6 logic levels.

 Constraint Details:

      7.680ns physical path delay wb_tlc/intf/SLICE_4257 to LED1Gn_MGIOL meets
      8.000ns delay constraint less
     -0.044ns skew and
      0.186ns CE_SET requirement (totaling 7.858ns) by 0.178ns

IOL_T68A attributes: FINE=FDEL0

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_4257 to LED1Gn_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R40C29C.CLK to   R40C29C.Q1 wb_tlc/intf/SLICE_4257 (from clk_125_c)
ROUTE   5   0.556   R40C29C.Q1 to   R40C30C.C0 pcie_adr[9]
CTOF_DEL   ---   0.164   R40C30C.C0 to   R40C30C.F0 wb_arb/SLICE_8881
ROUTE   1   0.577   R40C30C.F0 to   R39C29B.D1 wb_arb/un4_s5_sellto23_0_0_a2_1_4
CTOF_DEL   ---   0.164   R39C29B.D1 to   R39C29B.F1 wb_arb/SLICE_7326
ROUTE   4   1.037   R39C29B.F1 to   R33C25D.C1 wb_arb/N_844
CTOF_DEL   ---   0.164   R33C25D.C1 to   R33C25D.F1 SLICE_7317
ROUTE   12   0.350   R33C25D.F1 to   R33C25D.D0 N_846
CTOF_DEL   ---   0.164   R33C25D.D0 to   R33C25D.F0 SLICE_7317
ROUTE   10   1.227   R33C25D.F0 to   R31C43D.C1 gpio/N_855
CTOF_DEL   ---   0.164   R31C43D.C1 to   R31C43D.F1 gpio/SLICE_7315
ROUTE   8   2.838   R31C43D.F1 to   IOL_T68A.CE gpio.led_out_1_sqmuxa (to clk_125_c)

                    7.680   (14.3% logic, 85.7% route), 6 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4257:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R40C29C.CLK clk_125_c
                    ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to LED1Gn_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.459 *FF_TX_H_CLK_0 to   IOL_T68A.CLK clk_125_c
                    ----
                    1.459   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.178ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   wb_tlc/intf/wb_adr_o_1[9] (from clk_125_c +)
   Destination: FF   Data in   gpio_led_out_1io[6] (to clk_125_c +)

   Delay: 7.680ns (14.3% logic, 85.7% route), 6 logic levels.

 Constraint Details:

      7.680ns physical path delay wb_tlc/intf/SLICE_4257 to LED1Rn_MGIOL meets
      8.000ns delay constraint less
     -0.044ns skew and
      0.186ns CE_SET requirement (totaling 7.858ns) by 0.178ns

IOL_T68B attributes: FINE=FDEL0

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_4257 to LED1Rn_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R40C29C.CLK to   R40C29C.Q1 wb_tlc/intf/SLICE_4257 (from clk_125_c)
ROUTE   5   0.556   R40C29C.Q1 to   R40C30C.C0 pcie_adr[9]
CTOF_DEL   ---   0.164   R40C30C.C0 to   R40C30C.F0 wb_arb/SLICE_8881
ROUTE   1   0.577   R40C30C.F0 to   R39C29B.D1 wb_arb/un4_s5_sellto23_0_0_a2_1_4
CTOF_DEL   ---   0.164   R39C29B.D1 to   R39C29B.F1 wb_arb/SLICE_7326
ROUTE   4   1.037   R39C29B.F1 to   R33C25D.C1 wb_arb/N_844
CTOF_DEL   ---   0.164   R33C25D.C1 to   R33C25D.F1 SLICE_7317
ROUTE   12   0.350   R33C25D.F1 to   R33C25D.D0 N_846
CTOF_DEL   ---   0.164   R33C25D.D0 to   R33C25D.F0 SLICE_7317
ROUTE   10   1.227   R33C25D.F0 to   R31C43D.C1 gpio/N_855
CTOF_DEL   ---   0.164   R31C43D.C1 to   R31C43D.F1 gpio/SLICE_7315
ROUTE   8   2.838   R31C43D.F1 to   IOL_T68B.CE gpio.led_out_1_sqmuxa (to clk_125_c)

                    7.680   (14.3% logic, 85.7% route), 6 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4257:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R40C29C.CLK clk_125_c
                    ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to LED1Rn_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.459 *FF_TX_H_CLK_0 to   IOL_T68B.CLK clk_125_c
                    ----
                    1.459   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.185ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   wb_tlc/intf/wb_adr_o_1[10] (from clk_125_c +)
   Destination: FF   Data in   gpio_outp_iio[7] (to clk_125_c +)

   Delay: 7.673ns (14.3% logic, 85.7% route), 6 logic levels.

 Constraint Details:

      7.673ns physical path delay wb_tlc/intf/SLICE_4258 to OUT_7_MGIOL meets
      8.000ns delay constraint less
     -0.044ns skew and
      0.186ns CE_SET requirement (totaling 7.858ns) by 0.185ns

IOL_T64A attributes: FINE=FDEL0

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_4258 to OUT_7_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R40C29B.CLK to   R40C29B.Q0 wb_tlc/intf/SLICE_4258 (from clk_125_c)
ROUTE   5   0.673   R40C29B.Q0 to   R40C30C.A0 pcie_adr[10]
CTOF_DEL   ---   0.164   R40C30C.A0 to   R40C30C.F0 wb_arb/SLICE_8881
ROUTE   1   0.577   R40C30C.F0 to   R39C29B.D1 wb_arb/un4_s5_sellto23_0_0_a2_1_4
CTOF_DEL   ---   0.164   R39C29B.D1 to   R39C29B.F1 wb_arb/SLICE_7326
ROUTE   4   1.037   R39C29B.F1 to   R33C25D.C1 wb_arb/N_844
CTOF_DEL   ---   0.164   R33C25D.C1 to   R33C25D.F1 SLICE_7317
ROUTE   12   0.875   R33C25D.F1 to   R31C37C.D1 N_846
CTOF_DEL   ---   0.164   R31C37C.D1 to   R31C37C.F1 gpio/SLICE_7316
ROUTE   11   0.350   R31C37C.F1 to   R31C37C.D0 gpio/N_850
CTOF_DEL   ---   0.164   R31C37C.D0 to   R31C37C.F0 gpio/SLICE_7316
ROUTE   8   3.066   R31C37C.F0 to   IOL_T64A.CE gpio.outp_0_sqmuxa (to clk_125_c)

                    7.673   (14.3% logic, 85.7% route), 6 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4258:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R40C29B.CLK clk_125_c

                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to OUT_7_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.459 *FF_TX_H_CLK_0 to   IOL_T64A.CLK clk_125_c
                  ----
                    1.459   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.232ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   wb_tlc/intf/wb_adr_o_1[7] (from clk_125_c +)
   Destination: FF   Data in   gpio_outp_iio[7] (to clk_125_c +)

   Delay: 7.626ns (14.4% logic, 85.6% route), 6 logic levels.

 Constraint Details:

     7.626ns physical path delay wb_tlc/intf/SLICE_4256 to OUT_7_MGIOL meets
     8.000ns delay constraint less
    -0.044ns skew and
     0.186ns CE_SET requirement (totaling 7.858ns) by 0.232ns

IOL_T64A attributes: FINE=FDEL0

 Physical Path Details:

     Data path wb_tlc/intf/SLICE_4256 to OUT_7_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R40C32B.CLK to   R40C32B.Q1 wb_tlc/intf/SLICE_4256 (from clk_125_c)
ROUTE   5   0.626   R40C32B.Q1 to   R40C30C.B0 pcie_adr[7]
CTOF_DEL   ---   0.164   R40C30C.B0 to   R40C30C.F0 wb_arb/SLICE_8881
ROUTE   1   0.577   R40C30C.F0 to   R39C29B.D1 wb_arb/un4_s5_sellto23_0_0_a2_1_4
CTOF_DEL   ---   0.164   R39C29B.D1 to   R39C29B.F1 wb_arb/SLICE_7326
ROUTE   4   1.037   R39C29B.F1 to   R33C25D.C1 wb_arb/N_844
CTOF_DEL   ---   0.164   R33C25D.C1 to   R33C25D.F1 SLICE_7317
ROUTE   12   0.875   R33C25D.F1 to   R31C37C.D1 N_846
CTOF_DEL   ---   0.164   R31C37C.D1 to   R31C37C.F1 gpio/SLICE_7316
ROUTE   11   0.350   R31C37C.F1 to   R31C37C.D0 gpio/N_850
CTOF_DEL   ---   0.164   R31C37C.D0 to   R31C37C.F0 gpio/SLICE_7316
ROUTE   8   3.066   R31C37C.F0 to   IOL_T64A.CE gpio.outp_0_sqmuxa (to clk_125_c)

                    7.626   (14.4% logic, 85.6% route), 6 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4256:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R40C32B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to OUT_7_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.459 *FF_TX_H_CLK_0 to   IOL_T64A.CLK clk_125_c
                  ----
                    1.459   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.302ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   wb_tlc/intf/wb_adr_o_1[9] (from clk_125_c +)
   Destination: FF   Data in   gpio_outp_iio[7] (to clk_125_c +)

   Delay: 7.556ns (14.5% logic, 85.5% route), 6 logic levels.

 Constraint Details:

     7.556ns physical path delay wb_tlc/intf/SLICE_4257 to OUT_7_MGIOL meets
     8.000ns delay constraint less
    -0.044ns skew and
     0.186ns CE_SET requirement (totaling 7.858ns) by 0.302ns

IOL_T64A attributes: FINE=FDEL0

 Physical Path Details:

     Data path wb_tlc/intf/SLICE_4257 to OUT_7_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R40C29C.CLK to   R40C29C.Q1 wb_tlc/intf/SLICE_4257 (from clk_125_c)
ROUTE   5   0.556   R40C29C.Q1 to   R40C30C.C0 pcie_adr[9]
CTOF_DEL   ---   0.164   R40C30C.C0 to   R40C30C.F0 wb_arb/SLICE_8881
ROUTE   1   0.577   R40C30C.F0 to   R39C29B.D1 wb_arb/un4_s5_sellto23_0_0_a2_1_4
CTOF_DEL   ---   0.164   R39C29B.D1 to   R39C29B.F1 wb_arb/SLICE_7326
ROUTE   4   1.037   R39C29B.F1 to   R33C25D.C1 wb_arb/N_844
CTOF_DEL   ---   0.164   R33C25D.C1 to   R33C25D.F1 SLICE_7317
ROUTE   12   0.875   R33C25D.F1 to   R31C37C.D1 N_846
CTOF_DEL   ---   0.164   R31C37C.D1 to   R31C37C.F1 gpio/SLICE_7316
ROUTE   11   0.350   R31C37C.F1 to   R31C37C.D0 gpio/N_850
CTOF_DEL   ---   0.164   R31C37C.D0 to   R31C37C.F0 gpio/SLICE_7316
ROUTE   8   3.066   R31C37C.F0 to   IOL_T64A.CE gpio.outp_0_sqmuxa (to clk_125_c)

                    7.556   (14.5% logic, 85.5% route), 6 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4257:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R40C29C.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to OUT_7_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.459 *FF_TX_H_CLK_0 to   IOL_T64A.CLK clk_125_c
                  ----
                    1.459   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.329ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   wb_tlc/intf/wb_adr_o_1[6] (from clk_125_c +)
   Destination: FF   Data in   gpio_led_out_1io[7] (to clk_125_c +)

   Delay: 7.529ns (14.5% logic, 85.5% route), 6 logic levels.

 Constraint Details:

     7.529ns physical path delay wb_tlc/intf/SLICE_4256 to LED1Gn_MGIOL meets
     8.000ns delay constraint less
    -0.044ns skew and
     0.186ns CE_SET requirement (totaling 7.858ns) by 0.329ns

IOL_T68A attributes: FINE=FDEL0

 Physical Path Details:

     Data path wb_tlc/intf/SLICE_4256 to LED1Gn_MGIOL:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R40C32B.CLK to   R40C32B.Q0 wb_tlc/intf/SLICE_4256 (from clk_125_c)
ROUTE   8   0.405   R40C32B.Q0 to   R40C30C.D0 pcie_adr[6]
CTOF_DEL   ---   0.164   R40C30C.D0 to   R40C30C.F0 wb_arb/SLICE_8881
ROUTE   1   0.577   R40C30C.F0 to   R39C29B.D1 wb_arb/un4_s5_sellto23_0_0_a2_1_4
CTOF_DEL   ---   0.164   R39C29B.D1 to   R39C29B.F1 wb_arb/SLICE_7326
ROUTE   4   1.037   R39C29B.F1 to   R33C25D.C1 wb_arb/N_844
CTOF_DEL   ---   0.164   R33C25D.C1 to   R33C25D.F1 SLICE_7317
ROUTE   12   0.350   R33C25D.F1 to   R33C25D.D0 N_846
CTOF_DEL   ---   0.164   R33C25D.D0 to   R33C25D.F0 SLICE_7317
ROUTE   10   1.227   R33C25D.F0 to   R31C43D.C1 gpio/N_855
CTOF_DEL   ---   0.164   R31C43D.C1 to   R31C43D.F1 gpio/SLICE_7315
ROUTE   8   2.838   R31C43D.F1 to   IOL_T68A.CE gpio.led_out_1_sqmuxa (to clk_125_c)

                    7.529   (14.5% logic, 85.5% route), 6 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4256:

   Name   Fanout   Delay (ns)   Site   Resource

```
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R40C32B.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to LED1Gn_MGIOL:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.459 *FF_TX_H_CLK_0 to   IOL_T68A.CLK clk_125_c
                    --------
                      1.459   (0.0% logic, 100.0% route), 0 logic levels.

Report:  125.960MHz is the maximum frequency for this preference.


================================================================================
Preference: FREQUENCY NET "can_clk_c" 25.000000 MHz ;
            4096 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 2.207ns (weighted slack = 11.035ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_tlc/intf/write  (from clk_125_c +)
   Destination:    FF         Data in       can/i_can_registers/data_overrun_irq  (to can_clk_c +)

   Delay:               5.496ns  (14.0% logic, 86.0% route), 4 logic levels.

 Constraint Details:

      5.496ns physical path delay wb_tlc/intf/SLICE_5157 to can/i_can_registers/SLICE_1691 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.297ns CE_SET requirement (totaling 7.703ns) by 2.207ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_5157 to can/i_can_registers/SLICE_1691:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R33C31C.CLK to     R33C31C.Q0 wb_tlc/intf/SLICE_5157 (from clk_125_c)
ROUTE        33     1.080     R33C31C.Q0 to     R39C23D.C1 uart1_we
CTOF_DEL    ---     0.164     R39C23D.C1 to     R39C23D.F1 can/SLICE_8052
ROUTE         9     0.946     R39C23D.F1 to     R43C21D.D1 can/data_out7
CTOF_DEL    ---     0.164     R43C21D.D1 to     R43C21D.F1 can/i_can_registers/SLICE_6950
ROUTE         8     1.332     R43C21D.F1 to     R46C21B.B1 can/i_can_registers/read_irq_reg
CTOF_DEL    ---     0.164     R46C21B.B1 to     R46C21B.F1 can/i_can_registers/SLICE_1691
ROUTE         1     1.371     R46C21B.F1 to     R46C21B.CE can/i_can_registers/un1_data_overrun_irq5 (to can_clk_c)
                    --------
                      5.496   (14.0% logic, 86.0% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_5157:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R33C31C.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/i_can_registers/SLICE_1691:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       404     1.314 *_R53C70.CLKOP to    R46C21B.CLK can_clk_c
                    --------
                      2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       404     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                    --------
                      1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:


Passed: The following path meets requirements by 2.270ns (weighted slack = 11.350ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_tlc/intf/wb_adr_o_1_2[4]  (from clk_125_c +)
   Destination:    FF         Data in       can/i_can_registers/data_overrun_irq  (to can_clk_c +)

   Delay:               5.433ns  (14.1% logic, 85.9% route), 4 logic levels.

 Constraint Details:

      5.433ns physical path delay wb_tlc/intf/SLICE_4266 to can/i_can_registers/SLICE_1691 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.297ns CE_SET requirement (totaling 7.703ns) by 2.270ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_4266 to can/i_can_registers/SLICE_1691:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R41C28A.CLK to     R41C28A.Q0 wb_tlc/intf/SLICE_4266 (from clk_125_c)
ROUTE         4     0.955     R41C28A.Q0 to     R40C24D.C1 pcie_adr_2_r0[4]
CTOF_DEL    ---     0.164     R40C24D.C1 to     R40C24D.F1 can/i_can_registers/SLICE_6970
ROUTE         7     1.008     R40C24D.F1 to     R43C21D.C1 can/i_can_registers/N_656
CTOF_DEL    ---     0.164     R43C21D.C1 to     R43C21D.F1 can/i_can_registers/SLICE_6950
ROUTE         8     1.332     R43C21D.F1 to     R46C21B.B1 can/i_can_registers/read_irq_reg
CTOF_DEL    ---     0.164     R46C21B.B1 to     R46C21B.F1 can/i_can_registers/SLICE_1691
ROUTE         1     1.371     R46C21B.F1 to     R46C21B.CE can/i_can_registers/un1_data_overrun_irq5 (to can_clk_c)
                    --------
                      5.433   (14.1% logic, 85.9% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4266:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R41C28A.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/i_can_registers/SLICE_1691:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       404     1.314 *_R53C70.CLKOP to    R46C21B.CLK can_clk_c
                    --------
                      2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       404     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                    --------
                      1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:


Passed: The following path meets requirements by 2.352ns (weighted slack = 11.760ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_tlc/intf/wb_adr_o_1[6]  (from clk_125_c +)
   Destination:    FF         Data in       can/i_can_registers/data_overrun_irq  (to can_clk_c +)

   Delay:               5.351ns  (14.3% logic, 85.7% route), 4 logic levels.

 Constraint Details:

      5.351ns physical path delay wb_tlc/intf/SLICE_4256 to can/i_can_registers/SLICE_1691 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.297ns CE_SET requirement (totaling 7.703ns) by 2.352ns
```

```
 Physical Path Details:

      Data path wb_tlc/intf/SLICE_4256 to can/i_can_registers/SLICE_1691:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R40C32B.CLK to     R40C32B.Q0 wb_tlc/intf/SLICE_4256 (from clk_125_c)
ROUTE         8     0.873     R40C32B.Q0 to     R40C24D.B1 pcie_adr[6]
CTOF_DEL    ---     0.164     R40C24D.B1 to     R40C24D.F1 can/i_can_registers/SLICE_6970
ROUTE         7     1.008     R40C24D.F1 to     R43C21D.C1 can/i_can_registers/N_656
CTOF_DEL    ---     0.164     R43C21D.C1 to     R43C21D.F1 can/i_can_registers/SLICE_6950
ROUTE         8     1.332     R43C21D.F1 to     R46C21B.B1 can/i_can_registers/read_irq_reg
CTOF_DEL    ---     0.164     R46C21B.B1 to     R46C21B.F1 can/i_can_registers/SLICE_1691
ROUTE         1     1.371     R46C21B.F1 to     R46C21B.CE can/i_can_registers/un1_data_overrun_irq5 (to can_clk_c)
                  --------
                    5.351   (14.3% logic, 85.7% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4256:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R40C32B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/i_can_registers/SLICE_1691:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       404     1.314 *_R53C70.CLKOP to    R46C21B.CLK can_clk_c
                  --------
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       404     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                  --------
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:


Passed: The following path meets requirements by 2.385ns (weighted slack = 11.925ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_tlc/intf/wb_adr_o_1_1[4]  (from clk_125_c +)
   Destination:    FF         Data in        can/data_out[4]  (to can_clk_c +)

   Delay:               5.547ns  (25.7% logic, 74.3% route), 6 logic levels.

 Constraint Details:

      5.547ns physical path delay wb_tlc/intf/SLICE_4265 to can/SLICE_1812 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 2.385ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_4265 to can/SLICE_1812:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R39C24B.CLK to     R39C24B.Q0 wb_tlc/intf/SLICE_4265 (from clk_125_c)
ROUTE       100     1.603     R39C24B.Q0 to     R45C14C.D1 pcie_adr_1[4]
CTOF_DEL    ---     0.164     R45C14C.D1 to     R45C14C.F1 can/SLICE_6885
ROUTE         1     0.817     R45C14C.F1 to     R46C19D.D1 can/i_can_registers/N_589
CTOOFX_DEL  ---     0.338     R46C19D.D1 to   R46C19D.OFX0 can/i_can_registers/data_out_22[4]/SLICE_6323
ROUTE         1     0.824   R46C19D.OFX0 to     R48C25B.D0 can/i_can_registers/N_613
CTOOFX_DEL  ---     0.338     R48C25B.D0 to   R48C25B.OFX0 can/i_can_registers/data_out_35[4]/SLICE_6321
ROUTE         1     0.000   R48C25B.OFX0 to    R48C25A.FXA can/i_can_registers/N_717
FXTOOFX_DE  ---     0.146    R48C25A.FXA to   R48C25A.OFX1 can/i_can_registers/data_out_82[4]/SLICE_6325
ROUTE         1     0.878   R48C25A.OFX1 to     R45C26B.D0 can/data_out_regs[4]
CTOF_DEL    ---     0.164     R45C26B.D0 to     R45C26B.F0 can/SLICE_1812
ROUTE         1     0.000     R45C26B.F0 to    R45C26B.DI0 can/N_282_i (to can_clk_c)
                  --------
                    5.547   (25.7% logic, 74.3% route), 6 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4265:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R39C24B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/SLICE_1812:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       404     1.314 *_R53C70.CLKOP to    R45C26B.CLK can_clk_c
                  --------
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       404     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                  --------
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:


Passed: The following path meets requirements by 2.401ns (weighted slack = 12.005ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_tlc/intf/wb_adr_o_1[2]  (from clk_125_c +)
   Destination:    FF         Data in        can/i_can_registers/data_overrun_irq  (to can_clk_c +)

   Delay:               5.302ns  (14.5% logic, 85.5% route), 4 logic levels.

 Constraint Details:

      5.302ns physical path delay wb_tlc/intf/SLICE_5146 to can/i_can_registers/SLICE_1691 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.297ns CE_SET requirement (totaling 7.703ns) by 2.401ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_5146 to can/i_can_registers/SLICE_1691:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R39C25A.CLK to     R39C25A.Q0 wb_tlc/intf/SLICE_5146 (from clk_125_c)
ROUTE        78     1.208     R39C25A.Q0 to     R42C21C.B1 uart1_adr[2]
CTOF_DEL    ---     0.164     R42C21C.B1 to     R42C21C.F1 can/SLICE_1482
ROUTE         3     0.624     R42C21C.F1 to     R43C21D.B1 can/i_can_registers/N_693
CTOF_DEL    ---     0.164     R43C21D.B1 to     R43C21D.F1 can/i_can_registers/SLICE_6950
ROUTE         8     1.332     R43C21D.F1 to     R46C21B.B1 can/i_can_registers/read_irq_reg
CTOF_DEL    ---     0.164     R46C21B.B1 to     R46C21B.F1 can/i_can_registers/SLICE_1691
ROUTE         1     1.371     R46C21B.F1 to     R46C21B.CE can/i_can_registers/un1_data_overrun_irq5 (to can_clk_c)
                  --------
                    5.302   (14.5% logic, 85.5% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_5146:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R39C25A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/i_can_registers/SLICE_1691:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       404     1.314 *_R53C70.CLKOP to    R46C21B.CLK can_clk_c
```

                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name   Fanout   Delay (ns)   Site   Resource
CLKFB2OP_D ---   0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE   404   1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                  ----
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

Passed: The following path meets requirements by 2.408ns (weighted slack = 12.040ns)

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   wb_tlc/intf/wb_adr_o_1[0] (from clk_125_c +)
   Destination: FF   Data in   can/data_out[3] (to can_clk_c +)

   Delay: 5.524ns (22.6% logic, 77.4% route), 6 logic levels.

 Constraint Details:

      5.524ns physical path delay wb_tlc/intf/SLICE_5145 to can/SLICE_1811 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 2.408ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_5145 to can/SLICE_1811:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R39C24A.CLK to   R39C24A.Q0 wb_tlc/intf/SLICE_5145 (from clk_125_c)
ROUTE   73   1.520   R39C24A.Q0 to   R43C14D.C0 uart1_adr[0]
CTOF_DEL   ---   0.164   R43C14D.C0 to   R43C14D.F0 can/i_can_registers/SLICE_6989
ROUTE   1   0.978   R43C14D.F0 to   R40C21A.C0 can/i_can_registers/N_980
CTOOFX_DEL ---   0.338   R40C21A.C0 to   R40C21A.OFX0 can/i_can_registers/data_out_81[3]/SLICE_6328
ROUTE   1   0.000   R40C21A.OFX0 to   R40C21A.FXB can/i_can_registers/N_1084
FXTOOFX_DE ---   0.146   R40C21A.FXB to   R40C21A.OFX1 can/i_can_registers/data_out_81[3]/SLICE_6328
ROUTE   1   1.103   R40C21A.OFX1 to   R46C27B.D0 can/i_can_registers/N_1092
CTOF_DEL   ---   0.164   R46C27B.D0 to   R46C27B.F0 can/i_can_registers/SLICE_6948
ROUTE   1   0.672   R46C27B.F0 to   R45C30B.D1 can/data_out_regs[3]
CTOF_DEL   ---   0.164   R45C30B.D1 to   R45C30B.F1 can/SLICE_1811
ROUTE   1   0.000   R45C30B.F1 to   R45C30B.DI1 can/N_280_i (to can_clk_c)

                    5.524   (22.6% logic, 77.4% route), 6 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_5145:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R39C24A.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/SLICE_1811:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE ---   0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE   404   1.314 *_R53C70.CLKOP to   R45C30B.CLK can_clk_c
                  ----
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name   Fanout   Delay (ns)   Site   Resource
CLKFB2OP_D ---   0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE   404   1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                  ----
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

Passed: The following path meets requirements by 2.428ns (weighted slack = 12.140ns)

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   wb_tlc/intf/write (from clk_125_c +)
   Destination: FF   Data in   can/i_can_registers/ERROR_WARNING_REG/data_out[7] (to can_clk_c +)
                   FF   can/i_can_registers/ERROR_WARNING_REG/data_out[6]

   Delay: 5.275ns (14.5% logic, 85.5% route), 4 logic levels.

 Constraint Details:

      5.275ns physical path delay wb_tlc/intf/SLICE_5157 to can/i_can_registers/ERROR_WARNING_REG/SLICE_1507 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.297ns CE_SET requirement (totaling 7.703ns) by 2.428ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_5157 to can/i_can_registers/ERROR_WARNING_REG/SLICE_1507:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R33C31C.CLK to   R33C31C.Q0 wb_tlc/intf/SLICE_5157 (from clk_125_c)
ROUTE   33   1.303   R33C31C.Q0 to   R39C17C.C1 uart1_we
CTOF_DEL   ---   0.164   R39C17C.C1 to   R39C17C.F1 can/i_can_registers/SLICE_6958
ROUTE   9   0.372   R39C17C.F1 to   R39C17D.D1 can/i_can_registers/N_654
CTOF_DEL   ---   0.164   R39C17D.D1 to   R39C17D.F1 can/SLICE_6856
ROUTE   10   0.866   R39C17D.F1 to   R39C22D.D0 can/N_699
CTOF_DEL   ---   0.164   R39C22D.D0 to   R39C22D.F0 can/i_can_registers/SLICE_6936
ROUTE   4   1.967   R39C22D.F0 to   R43C15A.CE can/i_can_registers/we_error_warning_limit (to can_clk_c)

                    5.275   (14.5% logic, 85.5% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_5157:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R33C31C.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/i_can_registers/ERROR_WARNING_REG/SLICE_1507:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE ---   0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE   404   1.314 *_R53C70.CLKOP to   R43C15A.CLK can_clk_c
                  ----
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name   Fanout   Delay (ns)   Site   Resource
CLKFB2OP_D ---   0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE   404   1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                  ----
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

Passed: The following path meets requirements by 2.455ns (weighted slack = 12.275ns)

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   wb_tlc/intf/wb_adr_o_1[6] (from clk_125_c +)
   Destination: FF   Data in   can/i_can_registers/COMMAND_REG4/data_out[0] (to can_clk_c +)

   Delay: 5.248ns (14.6% logic, 85.4% route), 4 logic levels.

 Constraint Details:

      5.248ns physical path delay wb_tlc/intf/SLICE_4256 to can/i_can_registers/COMMAND_REG4/SLICE_1493 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and

     0.297ns CE_SET requirement (totaling 7.703ns) by 2.455ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_4256 to can/i_can_registers/COMMAND_REG4/SLICE_1493:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R40C32B.CLK to   R40C32B.Q0 wb_tlc/intf/SLICE_4256 (from clk_125_c)
ROUTE   8   1.249   R40C32B.Q0 to   R39C22D.C1 pcie_adr[6]
CTOF_DEL   ---   0.164   R39C22D.C1 to   R39C22D.F1 can/i_can_registers/SLICE_6936
ROUTE   9   1.569   R39C22D.F1 to   R54C14D.C1 can/i_can_registers/N_669
CTOF_DEL   ---   0.164   R54C14D.C1 to   R54C14D.F1 can/i_can_registers/SLICE_6934
ROUTE   4   0.484   R54C14D.F1 to   R54C14D.C0 can/i_can_registers/N_572_0
CTOF_DEL   ---   0.164   R54C14D.C0 to   R54C14D.F0 can/i_can_registers/SLICE_6934
ROUTE   1   1.179   R54C14D.F0 to   R54C14A.CE can/i_can_registers/COMMAND_REG4/un1_we_0_3 (to can_clk_c)

                    5.248   (14.6% logic, 85.4% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4256:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R40C32B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/i_can_registers/COMMAND_REG4/SLICE_1493:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE ---   0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE   404   1.314 *_R53C70.CLKOP to   R54C14A.CLK can_clk_c
                  ----
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name   Fanout   Delay (ns)   Site   Resource
CLKFB2OP_D ---   0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE   404   1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                  ----
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

Passed: The following path meets requirements by 2.460ns (weighted slack = 12.300ns)

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   wb_tlc/intf/wb_adr_o_1_2[4] (from clk_125_c +)
   Destination: FF   Data in   can/i_can_registers/TX_DATA_REG9/data_out[5] (to can_clk_c +)
                   FF   can/i_can_registers/TX_DATA_REG9/data_out[4]

   Delay: 5.243ns (14.6% logic, 85.4% route), 4 logic levels.

 Constraint Details:

      5.243ns physical path delay wb_tlc/intf/SLICE_4266 to can/i_can_registers/TX_DATA_REG9/SLICE_1799 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.297ns CE_SET requirement (totaling 7.703ns) by 2.460ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_4266 to can/i_can_registers/TX_DATA_REG9/SLICE_1799:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R41C28A.CLK to   R41C28A.Q0 wb_tlc/intf/SLICE_4266 (from clk_125_c)
ROUTE   4   1.297   R41C28A.Q0 to   R39C20C.B1 pcie_adr_2_r0[4]
CTOF_DEL   ---   0.164   R39C20C.B1 to   R39C20C.F1 can/SLICE_6940
ROUTE   9   1.330   R39C20C.F1 to   R42C18D.A1 can/N_392
CTOF_DEL   ---   0.164   R42C18D.A1 to   R42C18D.F1 can/i_can_registers/SLICE_6954
ROUTE   1   0.469   R42C18D.F1 to   R42C18D.C0 can/i_can_registers/N_696
CTOF_DEL   ---   0.164   R42C18D.C0 to   R42C18D.F0 can/i_can_registers/SLICE_6954
ROUTE   4   1.380   R42C18D.F0 to   R47C18C.CE can/i_can_registers/we_tx_data_9 (to can_clk_c)

                    5.243   (14.6% logic, 85.4% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4266:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R41C28A.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/i_can_registers/TX_DATA_REG9/SLICE_1799:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE ---   0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE   404   1.314 *_R53C70.CLKOP to   R47C18C.CLK can_clk_c
                  ----
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name   Fanout   Delay (ns)   Site   Resource
CLKFB2OP_D ---   0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE   404   1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                  ----
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

Passed: The following path meets requirements by 2.460ns (weighted slack = 12.300ns)

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   wb_tlc/intf/wb_adr_o_1_1[0] (from clk_125_c +)
   Destination: FF   Data in   can/i_can_registers/data_overrun_irq (to can_clk_c +)

   Delay: 5.243ns (14.6% logic, 85.4% route), 4 logic levels.

 Constraint Details:

      5.243ns physical path delay wb_tlc/intf/SLICE_1902 to can/i_can_registers/SLICE_1691 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.297ns CE_SET requirement (totaling 7.703ns) by 2.460ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_1902 to can/i_can_registers/SLICE_1691:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R39C24C.CLK to   R39C24C.Q0 wb_tlc/intf/SLICE_1902 (from clk_125_c)
ROUTE   82   1.149   R39C24C.Q0 to   R42C21C.C1 msi_adr_1[0]
CTOF_DEL   ---   0.164   R42C21C.C1 to   R42C21C.F1 can/SLICE_1482
ROUTE   3   0.624   R42C21C.F1 to   R43C21D.B1 can/i_can_registers/N_693
CTOF_DEL   ---   0.164   R43C21D.B1 to   R43C21D.F1 can/i_can_registers/SLICE_6950
ROUTE   8   1.332   R43C21D.F1 to   R46C21B.B1 can/i_can_registers/read_irq_reg
CTOF_DEL   ---   0.164   R46C21B.B1 to   R46C21B.F1 can/i_can_registers/SLICE_1691
ROUTE   1   1.371   R46C21B.F1 to   R46C21B.CE can/i_can_registers/un1_data_overrun_irq5 (to can_clk_c)

                    5.243   (14.6% logic, 85.4% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_1902:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R39C24C.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/i_can_registers/SLICE_1691:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE ---   0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE   404   1.314 *_R53C70.CLKOP to   R46C21B.CLK can_clk_c
                  ----
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

```
PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       404     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                    --------
                      1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

Report:   34.524MHz is the maximum frequency for this preference.


================================================================================
Preference: FREQUENCY NET "uart_clk_c" 25.000000 MHz ;
            4096 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 2.176ns (weighted slack = 10.880ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_tlc/intf/wb_sel_o_0[1]  (from clk_125_c +)
   Destination:    FF         Data in       uart4/regs/dl[3]  (to uart_clk_c +)

   Delay:               5.679ns  (7.7% logic, 92.3% route), 2 logic levels.

 Constraint Details:

      5.679ns physical path delay wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5528 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 2.176ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5528:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R33C28B.CLK to     R33C28B.Q1 wb_tlc/intf/SLICE_5156 (from clk_125_c)
ROUTE        23     1.093     R33C28B.Q1 to     R34C18B.D1 uart1_sel[1]
CTOF_DEL    ---     0.164     R34C18B.D1 to     R34C18B.F1 SLICE_5172
ROUTE        36     4.147     R34C18B.F1 to     R56C59B.M1 I_945.t1 (to uart_clk_c)
                    --------
                      5.679   (7.7% logic, 92.3% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_5156:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R33C28B.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart4/regs/SLICE_5528:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R56C59B.CLK uart_clk_c
                    --------
                      2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                    --------
                      1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 2.501ns (weighted slack = 12.505ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_tlc/intf/wb_sel_o_0[1]  (from clk_125_c +)
   Destination:    FF         Data in       uart4/regs/mcr[3]  (to uart_clk_c +)

   Delay:               5.354ns  (8.2% logic, 91.8% route), 2 logic levels.

 Constraint Details:

      5.354ns physical path delay wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5596 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 2.501ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5596:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R33C28B.CLK to     R33C28B.Q1 wb_tlc/intf/SLICE_5156 (from clk_125_c)
ROUTE        23     1.093     R33C28B.Q1 to     R34C18B.D1 uart1_sel[1]
CTOF_DEL    ---     0.164     R34C18B.D1 to     R34C18B.F1 SLICE_5172
ROUTE        36     3.822     R34C18B.F1 to     R56C56A.M1 I_945.t1 (to uart_clk_c)
                    --------
                      5.354   (8.2% logic, 91.8% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_5156:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R33C28B.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart4/regs/SLICE_5596:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R56C56A.CLK uart_clk_c
                    --------
                      2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                    --------
                      1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 2.575ns (weighted slack = 12.875ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_tlc/intf/wb_sel_o_0[1]  (from clk_125_c +)
   Destination:    FF         Data in       uart4/regs/dl[6]  (to uart_clk_c +)

   Delay:               5.280ns  (8.3% logic, 91.7% route), 2 logic levels.

 Constraint Details:

      5.280ns physical path delay wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5530 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 2.575ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5530:

   Name    Fanout   Delay (ns)          Site               Resource
```

```
REG_DEL     ---     0.275    R33C28B.CLK to     R33C28B.Q1 wb_tlc/intf/SLICE_5156 (from clk_125_c)
ROUTE        23     1.010     R33C28B.Q1 to     R34C16C.C0 uart1_sel[1]
CTOF_DEL    ---     0.164     R34C16C.C0 to     R34C16C.F0 SLICE_5174
ROUTE        31     3.831     R34C16C.F0 to     R56C59C.M0 I_948.t1 (to uart_clk_c)
                   --------
                     5.280   (8.3% logic, 91.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_5156:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R33C28B.CLK clk_125_c
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart4/regs/SLICE_5530:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R56C59C.CLK uart_clk_c
                   --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                   --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 2.583ns (weighted slack = 12.915ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_tlc/intf/wb_sel_o_0[1]  (from clk_125_c +)
   Destination:    FF         Data in        uart4/regs/dl[14]  (to uart_clk_c +)

   Delay:               5.272ns  (8.3% logic, 91.7% route), 2 logic levels.

 Constraint Details:

      5.272ns physical path delay wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5534 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 2.583ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5534:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R33C28B.CLK to     R33C28B.Q1 wb_tlc/intf/SLICE_5156 (from clk_125_c)
ROUTE        23     1.010     R33C28B.Q1 to     R34C16C.C0 uart1_sel[1]
CTOF_DEL    ---     0.164     R34C16C.C0 to     R34C16C.F0 SLICE_5174
ROUTE        31     3.823     R34C16C.F0 to     R55C59B.M0 I_948.t1 (to uart_clk_c)
                   --------
                     5.272   (8.3% logic, 91.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_5156:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R33C28B.CLK clk_125_c
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart4/regs/SLICE_5534:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R55C59B.CLK uart_clk_c
                   --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                   --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 2.583ns (weighted slack = 12.915ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_tlc/intf/wb_sel_o_0[1]  (from clk_125_c +)
   Destination:    FF         Data in        uart4/regs/scratch[6]  (to uart_clk_c +)

   Delay:               5.272ns  (8.3% logic, 91.7% route), 2 logic levels.

 Constraint Details:

      5.272ns physical path delay wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5651 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 2.583ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5651:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R33C28B.CLK to     R33C28B.Q1 wb_tlc/intf/SLICE_5156 (from clk_125_c)
ROUTE        23     1.010     R33C28B.Q1 to     R34C16C.C0 uart1_sel[1]
CTOF_DEL    ---     0.164     R34C16C.C0 to     R34C16C.F0 SLICE_5174
ROUTE        31     3.823     R34C16C.F0 to     R56C58A.M0 I_948.t1 (to uart_clk_c)
                   --------
                     5.272   (8.3% logic, 91.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_5156:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R33C28B.CLK clk_125_c
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart4/regs/SLICE_5651:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R56C58A.CLK uart_clk_c
                   --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                   --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 2.583ns (weighted slack = 12.915ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_tlc/intf/wb_sel_o_0[1]  (from clk_125_c +)
   Destination:    FF         Data in        uart4/regs/fcr[0]  (to uart_clk_c +)
```

```
   Delay:               5.272ns  (8.3% logic, 91.7% route), 2 logic levels.

 Constraint Details:

      5.272ns physical path delay wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5537 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 2.583ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5537:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R33C28B.CLK to     R33C28B.Q1 wb_tlc/intf/SLICE_5156 (from clk_125_c)
ROUTE        23     1.010     R33C28B.Q1 to     R34C16C.C0 uart1_sel[1]
CTOF_DEL    ---     0.164     R34C16C.C0 to     R34C16C.F0 SLICE_5174
ROUTE        31     3.823     R34C16C.F0 to     R59C59B.M0 I_948.t1 (to uart_clk_c)
                   --------
                     5.272   (8.3% logic, 91.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_5156:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R33C28B.CLK clk_125_c
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart4/regs/SLICE_5537:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R59C59B.CLK uart_clk_c
                   --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                   --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 2.585ns (weighted slack = 12.925ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_tlc/intf/wb_sel_o_0[1]  (from clk_125_c +)
   Destination:    FF         Data in        uart4/regs/dl[15]  (to uart_clk_c +)

   Delay:               5.270ns  (8.3% logic, 91.7% route), 2 logic levels.

 Constraint Details:

      5.270ns physical path delay wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5534 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 2.585ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5534:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R33C28B.CLK to     R33C28B.Q1 wb_tlc/intf/SLICE_5156 (from clk_125_c)
ROUTE        23     1.010     R33C28B.Q1 to     R34C16C.C1 uart1_sel[1]
CTOF_DEL    ---     0.164     R34C16C.C1 to     R34C16C.F1 SLICE_5174
ROUTE        31     3.821     R34C16C.F1 to     R55C59B.M1 I_949.t1 (to uart_clk_c)
                   --------
                     5.270   (8.3% logic, 91.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_5156:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R33C28B.CLK clk_125_c
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart4/regs/SLICE_5534:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R55C59B.CLK uart_clk_c
                   --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                   --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 2.589ns (weighted slack = 12.945ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_tlc/intf/wb_sel_o_0[1]  (from clk_125_c +)
   Destination:    FF         Data in        uart4/regs/scratch[7]  (to uart_clk_c +)

   Delay:               5.266ns  (8.3% logic, 91.7% route), 2 logic levels.

 Constraint Details:

      5.266ns physical path delay wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5651 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 2.589ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5651:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R33C28B.CLK to     R33C28B.Q1 wb_tlc/intf/SLICE_5156 (from clk_125_c)
ROUTE        23     1.010     R33C28B.Q1 to     R34C16C.C1 uart1_sel[1]
CTOF_DEL    ---     0.164     R34C16C.C1 to     R34C16C.F1 SLICE_5174
ROUTE        31     3.817     R34C16C.F1 to     R56C58A.M1 I_949.t1 (to uart_clk_c)
                   --------
                     5.266   (8.3% logic, 91.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_5156:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R33C28B.CLK clk_125_c
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart4/regs/SLICE_5651:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R56C58A.CLK uart_clk_c
                   --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:
```

```
   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                    --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 2.596ns (weighted slack = 12.980ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_tlc/intf/wb_sel_o_0[1]  (from clk_125_c +)
   Destination:    FF         Data in       uart4/regs/fcr[1]  (to uart_clk_c +)

   Delay:               5.259ns  (8.3% logic, 91.7% route), 2 logic levels.

 Constraint Details:

      5.259ns physical path delay wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5537 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 2.596ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5537:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R33C28B.CLK to     R33C28B.Q1 wb_tlc/intf/SLICE_5156 (from clk_125_c)
ROUTE        23     1.010     R33C28B.Q1 to     R34C16C.C1 uart1_sel[1]
CTOF_DEL    ---     0.164     R34C16C.C1 to     R34C16C.F1 SLICE_5174
ROUTE        31     3.810     R34C16C.F1 to     R59C59B.M1 I_949.t1 (to uart_clk_c)
                    --------
                     5.259   (8.3% logic, 91.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_5156:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R33C28B.CLK clk_125_c
                    --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart4/regs/SLICE_5537:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R59C59B.CLK uart_clk_c
                    --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                    --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 2.604ns (weighted slack = 13.020ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_tlc/intf/wb_sel_o_0[1]  (from clk_125_c +)
   Destination:    FF         Data in       uart4/regs/lcr[7]  (to uart_clk_c +)

   Delay:               5.251ns  (8.4% logic, 91.6% route), 2 logic levels.

 Constraint Details:

      5.251ns physical path delay wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5578 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 2.604ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_5156 to uart4/regs/SLICE_5578:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R33C28B.CLK to     R33C28B.Q1 wb_tlc/intf/SLICE_5156 (from clk_125_c)
ROUTE        23     1.010     R33C28B.Q1 to     R34C16C.C1 uart1_sel[1]
CTOF_DEL    ---     0.164     R34C16C.C1 to     R34C16C.F1 SLICE_5174
ROUTE        31     3.802     R34C16C.F1 to     R55C58B.M1 I_949.t1 (to uart_clk_c)
                    --------
                     5.251   (8.4% logic, 91.6% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_5156:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R33C28B.CLK clk_125_c
                    --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart4/regs/SLICE_5578:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R55C58B.CLK uart_clk_c
                    --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                    --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

Report:   34.341MHz is the maximum frequency for this preference.


================================================================================
Preference: FREQUENCY NET "pcie/pclk" 250.000000 MHz ;
            987 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.418ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_pcs_pipe/pipe_top_0/RxData_chx_reg[7]  (from pcie/pclk +)
   Destination:    FF         Data in       pcie/u1_pcs_pipe/pipe_top_0/RxValid_chx  (to pcie/pclk +)

   Delay:               3.285ns  (23.3% logic, 76.7% route), 4 logic levels.

 Constraint Details:

      3.285ns physical path delay pcie/u1_pcs_pipe/pipe_top_0/SLICE_4221 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_1962 meets
      4.000ns delay constraint less
      0.000ns skew and
      0.297ns CE_SET requirement (totaling 3.703ns) by 0.418ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pipe_top_0/SLICE_4221 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_1962:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R45C61A.CLK to     R45C61A.Q1 pcie/u1_pcs_pipe/pipe_top_0/SLICE_4221 (from pcie/pclk)
ROUTE         2     0.540     R45C61A.Q1 to     R45C62A.C1 pcie/u1_pcs_pipe/pipe_top_0/RxData_chx_reg[7]
CTOF_DEL    ---     0.164     R45C62A.C1 to     R45C62A.F1 pcie/u1_pcs_pipe/pipe_top_0/SLICE_7384
ROUTE         1     0.596     R45C62A.F1 to     R45C62A.A0 pcie/u1_pcs_pipe/pipe_top_0/un1_RxValid_chx5_0_a2_0
CTOF_DEL    ---     0.164     R45C62A.A0 to     R45C62A.F0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_7384
```

```
ROUTE         1     0.569     R45C62A.F0 to     R45C62D.B0 pcie/u1_pcs_pipe/pipe_top_0/un1_RxValid_chx5_0_a2_6
CTOF_DEL    ---     0.164     R45C62D.B0 to     R45C62D.F0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_7383
ROUTE         1     0.813     R45C62D.F0 to     R45C63A.CE pcie/u1_pcs_pipe/pipe_top_0/un1_RxValid_chx5_0 (to pcie/pclk)
                  --------
                    3.285   (23.3% logic, 76.7% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4221:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to    R45C61A.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_1962:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to    R45C63A.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.496ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         PCSD       Port           pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0(ASIC)  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_pcs_pipe/pipe_top_0/RxData_chx_reg[5]  (to pcie/pclk +)

   Delay:               3.207ns  (30.5% logic, 69.5% route), 1 logic levels.

 Constraint Details:

      3.207ns physical path delay pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4220 meets
      4.000ns delay constraint less
      0.152ns skew and
      0.145ns M_SET requirement (totaling 3.703ns) by 0.496ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4220:

   Name    Fanout   Delay (ns)          Site               Resource
C2OUT_DEL   ---     0.979 *.FF_RXI_CLK_0 to *A.FF_RX_D_0_5 pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 (from pcie/pclk)
ROUTE         1     2.228 *A.FF_RX_D_0_5 to     R45C62C.M1 pcie/u1_pcs_pipe/RxData_0_in[5] (to pcie/pclk)
                  --------
                    3.207   (30.5% logic, 69.5% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.567 *FF_TX_F_CLK_0 to *.FF_RXI_CLK_0 pcie/pclk
                  --------
                    1.567   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4220:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to    R45C62C.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.590ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_pcs_pipe/pipe_top_0/RxData_chx_reg[6]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_pcs_pipe/pipe_top_0/RxValid_chx  (to pcie/pclk +)

   Delay:               3.113ns  (24.6% logic, 75.4% route), 4 logic levels.

 Constraint Details:

      3.113ns physical path delay pcie/u1_pcs_pipe/pipe_top_0/SLICE_4221 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_1962 meets
      4.000ns delay constraint less
      0.000ns skew and
      0.297ns CE_SET requirement (totaling 3.703ns) by 0.590ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pipe_top_0/SLICE_4221 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_1962:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R45C61A.CLK to     R45C61A.Q0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_4221 (from pcie/pclk)
ROUTE         2     0.368     R45C61A.Q0 to     R45C62A.D1 pcie/u1_pcs_pipe/pipe_top_0/RxData_chx_reg[6]
CTOF_DEL    ---     0.164     R45C62A.D1 to     R45C62A.F1 pcie/u1_pcs_pipe/pipe_top_0/SLICE_7384
ROUTE         1     0.596     R45C62A.F1 to     R45C62A.A0 pcie/u1_pcs_pipe/pipe_top_0/un1_RxValid_chx5_0_a2_0
CTOF_DEL    ---     0.164     R45C62A.A0 to     R45C62A.F0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_7384
ROUTE         1     0.569     R45C62A.F0 to     R45C62D.B0 pcie/u1_pcs_pipe/pipe_top_0/un1_RxValid_chx5_0_a2_6
CTOF_DEL    ---     0.164     R45C62D.B0 to     R45C62D.F0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_7383
ROUTE         1     0.813     R45C62D.F0 to     R45C63A.CE pcie/u1_pcs_pipe/pipe_top_0/un1_RxValid_chx5_0 (to pcie/pclk)
                  --------
                    3.113   (24.6% logic, 75.4% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4221:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to    R45C61A.CLK pcie/pclk
                  -------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_1962:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to    R45C63A.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.674ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         PCSD       Port           pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0(ASIC)  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_pcs_pipe/pipe_top_0/RxData_chx_reg[1]  (to pcie/pclk +)

   Delay:               3.029ns  (32.3% logic, 67.7% route), 1 logic levels.

 Constraint Details:

      3.029ns physical path delay pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4218 meets
      4.000ns delay constraint less
      0.152ns skew and
      0.145ns M_SET requirement (totaling 3.703ns) by 0.674ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4218:

   Name    Fanout   Delay (ns)          Site               Resource
C2OUT_DEL   ---     0.979 *.FF_RXI_CLK_0 to *A.FF_RX_D_0_1 pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 (from pcie/pclk)
ROUTE         1     2.050 *A.FF_RX_D_0_1 to     R45C62B.M1 pcie/u1_pcs_pipe/RxData_0_in[1] (to pcie/pclk)
                  --------
                    3.029   (32.3% logic, 67.7% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.567 *FF_TX_F_CLK_0 to *.FF_RXI_CLK_0 pcie/pclk
                  --------
                    1.567   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4218:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to    R45C62B.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.730ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         PCSD       Port           pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0(ASIC)  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_pcs_pipe/pipe_top_0/RxData_chx_reg[0]  (to pcie/pclk +)
```

```
   Delay:               2.973ns  (32.9% logic, 67.1% route), 1 logic levels.

 Constraint Details:

      2.973ns physical path delay pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4218 meets
      4.000ns delay constraint less
      0.152ns skew and
      0.145ns M_SET requirement (totaling 3.703ns) by 0.730ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4218:

   Name    Fanout   Delay (ns)          Site               Resource
C2OUT_DEL   ---     0.979 *.FF_RXI_CLK_0 to *A.FF_RX_D_0_0 pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 (from pcie/pclk)
ROUTE         1     1.994 *A.FF_RX_D_0_0 to     R45C62B.M0 pcie/u1_pcs_pipe/RxData_0_in[0] (to pcie/pclk)
                   --------
                     2.973   (32.9% logic, 67.1% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.567 *FF_TX_F_CLK_0 to *.FF_RXI_CLK_0 pcie/pclk
                   --------
                     1.567   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4218:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to    R45C62B.CLK pcie/pclk
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.730ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         PCSD       Port           pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0(ASIC)  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_pcs_pipe/pipe_top_0/RxData_chx_reg[2]  (to pcie/pclk +)

   Delay:               2.973ns  (32.9% logic, 67.1% route), 1 logic levels.

 Constraint Details:

      2.973ns physical path delay pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4219 meets
      4.000ns delay constraint less
      0.152ns skew and
      0.145ns M_SET requirement (totaling 3.703ns) by 0.730ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4219:

   Name    Fanout   Delay (ns)          Site               Resource
C2OUT_DEL   ---     0.979 *.FF_RXI_CLK_0 to *A.FF_RX_D_0_2 pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 (from pcie/pclk)
ROUTE         1     1.994 *A.FF_RX_D_0_2 to     R46C62B.M0 pcie/u1_pcs_pipe/RxData_0_in[2] (to pcie/pclk)
                   --------
                     2.973   (32.9% logic, 67.1% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.567 *FF_TX_F_CLK_0 to *.FF_RXI_CLK_0 pcie/pclk
                   --------
                     1.567   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4219:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to    R46C62B.CLK pcie/pclk
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.759ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         PCSD       Port           pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0(ASIC)  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_pcs_pipe/pipe_top_0/RxData_chx_reg[3]  (to pcie/pclk +)

   Delay:               2.944ns  (33.3% logic, 66.7% route), 1 logic levels.

 Constraint Details:

      2.944ns physical path delay pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4219 meets
      4.000ns delay constraint less
      0.152ns skew and
      0.145ns M_SET requirement (totaling 3.703ns) by 0.759ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4219:

   Name    Fanout   Delay (ns)          Site               Resource
C2OUT_DEL   ---     0.979 *.FF_RXI_CLK_0 to *A.FF_RX_D_0_3 pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 (from pcie/pclk)
ROUTE         1     1.965 *A.FF_RX_D_0_3 to     R46C62B.M1 pcie/u1_pcs_pipe/RxData_0_in[3] (to pcie/pclk)
                   --------
                     2.944   (33.3% logic, 66.7% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.567 *FF_TX_F_CLK_0 to *.FF_RXI_CLK_0 pcie/pclk
                   --------
                     1.567   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4219:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to    R46C62B.CLK pcie/pclk
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.777ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         PCSD       Port           pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0(ASIC)  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_pcs_pipe/pipe_top_0/RxDataK_chx_reg  (to pcie/pclk +)

   Delay:               2.926ns  (33.5% logic, 66.5% route), 1 logic levels.

 Constraint Details:

      2.926ns physical path delay pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_7384 meets
      4.000ns delay constraint less
      0.152ns skew and
      0.145ns M_SET requirement (totaling 3.703ns) by 0.777ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_7384:

   Name    Fanout   Delay (ns)          Site               Resource
C2OUT_DEL   ---     0.979 *.FF_RXI_CLK_0 to *A.FF_RX_D_0_8 pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 (from pcie/pclk)
ROUTE         1     1.947 *A.FF_RX_D_0_8 to     R45C62A.M0 pcie/u1_pcs_pipe/RxDataK_0_in (to pcie/pclk)
                   --------
                     2.926   (33.5% logic, 66.5% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.567 *FF_TX_F_CLK_0 to *.FF_RXI_CLK_0 pcie/pclk
                   --------
                     1.567   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_7384:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to    R45C62A.CLK pcie/pclk
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.
```

Passed: The following path meets requirements by 0.855ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: PCSD   Port   pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0(ASIC) (from pcie/pclk +)
   Destination: FF   Data in   pcie/u1_pcs_pipe/pipe_top_0/RxData_chx_reg[7] (to pcie/pclk +)

   Delay: 2.848ns (34.4% logic, 65.6% route), 1 logic levels.

 Constraint Details:

      2.848ns physical path delay pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4221 meets
      4.000ns delay constraint less
      0.152ns skew and
      0.145ns M_SET requirement (totaling 3.703ns) by 0.855ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4221:

   Name   Fanout   Delay (ns)   Site   Resource
C2OUT_DEL   ---   0.979 *.FF_RXI_CLK_0 to *A.FF_RX_D_0_7 pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 (from pcie/pclk)
ROUTE   1   1.869 *A.FF_RX_D_0_7 to   R45C61A.M1 pcie/u1_pcs_pipe/RxData_0_in[7] (to pcie/pclk)

                    2.848   (34.4% logic, 65.6% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   192   1.567 *FF_TX_F_CLK_0 to *.FF_RXI_CLK_0 pcie/pclk
                  ----
                    1.567   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4221:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   192   1.415 *FF_TX_F_CLK_0 to   R45C61A.CLK pcie/pclk
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.952ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: PCSD   Port   pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0(ASIC) (from pcie/pclk +)
   Destination: FF   Data in   pcie/u1_pcs_pipe/pipe_top_0/RxData_chx_reg[4] (to pcie/pclk +)

   Delay: 2.751ns (35.6% logic, 64.4% route), 1 logic levels.

 Constraint Details:

      2.751ns physical path delay pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4220 meets
      4.000ns delay constraint less
      0.152ns skew and
      0.145ns M_SET requirement (totaling 3.703ns) by 0.952ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4220:

   Name   Fanout   Delay (ns)   Site   Resource
C2OUT_DEL   ---   0.979 *.FF_RXI_CLK_0 to *A.FF_RX_D_0_4 pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 (from pcie/pclk)
ROUTE   1   1.772 *A.FF_RX_D_0_4 to   R45C62C.M0 pcie/u1_pcs_pipe/RxData_0_in[4] (to pcie/pclk)

                    2.751   (35.6% logic, 64.4% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   192   1.567 *FF_TX_F_CLK_0 to *.FF_RXI_CLK_0 pcie/pclk
                  ----
                    1.567   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4220:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   192   1.415 *FF_TX_F_CLK_0 to   R45C62C.CLK pcie/pclk
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Report: 279.174MHz is the maximum frequency for this preference.

==
Preference: FREQUENCY NET "pcie/u1_pcs_pipe/ff_rx_fclk_0" 250.000000 MHz ;
            1 item scored, 0 timing errors detected.

Passed: The following path meets requirements by 1.574ns
         The internal maximum frequency of the following component is 412.201 MHz

 Logical Details: Cell type Pin name   Component name

   Destination: FSLICE   CLK   pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248

   Delay: 2.426ns -- based on Minimum Pulse Width

Passed: The following path meets requirements by 3.251ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_pcs_pipe/pipe_top_0/sync1_RxPolarity (from pcie/u1_pcs_pipe/ff_rx_fclk_0 +)
   Destination: FF   Data in   pcie/u1_pcs_pipe/pipe_top_0/sync2_RxPolarity (to pcie/u1_pcs_pipe/ff_rx_fclk_0 +)

   Delay: 0.604ns (45.5% logic, 54.5% route), 1 logic levels.

 Constraint Details:

      0.604ns physical path delay pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248 meets
      4.000ns delay constraint less
      0.000ns skew and
      0.145ns M_SET requirement (totaling 3.855ns) by 3.251ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R42C62B.CLK to   R42C62B.Q0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248 (from pcie/u1_pcs_pipe/ff_rx_fclk_0)
ROUTE   1   0.329   R42C62B.Q0 to   R42C62B.M1 pcie/u1_pcs_pipe/pipe_top_0/sync1_RxPolarity (to pcie/u1_pcs_pipe/ff_rx_fclk_0)

                    0.604   (45.5% logic, 54.5% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   1   3.129 *FF_RX_F_CLK_0 to   R42C62B.CLK pcie/u1_pcs_pipe/ff_rx_fclk_0

                    3.129   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   1   3.129 *FF_RX_F_CLK_0 to   R42C62B.CLK pcie/u1_pcs_pipe/ff_rx_fclk_0

                    3.129   (0.0% logic, 100.0% route), 0 logic levels.

Report: 412.201MHz is the maximum frequency for this preference.

==
Preference: BLOCK PATH FROM PORT "rstn" ;
            119 items scored, 0 timing errors detected.

==
Preference: BLOCK PATH TO PORT "OUT*" ;
            0 items scored, 0 timing errors detected.

==

```
Preference: BLOCK PATH FROM PORT "INP*" ;
            16 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: BLOCK PATH FROM PORT "SRAM_A*" ;
            0 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: BLOCK PATH TO PORT "LED*" ;
            8 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: BLOCK PATH FROM CELL "*ctc_reset_chx*" ;
            14 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*cnt_done_nfts_rx*" 2.000000 X ;
            214 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 10.488ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               5.444ns  (25.9% logic, 74.1% route), 6 logic levels.

 Constraint Details:

      5.444ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 10.488ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R23C70C.CLK to     R23C70C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE         1     1.253     R23C70C.Q1 to     R22C71B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]
CTOF_DEL    ---     0.164     R22C71B.B1 to     R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE        24     0.872     R22C71B.F1 to     R20C72D.D1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL    ---     0.164     R20C72D.D1 to     R20C72D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8024
ROUTE         1     1.058     R20C72D.F1 to     R19C71C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_df26
C0TOFCO_DE  ---     0.423     R19C71C.A0 to    R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE         1     0.000    R19C71C.FCO to    R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.220    R19C72A.FCI to     R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE         1     0.851     R19C72A.F1 to     R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.164     R23C69B.D0 to     R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE         1     0.000     R23C69B.F0 to    R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    5.444   (25.9% logic, 74.1% route), 6 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C70C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C69B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 10.622ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               5.310ns  (24.4% logic, 75.6% route), 6 logic levels.

 Constraint Details:

      5.310ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 10.622ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R23C70C.CLK to     R23C70C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE         1     1.253     R23C70C.Q1 to     R22C71B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]
CTOF_DEL    ---     0.164     R22C71B.B1 to     R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE        24     0.892     R22C71B.F1 to     R19C72B.D1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL    ---     0.164     R19C72B.D1 to     R19C72B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8023
ROUTE         1     1.017     R19C72B.F1 to     R19C71C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_df26
C1TOFCO_DE  ---     0.310     R19C71C.A1 to    R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE         1     0.000    R19C71C.FCO to    R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.220    R19C72A.FCI to     R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE         1     0.851     R19C72A.F1 to     R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.164     R23C69B.D0 to     R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE         1     0.000     R23C69B.F0 to    R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    5.310   (24.4% logic, 75.6% route), 6 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C70C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C69B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 10.629ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[3]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               5.303ns  (35.0% logic, 65.0% route), 13 logic levels.

 Constraint Details:

      5.303ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_977 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 10.629ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_977 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R23C70B.CLK to     R23C70B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_977 (from clk_125_c)
ROUTE         2     1.394     R23C70B.Q1 to     R19C67C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[3]
CTOF_DEL    ---     0.164     R19C67C.A1 to     R19C67C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7800
ROUTE         2     0.370     R19C67C.F1 to     R19C67D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c5_a0_1
CTOF_DEL    ---     0.164     R19C67D.D0 to     R19C67D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_9448
ROUTE         1     0.830     R19C67D.F0 to     R19C69B.A0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c5_i
C0TOFCO_DE  ---     0.423     R19C69B.A0 to    R19C69B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000    R19C69B.FCO to    R19C69C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
```

FCITOFCO_D ---   0.064   R19C69C.FCI to   R19C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE   1   0.000   R19C69C.FCO to   R19C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D ---   0.064   R19C70A.FCI to   R19C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE   1   0.000   R19C70A.FCO to   R19C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D ---   0.064   R19C70B.FCI to   R19C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE   1   0.000   R19C70B.FCO to   R19C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D ---   0.064   R19C70C.FCI to   R19C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE   1   0.000   R19C70C.FCO to   R19C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D ---   0.064   R19C71A.FCI to   R19C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1032
ROUTE   1   0.000   R19C71A.FCO to   R19C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D ---   0.064   R19C71B.FCI to   R19C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1033
ROUTE   1   0.000   R19C71B.FCO to   R19C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D ---   0.064   R19C71C.FCI to   R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE   1   0.000   R19C71C.FCO to   R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE ---   0.220   R19C72A.FCI to   R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE   1   0.851   R19C72A.F1 to   R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL   ---   0.164   R23C69B.D0 to   R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE   1   0.000   R23C69B.F0 to   R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)

                    5.303   (35.0% logic, 65.0% route), 13 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_977:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R23C70B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R23C69B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 10.683ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[4] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx (to clk_125_c +)

   Delay: 5.249ns (26.9% logic, 73.1% route), 6 logic levels.

 Constraint Details:

      5.249ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 10.683ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R23C70C.CLK to   R23C70C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE   1   1.058   R23C70C.Q0 to   R22C71B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[4]
CTOF_DEL   ---   0.164   R22C71B.A1 to   R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE   24   0.872   R22C71B.F1 to   R20C72D.D1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL   ---   0.164   R20C72D.D1 to   R20C72D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8024
ROUTE   1   1.058   R20C72D.F1 to   R19C71C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_df26
C0TOFCO_DE ---   0.423   R19C71C.A0 to   R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE   1   0.000   R19C71C.FCO to   R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE ---   0.220   R19C72A.FCI to   R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE   1   0.851   R19C72A.F1 to   R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL   ---   0.164   R23C69B.D0 to   R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE   1   0.000   R23C69B.F0 to   R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)

                    5.249   (26.9% logic, 73.1% route), 6 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R23C70C.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R23C69B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 10.708ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx (to clk_125_c +)

   Delay: 5.224ns (27.3% logic, 72.7% route), 8 logic levels.

 Constraint Details:

      5.224ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 10.708ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R23C70C.CLK to   R23C70C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE   1   1.253   R23C70C.Q1 to   R22C71B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]
CTOF_DEL   ---   0.164   R22C71B.B1 to   R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE   24   0.892   R22C71B.F1 to   R19C72D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL   ---   0.164   R19C72D.D0 to   R19C72D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8027
ROUTE   1   0.803   R19C72D.F0 to   R19C71A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_lt20
C1TOFCO_DE ---   0.310   R19C71A.B1 to   R19C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1032
ROUTE   1   0.000   R19C71A.FCO to   R19C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D ---   0.064   R19C71B.FCI to   R19C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1033
ROUTE   1   0.000   R19C71B.FCO to   R19C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D ---   0.064   R19C71C.FCI to   R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE   1   0.000   R19C71C.FCO to   R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE ---   0.220   R19C72A.FCI to   R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE   1   0.851   R19C72A.F1 to   R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL   ---   0.164   R23C69B.D0 to   R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE   1   0.000   R23C69B.F0 to   R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)

                    5.224   (27.3% logic, 72.7% route), 8 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R23C70C.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R23C69B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 10.743ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx (to clk_125_c +)

   Delay: 5.189ns (27.2% logic, 72.8% route), 6 logic levels.

 Constraint Details:

      5.189ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 10.743ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275	R23C70C.CLK to	R23C70C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE	1	1.253	R23C70C.Q1 to	R22C71B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]
CTOF_DEL	---	0.164	R22C71B.B1 to	R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE	24	0.872	R22C71B.F1 to	R20C72D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL	---	0.164	R20C72D.D0 to	R20C72D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8024
ROUTE	1	0.803	R20C72D.F0 to	R19C71C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_lt26
C0TOFCO_DE	---	0.423	R19C71C.B0 to	R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE	1	0.000	R19C71C.FCO to	R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE	---	0.220	R19C72A.FCI to	R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE	1	0.851	R19C72A.F1 to	R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL	---	0.164	R23C69B.D0 to	R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE	1	0.000	R23C69B.F0 to	R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
		5.189	(27.2% logic, 72.8% route), 6 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R23C70C.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R23C69B.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Passed: The following path meets requirements by 10.751ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[7] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx (to clk_125_c +)

Delay: 5.181ns (27.2% logic, 72.8% route), 6 logic levels.

Constraint Details:

5.181ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2964 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
16.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 15.932ns) by 10.751ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2964 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275	R23C71C.CLK to	R23C71C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2964 (from clk_125_c)
ROUTE	2	0.830	R23C71C.Q1 to	R22C71D.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[7]
CTOF_DEL	---	0.164	R22C71D.A1 to	R22C71D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7777
ROUTE	22	1.032	R22C71D.F1 to	R20C72D.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_1_0
CTOF_DEL	---	0.164	R20C72D.C1 to	R20C72D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8024
ROUTE	1	1.058	R20C72D.F1 to	R19C71C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_df26
C0TOFCO_DE	---	0.423	R19C71C.A0 to	R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE	1	0.000	R19C71C.FCO to	R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE	---	0.220	R19C72A.FCI to	R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE	1	0.851	R19C72A.F1 to	R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL	---	0.164	R23C69B.D0 to	R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE	1	0.000	R23C69B.F0 to	R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
		5.181	(27.2% logic, 72.8% route), 6 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2964:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R23C71C.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R23C69B.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Passed: The following path meets requirements by 10.760ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx (to clk_125_c +)

Delay: 5.172ns (28.5% logic, 71.5% route), 7 logic levels.

Constraint Details:

5.172ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
16.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 15.932ns) by 10.760ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275	R23C70C.CLK to	R23C70C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE	1	1.253	R23C70C.Q1 to	R22C71B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]
CTOF_DEL	---	0.164	R22C71B.B1 to	R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE	24	0.764	R22C71B.F1 to	R20C71C.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL	---	0.164	R20C71C.C0 to	R20C71C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8026
ROUTE	1	0.830	R20C71C.F0 to	R19C71B.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_lt22
C0TOFCO_DE	---	0.423	R19C71B.A0 to	R19C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1033
ROUTE	1	0.000	R19C71B.FCO to	R19C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D	---	0.064	R19C71C.FCI to	R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE	1	0.000	R19C71C.FCO to	R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE	---	0.220	R19C72A.FCI to	R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE	1	0.851	R19C72A.F1 to	R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL	---	0.164	R23C69B.D0 to	R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE	1	0.000	R23C69B.F0 to	R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
		5.172	(28.5% logic, 71.5% route), 7 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R23C70C.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R23C69B.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Passed: The following path meets requirements by 10.778ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx (to clk_125_c +)

Delay: 5.154ns (26.4% logic, 73.6% route), 7 logic levels.

Constraint Details:

5.154ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
16.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 15.932ns) by 10.778ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

```
   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R23C70C.CLK to     R23C70C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE         1     1.253     R23C70C.Q1 to     R22C71B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]
CTOF_DEL    ---     0.164     R22C71B.B1 to     R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE        24     0.892     R22C71B.F1 to     R19C72C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL    ---     0.164     R19C72C.D1 to     R19C72C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8025
ROUTE         1     0.797     R19C72C.F1 to     R19C71B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_df24
C1TOFCO_DE  ---     0.310     R19C71B.B1 to    R19C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1033
ROUTE         1     0.000    R19C71B.FCO to    R19C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.064    R19C71C.FCI to    R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE         1     0.000    R19C71C.FCO to    R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.220    R19C72A.FCI to     R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE         1     0.851     R19C72A.F1 to     R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.164     R23C69B.D0 to     R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE         1     0.000     R23C69B.F0 to    R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    5.154   (26.4% logic, 73.6% route), 7 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C70C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C69B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 10.817ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[4]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               5.115ns  (25.4% logic, 74.6% route), 6 logic levels.

 Constraint Details:

      5.115ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 10.817ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R23C70C.CLK to     R23C70C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE         1     1.058     R23C70C.Q0 to     R22C71B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[4]
CTOF_DEL    ---     0.164     R22C71B.A1 to     R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE        24     0.892     R22C71B.F1 to     R19C72B.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL    ---     0.164     R19C72B.D1 to     R19C72B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8023
ROUTE         1     1.017     R19C72B.F1 to     R19C71C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_df28
C1TOFCO_DE  ---     0.310     R19C71C.A1 to    R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE         1     0.000    R19C71C.FCO to    R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.220    R19C72A.FCI to     R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE         1     0.851     R19C72A.F1 to     R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.164     R23C69B.D0 to     R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE         1     0.000     R23C69B.F0 to    R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    5.115   (25.4% logic, 74.6% route), 6 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C70C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C69B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


================================================================================
Preference: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*ltssm_nfts_rx_skp*" 2.000000 X ;
            244 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 9.084ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               6.848ns  (20.3% logic, 79.7% route), 7 logic levels.

 Constraint Details:

      6.848ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.084ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R23C70C.CLK to     R23C70C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE         1     1.253     R23C70C.Q1 to     R22C71B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]
CTOF_DEL    ---     0.164     R22C71B.B1 to     R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE        24     0.391     R22C71B.F1 to     R21C71C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL    ---     0.164     R21C71C.D1 to     R21C71C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780
ROUTE        16     0.857     R21C71C.F1 to     R20C72C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i
CTOF_DEL    ---     0.164     R20C72C.B1 to     R20C72C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8142
ROUTE         1     1.692     R20C72C.F1 to     R18C71C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_lt30
C1TOFCO_DE  ---     0.310     R18C71C.A1 to    R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE         1     0.000    R18C71C.FCO to    R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.149    R18C72A.FCI to     R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE         1     1.265     R18C72A.F0 to     R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.164     R21C70A.A0 to     R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE         1     0.000     R21C70A.F0 to    R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    6.848   (20.3% logic, 79.7% route), 7 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C70C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R21C70A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 9.279ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[4]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               6.653ns  (20.9% logic, 79.1% route), 7 logic levels.

 Constraint Details:

      6.653ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     16.000ns delay constraint less
      0.000ns skew and
```

     0.068ns DIN_SET requirement (totaling 15.932ns) by 9.279ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R23C70C.CLK to   R23C70C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE   1   1.058   R23C70C.Q0 to   R22C71B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[4]
CTOF_DEL   ---   0.164   R22C71B.A1 to   R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE   24   0.391   R22C71B.F1 to   R21C71C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL   ---   0.164   R21C71C.D1 to   R21C71C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780
ROUTE   16   0.857   R21C71C.F1 to   R20C72C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i
CTOF_DEL   ---   0.164   R20C72C.B1 to   R20C72C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8142
ROUTE   1   1.692   R20C72C.F1 to   R18C71C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_lt30
C1TOFCO_DE ---   0.310   R18C71C.A1 to   R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE   1   0.000   R18C71C.FCO to   R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE ---   0.149   R18C72A.FCI to   R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE   1   1.265   R18C72A.F0 to   R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL   ---   0.164   R21C70A.A0 to   R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE   1   0.000   R21C70A.F0 to   R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)

                    6.653   (20.9% logic, 79.1% route), 7 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R23C70C.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R21C70A.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 9.295ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

   Delay: 6.637ns (21.9% logic, 78.1% route), 8 logic levels.

 Constraint Details:

      6.637ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.295ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R23C70C.CLK to   R23C70C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE   1   1.253   R23C70C.Q1 to   R22C71B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]
CTOF_DEL   ---   0.164   R22C71B.B1 to   R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE   24   0.391   R22C71B.F1 to   R21C71C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL   ---   0.164   R21C71C.D1 to   R21C71C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780
ROUTE   16   0.857   R21C71C.F1 to   R20C72B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i
CTOF_DEL   ---   0.164   R20C72B.B0 to   R20C72B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8140
ROUTE   1   1.417   R20C72B.F0 to   R18C71B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_df26
C1TOFCO_DE ---   0.310   R18C71B.A1 to   R18C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE   1   0.000   R18C71B.FCO to   R18C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D ---   0.064   R18C71C.FCI to   R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE   1   0.000   R18C71C.FCO to   R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE ---   0.149   R18C72A.FCI to   R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE   1   1.265   R18C72A.F0 to   R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL   ---   0.164   R21C70A.A0 to   R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE   1   0.000   R21C70A.F0 to   R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)

                    6.637   (21.9% logic, 78.1% route), 8 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R23C70C.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R21C70A.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 9.383ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[8] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

   Delay: 6.549ns (21.2% logic, 78.8% route), 7 logic levels.

 Constraint Details:

      6.549ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_980 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.383ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_980 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R23C71B.CLK to   R23C71B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_980 (from clk_125_c)
ROUTE   2   0.803   R23C71B.Q0 to   R22C71A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[8]
CTOF_DEL   ---   0.164   R22C71A.B1 to   R22C71A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7796
ROUTE   2   0.542   R22C71A.F1 to   R21C71C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c8_a0_0
CTOF_DEL   ---   0.164   R21C71C.C1 to   R21C71C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780
ROUTE   16   0.857   R21C71C.F1 to   R20C72C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i
CTOF_DEL   ---   0.164   R20C72C.B1 to   R20C72C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8142
ROUTE   1   1.692   R20C72C.F1 to   R18C71C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_lt30
C1TOFCO_DE ---   0.310   R18C71C.A1 to   R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE   1   0.000   R18C71C.FCO to   R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE ---   0.149   R18C72A.FCI to   R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE   1   1.265   R18C72A.F0 to   R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL   ---   0.164   R21C70A.A0 to   R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE   1   0.000   R21C70A.F0 to   R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)

                    6.549   (21.2% logic, 78.8% route), 7 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_980:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R23C71B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R21C70A.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 9.445ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

   Delay: 6.487ns (26.6% logic, 73.4% route), 12 logic levels.

 Constraint Details:

      6.487ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.445ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R23C70C.CLK to   R23C70C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE   1   1.253   R23C70C.Q1 to   R22C71B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]
CTOF_DEL   ---   0.164   R22C71B.B1 to   R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE   24   0.408   R22C71B.F1 to   R22C71A.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL   ---   0.164   R22C71A.B0 to   R22C71A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7796
ROUTE   7   1.838   R22C71A.F0 to   R18C69C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c8_i
C0TOFCO_DE ---   0.423   R18C69C.B0 to   R18C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE   1   0.000   R18C69C.FCO to   R18C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11]
FCITOFCO_D ---   0.064   R18C70A.FCI to   R18C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE   1   0.000   R18C70A.FCO to   R18C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D ---   0.064   R18C70B.FCI to   R18C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE   1   0.000   R18C70B.FCO to   R18C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D ---   0.064   R18C70C.FCI to   R18C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE   1   0.000   R18C70C.FCO to   R18C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D ---   0.064   R18C71A.FCI to   R18C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1006
ROUTE   1   0.000   R18C71A.FCO to   R18C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D ---   0.064   R18C71B.FCI to   R18C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE   1   0.000   R18C71B.FCO to   R18C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D ---   0.064   R18C71C.FCI to   R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE   1   0.000   R18C71C.FCO to   R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE ---   0.149   R18C72A.FCI to   R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE   1   1.265   R18C72A.F0 to   R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL   ---   0.164   R21C70A.A0 to   R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE   1   0.000   R21C70A.F0 to   R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)

                    6.487   (26.6% logic, 73.4% route), 12 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R23C70C.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R21C70A.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 9.490ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[4] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

   Delay: 6.442ns (22.6% logic, 77.4% route), 8 logic levels.

 Constraint Details:

      6.442ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.490ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R23C70C.CLK to   R23C70C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE   1   1.058   R23C70C.Q0 to   R22C71B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[4]
CTOF_DEL   ---   0.164   R22C71B.A1 to   R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE   24   0.391   R22C71B.F1 to   R21C71C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL   ---   0.164   R21C71C.D1 to   R21C71C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780
ROUTE   16   0.857   R21C71C.F1 to   R20C72B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i
CTOF_DEL   ---   0.164   R20C72B.B0 to   R20C72B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8140
ROUTE   1   1.417   R20C72B.F0 to   R18C71B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_df26
C1TOFCO_DE ---   0.310   R18C71B.A1 to   R18C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE   1   0.000   R18C71B.FCO to   R18C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D ---   0.064   R18C71C.FCI to   R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE   1   0.000   R18C71C.FCO to   R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE ---   0.149   R18C72A.FCI to   R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE   1   1.265   R18C72A.F0 to   R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL   ---   0.164   R21C70A.A0 to   R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE   1   0.000   R21C70A.F0 to   R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)

                    6.442   (22.6% logic, 77.4% route), 8 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R23C70C.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R21C70A.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 9.494ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

   Delay: 6.438ns (26.0% logic, 74.0% route), 13 logic levels.

 Constraint Details:

      6.438ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.494ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R23C70C.CLK to   R23C70C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE   1   1.253   R23C70C.Q1 to   R22C71B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]
CTOF_DEL   ---   0.164   R22C71B.B1 to   R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE   24   0.408   R22C71B.F1 to   R22C71A.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL   ---   0.164   R22C71A.B0 to   R22C71A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7796
ROUTE   7   1.838   R22C71A.F0 to   R18C69B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c8_i
C1TOFCO_DE ---   0.310   R18C69B.B1 to   R18C69B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001
ROUTE   1   0.000   R18C69B.FCO to   R18C69C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[9]
FCITOFCO_D ---   0.064   R18C69C.FCI to   R18C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE   1   0.000   R18C69C.FCO to   R18C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11]
FCITOFCO_D ---   0.064   R18C70A.FCI to   R18C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE   1   0.000   R18C70A.FCO to   R18C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D ---   0.064   R18C70B.FCI to   R18C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE   1   0.000   R18C70B.FCO to   R18C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D ---   0.064   R18C70C.FCI to   R18C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE   1   0.000   R18C70C.FCO to   R18C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D ---   0.064   R18C71A.FCI to   R18C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1006
ROUTE   1   0.000   R18C71A.FCO to   R18C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D ---   0.064   R18C71B.FCI to   R18C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE   1   0.000   R18C71B.FCO to   R18C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D ---   0.064   R18C71C.FCI to   R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE   1   0.000   R18C71C.FCO to   R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE ---   0.149   R18C72A.FCI to   R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE   1   1.265   R18C72A.F0 to   R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL   ---   0.164   R21C70A.A0 to   R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE   1   0.000   R21C70A.F0 to   R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)

                    6.438   (26.0% logic, 74.0% route), 13 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

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   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C70C.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R21C70A.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 9.503ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               6.429ns  (21.6% logic, 78.4% route), 7 logic levels.

 Constraint Details:

      6.429ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.503ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R23C70C.CLK to     R23C70C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE         1     1.253     R23C70C.Q1 to     R22C71B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]
CTOF_DEL    ---     0.164     R22C71B.B1 to     R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE        24     0.391     R22C71B.F1 to     R21C71C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL    ---     0.164     R21C71C.D1 to     R21C71C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780
ROUTE        16     0.857     R21C71C.F1 to     R20C72C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i
CTOF_DEL    ---     0.164     R20C72C.B0 to     R20C72C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8142
ROUTE         1     1.273     R20C72C.F0 to     R18C71C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_df30
C1TOFCO_DE  ---     0.310     R18C71C.B1 to    R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE         1     0.000    R18C71C.FCO to    R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.149    R18C72A.FCI to     R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE         1     1.265     R18C72A.F0 to     R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.164     R21C70A.A0 to     R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE         1     0.000     R21C70A.F0 to    R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
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                      6.429   (21.6% logic, 78.4% route), 7 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C70C.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R21C70A.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 9.531ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               6.401ns  (22.7% logic, 77.3% route), 8 logic levels.

 Constraint Details:

      6.401ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.531ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R23C70C.CLK to     R23C70C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978 (from clk_125_c)
ROUTE         1     1.253     R23C70C.Q1 to     R22C71B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]
CTOF_DEL    ---     0.164     R22C71B.B1 to     R22C71B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7778
ROUTE        24     0.391     R22C71B.F1 to     R21C71C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL    ---     0.164     R21C71C.D1 to     R21C71C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780
ROUTE        16     0.857     R21C71C.F1 to     R20C72B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i
CTOF_DEL    ---     0.164     R20C72B.B1 to     R20C72B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8140
ROUTE         1     1.181     R20C72B.F1 to     R18C71B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_lt26
C1TOFCO_DE  ---     0.310     R18C71B.B1 to    R18C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE         1     0.000    R18C71B.FCO to    R18C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.064    R18C71C.FCI to    R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE         1     0.000    R18C71C.FCO to    R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.149    R18C72A.FCI to     R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE         1     1.265     R18C72A.F0 to     R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.164     R21C70A.A0 to     R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE         1     0.000     R21C70A.F0 to    R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                    --------
                      6.401   (22.7% logic, 77.3% route), 8 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_978:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C70C.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R21C70A.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 9.543ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[7]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               6.389ns  (21.8% logic, 78.2% route), 7 logic levels.

 Constraint Details:

      6.389ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2964 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.543ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2964 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R23C71C.CLK to     R23C71C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2964 (from clk_125_c)
ROUTE         2     0.643     R23C71C.Q1 to     R22C71A.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[7]
CTOF_DEL    ---     0.164     R22C71A.A1 to     R22C71A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7796
ROUTE         2     0.542     R22C71A.F1 to     R21C71C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c8_a0_0
CTOF_DEL    ---     0.164     R21C71C.C1 to     R21C71C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780
ROUTE        16     0.857     R21C71C.F1 to     R20C72C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i
CTOF_DEL    ---     0.164     R20C72C.B1 to     R20C72C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8142
ROUTE         1     1.692     R20C72C.F1 to     R18C71C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_lt30
C1TOFCO_DE  ---     0.310     R18C71C.A1 to    R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE         1     0.000    R18C71C.FCO to    R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.149    R18C72A.FCI to     R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE         1     1.265     R18C72A.F0 to     R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.164     R21C70A.A0 to     R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE         1     0.000     R21C70A.F0 to    R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                    --------
                      6.389   (21.8% logic, 78.2% route), 7 logic levels.
```

```
 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2964:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C71C.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R21C70A.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr*" 6.000000 ns ;
            33 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 4.133ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM1

   Delay:               2.126ns  (12.9% logic, 87.1% route), 2 logic levels.

 Constraint Details:

      2.126ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1386 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.259ns WAD_SET requirement (totaling 6.259ns) by 4.133ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1386:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R37C59C.CLK to     R37C59C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE        12     1.851     R37C59C.Q0 to     R34C61C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL    ---     0.000     R34C61C.A0 to  R34C61C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE         2     0.000  R34C61C.WADO0 to   R34C61B.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT)
                    --------
                      2.126   (12.9% logic, 87.1% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R37C59C.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1386:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R34C61C.CLK clk_125_c
ZERO_DEL    ---     0.000    R34C61C.CLK to   R34C61C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE         2     0.000   R34C61C.WCKO to    R34C61B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT
                    --------
                      1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 4.133ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0

   Delay:               2.126ns  (12.9% logic, 87.1% route), 2 logic levels.

 Constraint Details:

      2.126ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1393 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.259ns WAD_SET requirement (totaling 6.259ns) by 4.133ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1393:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R37C59C.CLK to     R37C59C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE        12     1.851     R37C59C.Q0 to     R34C62C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL    ---     0.000     R34C62C.A0 to  R34C62C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE         2     0.000  R34C62C.WADO0 to   R34C62A.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
                    --------
                      2.126   (12.9% logic, 87.1% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R37C59C.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1393:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R34C62C.CLK clk_125_c
ZERO_DEL    ---     0.000    R34C62C.CLK to   R34C62C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE         2     0.000   R34C62C.WCKO to    R34C62A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
                    --------
                      1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 4.133ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1

   Delay:               2.126ns  (12.9% logic, 87.1% route), 2 logic levels.

 Constraint Details:

      2.126ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1394 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.259ns WAD_SET requirement (totaling 6.259ns) by 4.133ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1394:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R37C59C.CLK to     R37C59C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE        12     1.851     R37C59C.Q0 to     R34C62C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL    ---     0.000     R34C62C.A0 to  R34C62C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE         2     0.000  R34C62C.WADO0 to   R34C62B.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
                    --------
                      2.126   (12.9% logic, 87.1% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R37C59C.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1394:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R34C62C.CLK clk_125_c
ZERO_DEL    ---     0.000    R34C62C.CLK to   R34C62C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE         2     0.000   R34C62C.WCKO to    R34C62B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
                    --------
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                  1.415   (0.0% logic, 100.0% route), 1 logic levels.

Passed: The following path meets requirements by 4.133ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT +)
                   FF   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0

   Delay: 2.126ns (12.9% logic, 87.1% route), 2 logic levels.

 Constraint Details:

     2.126ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385 meets
     6.000ns delay constraint less
     0.000ns skew and
    -0.259ns WAD_SET requirement (totaling 6.259ns) by 4.133ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R37C59C.CLK to   R37C59C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE   12   1.851   R37C59C.Q0 to   R34C61C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL   ---   0.000   R34C61C.A0 to R34C61C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE   2   0.000 R34C61C.WADO0 to   R34C61A.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT)

                  2.126   (12.9% logic, 87.1% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R37C59C.CLK clk_125_c
                  ----
                  1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R34C61C.CLK clk_125_c
ZERO_DEL   ---   0.000   R34C61C.CLK to   R34C61C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE   2   0.000   R34C61C.WCKO to   R34C61A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT

                  1.415   (0.0% logic, 100.0% route), 1 logic levels.

Passed: The following path meets requirements by 4.595ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT +)
                   FF   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/RAM0

   Delay: 1.664ns (16.5% logic, 83.5% route), 2 logic levels.

 Constraint Details:

     1.664ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1388 meets
     6.000ns delay constraint less
     0.000ns skew and
    -0.259ns WAD_SET requirement (totaling 6.259ns) by 4.595ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1388:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R37C59C.CLK to   R37C59C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE   12   1.389   R37C59C.Q0 to   R34C58C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL   ---   0.000   R34C58C.A0 to R34C58C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1387
ROUTE   1   0.000 R34C58C.WADO0 to   R34C58A.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT)

                  1.664   (16.5% logic, 83.5% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R37C59C.CLK clk_125_c
                  ----
                  1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1388:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R34C58C.CLK clk_125_c
ZERO_DEL   ---   0.000   R34C58C.CLK to   R34C58C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1387
ROUTE   2   0.000   R34C58C.WCKO to   R34C58A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT

                  1.415   (0.0% logic, 100.0% route), 1 logic levels.

Passed: The following path meets requirements by 4.630ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT +)
                   FF   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM0

   Delay: 1.629ns (16.9% logic, 83.1% route), 2 logic levels.

 Constraint Details:

     1.629ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1379 meets
     6.000ns delay constraint less
     0.000ns skew and
    -0.259ns WAD_SET requirement (totaling 6.259ns) by 4.630ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1379:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R37C59C.CLK to   R37C59C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE   12   1.354   R37C59C.Q0 to   R39C57C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL   ---   0.000   R39C57C.A0 to R39C57C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1378
ROUTE   2   0.000 R39C57C.WADO0 to   R39C57A.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT)

                  1.629   (16.9% logic, 83.1% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R37C59C.CLK clk_125_c
                  ----
                  1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1379:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R39C57C.CLK clk_125_c
ZERO_DEL   ---   0.000   R39C57C.CLK to   R39C57C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1378
ROUTE   2   0.000   R39C57C.WCKO to   R39C57A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT

                  1.415   (0.0% logic, 100.0% route), 1 logic levels.

Passed: The following path meets requirements by 4.630ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM1 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT +)

   Delay: 1.629ns (16.9% logic, 83.1% route), 2 logic levels.

 Constraint Details:

     1.629ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1380 meets
     6.000ns delay constraint less
     0.000ns skew and
    -0.259ns WAD_SET requirement (totaling 6.259ns) by 4.630ns

 Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1380:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275	R37C59C.CLK to	R37C59C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE	12	1.354	R37C59C.Q0 to	R39C57C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL	---	0.000	R39C57C.A0 to	R39C57C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1378
ROUTE	2	0.000	R39C57C.WADO0 to	R39C57B.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT)
		1.629	(16.9% logic, 83.1% route), 2 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R37C59C.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1380:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R39C57C.CLK clk_125_c
ZERO_DEL	---	0.000	R39C57C.CLK to	R39C57C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1378
ROUTE	2	0.000	R39C57C.WCKO to	R39C57B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT
		1.415	(0.0% logic, 100.0% route), 1 logic levels.	

Passed: The following path meets requirements by 4.644ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0rff_3 (to clk_125_c +)

Delay: 1.288ns (34.1% logic, 65.9% route), 2 logic levels.

Constraint Details:

1.288ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3340 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 4.644ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3340:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275	R37C59C.CLK to	R37C59C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE	11	0.849	R37C59C.Q1 to	R37C58C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
CTOF_DEL	---	0.164	R37C58C.B1 to	R37C58C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3340
ROUTE	1	0.000	R37C58C.F1 to	R37C58C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_33181_0 (to clk_125_c)
		1.288	(34.1% logic, 65.9% route), 2 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R37C59C.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3340:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R37C58C.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Passed: The following path meets requirements by 4.649ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
FF pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0

Delay: 1.610ns (17.1% logic, 82.9% route), 2 logic levels.

Constraint Details:

1.610ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1393 meets
6.000ns delay constraint less
0.000ns skew and
-0.259ns WAD_SET requirement (totaling 6.259ns) by 4.649ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1393:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275	R37C59C.CLK to	R37C59C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE	11	1.335	R37C59C.Q1 to	R34C62C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
ZERO_DEL	---	0.000	R34C62C.B0 to	R34C62C.WADO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE	2	0.000	R34C62C.WADO1 to	R34C62A.WAD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WAD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
		1.610	(17.1% logic, 82.9% route), 2 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R37C59C.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1393:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R34C62C.CLK clk_125_c
ZERO_DEL	---	0.000	R34C62C.CLK to	R34C62C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE	2	0.000	R34C62C.WCKO to	R34C62A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
		1.415	(0.0% logic, 100.0% route), 1 logic levels.	

Passed: The following path meets requirements by 4.649ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
FF pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1

Delay: 1.610ns (17.1% logic, 82.9% route), 2 logic levels.

Constraint Details:

1.610ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1394 meets
6.000ns delay constraint less
0.000ns skew and
-0.259ns WAD_SET requirement (totaling 6.259ns) by 4.649ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1394:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275	R37C59C.CLK to	R37C59C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE	11	1.335	R37C59C.Q1 to	R34C62C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
ZERO_DEL	---	0.000	R34C62C.B0 to	R34C62C.WADO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE	2	0.000	R34C62C.WADO1 to	R34C62B.WAD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WAD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
		1.610	(17.1% logic, 82.9% route), 2 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R37C59C.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1394:

Name	Fanout	Delay (ns)	Site	Resource

```
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R34C62C.CLK clk_125_c
ZERO_DEL    ---     0.000    R34C62C.CLK to   R34C62C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE         2     0.000   R34C62C.WCKO to    R34C62B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
                  --------
                    1.415   (0.0% logic, 100.0% route), 1 logic levels.

Report:  535.619MHz is the maximum frequency for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr*" 6.000000 ns ;
            147 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 2.427ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[8]  (to clk_125_c +)

   Delay:               3.505ns  (17.2% logic, 82.8% route), 3 logic levels.

 Constraint Details:

      3.505ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2760 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 2.427ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2760:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R21C52B.CLK to     R21C52B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE        30     1.866     R21C52B.Q0 to     R12C58A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL    ---     0.164     R12C58A.A0 to     R12C58A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_1/SLICE_1359
ROUTE         1     1.036     R12C58A.F0 to     R16C58A.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0rx[8]
CTOF_DEL    ---     0.164     R16C58A.C1 to     R16C58A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2760
ROUTE         1     0.000     R16C58A.F1 to    R16C58A.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[8] (to clk_125_c)
                  --------
                    3.505   (17.2% logic, 82.8% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2760:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R16C58A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 2.538ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[9]  (to clk_125_c +)

   Delay:               3.394ns  (17.8% logic, 82.2% route), 3 logic levels.

 Constraint Details:

      3.394ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2759 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 2.538ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2759:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R21C52B.CLK to     R21C52B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE        30     1.866     R21C52B.Q0 to     R12C58A.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL    ---     0.164     R12C58A.A1 to     R12C58A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_1/SLICE_1359
ROUTE         1     0.925     R12C58A.F1 to     R15C58B.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0rx[9]
CTOF_DEL    ---     0.164     R15C58B.C1 to     R15C58B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2759
ROUTE         1     0.000     R15C58B.F1 to    R15C58B.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[9] (to clk_125_c)
                  --------
                    3.394   (17.8% logic, 82.2% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2759:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R15C58B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 2.543ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[6]  (to clk_125_c +)

   Delay:               3.389ns  (17.8% logic, 82.2% route), 3 logic levels.

 Constraint Details:

      3.389ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2753 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 2.543ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2753:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R21C52B.CLK to     R21C52B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE        30     1.429     R21C52B.Q0 to     R15C59D.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL    ---     0.164     R15C59D.A1 to     R15C59D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_8273
ROUTE        12     1.357     R15C59D.F1 to     R16C57A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1ror_1
CTOF_DEL    ---     0.164     R16C57A.A0 to     R16C57A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2753
ROUTE         1     0.000     R16C57A.F0 to    R16C57A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[6] (to clk_125_c)
                  --------
                    3.389   (17.8% logic, 82.2% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2753:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R16C57A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 2.543ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[7]  (to clk_125_c +)

   Delay:               3.389ns  (17.8% logic, 82.2% route), 3 logic levels.
```

Constraint Details:

     3.389ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2753 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 2.543ns

Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2753:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R21C52B.CLK to   R21C52B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE   30   1.429   R21C52B.Q0 to   R15C59D.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL   ---   0.164   R15C59D.A1 to   R15C59D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_8273
ROUTE   12   1.357   R15C59D.F1 to   R16C57A.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1ror_1
CTOF_DEL   ---   0.164   R16C57A.A1 to   R16C57A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2753
ROUTE   1   0.000   R16C57A.F1 to   R16C57A.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[7] (to clk_125_c)

                    3.389   (17.8% logic, 82.2% route), 3 logic levels.

Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R21C52B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2753:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R16C57A.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 2.561ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[7] (to clk_125_c +)

   Delay: 3.371ns (17.9% logic, 82.1% route), 3 logic levels.

 Constraint Details:

     3.371ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2757 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 2.561ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2757:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R21C52B.CLK to   R21C52B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE   29   1.878   R21C52B.Q1 to   R15C58A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL   ---   0.164   R15C58A.B1 to   R15C58A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2791
ROUTE   12   0.890   R15C58A.F1 to   R16C56B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0ror_0
CTOF_DEL   ---   0.164   R16C56B.B1 to   R16C56B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2757
ROUTE   1   0.000   R16C56B.F1 to   R16C56B.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[7] (to clk_125_c)

                    3.371   (17.9% logic, 82.1% route), 3 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R21C52B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2757:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R16C56B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 2.561ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[5] (to clk_125_c +)

   Delay: 3.371ns (17.9% logic, 82.1% route), 3 logic levels.

 Constraint Details:

     3.371ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2756 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 2.561ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2756:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R21C52B.CLK to   R21C52B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE   29   1.878   R21C52B.Q1 to   R15C58A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL   ---   0.164   R15C58A.B1 to   R15C58A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2791
ROUTE   12   0.890   R15C58A.F1 to   R16C56C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0ror_0
CTOF_DEL   ---   0.164   R16C56C.B1 to   R16C56C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2756
ROUTE   1   0.000   R16C56C.F1 to   R16C56C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[5] (to clk_125_c)

                    3.371   (17.9% logic, 82.1% route), 3 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R21C52B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2756:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R16C56C.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 2.561ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[4] (to clk_125_c +)

   Delay: 3.371ns (17.9% logic, 82.1% route), 3 logic levels.

 Constraint Details:

     3.371ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2756 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 2.561ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2756:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R21C52B.CLK to   R21C52B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE   29   1.878   R21C52B.Q1 to   R15C58A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL   ---   0.164   R15C58A.B1 to   R15C58A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2791
ROUTE   12   0.890   R15C58A.F1 to   R16C56C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0ror_0
CTOF_DEL   ---   0.164   R16C56C.B0 to   R16C56C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2756
ROUTE   1   0.000   R16C56C.F0 to   R16C56C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[4] (to clk_125_c)

                    3.371   (17.9% logic, 82.1% route), 3 logic levels.

 Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R21C52B.CLK	clk_125_c
		1.415 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2756:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R16C56C.CLK	clk_125_c
		1.415 (0.0% logic, 100.0% route), 0 logic levels.		

Passed: The following path meets requirements by 2.561ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[6] (to clk_125_c +)

Delay: 3.371ns (17.9% logic, 82.1% route), 3 logic levels.

Constraint Details:

3.371ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2757 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 2.561ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2757:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275 R21C52B.CLK to	R21C52B.Q1	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE	29	1.878 R21C52B.Q1 to	R15C58A.B1	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL	---	0.164 R15C58A.B1 to	R15C58A.F1	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2791
ROUTE	12	0.890 R15C58A.F1 to	R16C56B.B0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0ror_0
CTOF_DEL	---	0.164 R16C56B.B0 to	R16C56B.F0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2757
ROUTE	1	0.000 R16C56B.F0 to	R16C56B.DI0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[6] (to clk_125_c)
		3.371 (17.9% logic, 82.1% route), 3 logic levels.		

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R21C52B.CLK	clk_125_c
		1.415 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2757:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R16C56B.CLK	clk_125_c
		1.415 (0.0% logic, 100.0% route), 0 logic levels.		

Passed: The following path meets requirements by 2.570ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[5] (to clk_125_c +)

Delay: 3.362ns (17.9% logic, 82.1% route), 3 logic levels.

Constraint Details:

3.362ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2752 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 2.570ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2752:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275 R21C52B.CLK to	R21C52B.Q0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE	30	1.429 R21C52B.Q0 to	R15C59D.A1	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL	---	0.164 R15C59D.A1 to	R15C59D.F1	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_8273
ROUTE	12	1.330 R15C59D.F1 to	R16C57C.B1	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1ror_1
CTOF_DEL	---	0.164 R16C57C.B1 to	R16C57C.F1	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2752
ROUTE	1	0.000 R16C57C.F1 to	R16C57C.DI1	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[5] (to clk_125_c)
		3.362 (17.9% logic, 82.1% route), 3 logic levels.		

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R21C52B.CLK	clk_125_c
		1.415 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2752:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R16C57C.CLK	clk_125_c
		1.415 (0.0% logic, 100.0% route), 0 logic levels.		

Passed: The following path meets requirements by 2.570ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[4] (to clk_125_c +)

Delay: 3.362ns (17.9% logic, 82.1% route), 3 logic levels.

Constraint Details:

3.362ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2752 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 2.570ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2752:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275 R21C52B.CLK to	R21C52B.Q0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE	30	1.429 R21C52B.Q0 to	R15C59D.A1	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL	---	0.164 R15C59D.A1 to	R15C59D.F1	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_8273
ROUTE	12	1.330 R15C59D.F1 to	R16C57C.B0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1ror_1
CTOF_DEL	---	0.164 R16C57C.B0 to	R16C57C.F0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2752
ROUTE	1	0.000 R16C57C.F0 to	R16C57C.DI0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[4] (to clk_125_c)
		3.362 (17.9% logic, 82.1% route), 3 logic levels.		

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R21C52B.CLK	clk_125_c
		1.415 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2752:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R16C57C.CLK	clk_125_c
		1.415 (0.0% logic, 100.0% route), 0 logic levels.		

Report: 279.877MHz is the maximum frequency for this preference.

==
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr*" 6.000000 ns ;
14 items scored, 0 timing errors detected.

Passed: The following path meets requirements by 4.647ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_eidle_tx (to clk_125_c +)

   Delay: 1.285ns (34.2% logic, 65.8% route), 2 logic levels.

 Constraint Details:

     1.285ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.647ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R10C66B.CLK to   R10C66B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 (from clk_125_c)
ROUTE   5   0.846   R10C66B.Q0 to   R12C66A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]
CTOF_DEL   ---   0.164   R12C66A.A0 to   R12C66A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0
ROUTE   1   0.000   R12C66A.F0 to   R12C66A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/ltssm_eidle_tx (to clk_125_c)

                    1.285   (34.2% logic, 65.8% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R10C66B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R12C66A.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 4.657ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3] (to clk_125_c +)

   Delay: 1.275ns (34.4% logic, 65.6% route), 2 logic levels.

 Constraint Details:

     1.275ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.657ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R11C66B.CLK to   R11C66B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210 (from clk_125_c)
ROUTE   2   0.836   R11C66B.Q0 to   R11C66B.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]
CTOF_DEL   ---   0.164   R11C66B.A0 to   R11C66B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210
ROUTE   1   0.000   R11C66B.F0 to   R11C66B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n3 (to clk_125_c)

                    1.275   (34.4% logic, 65.6% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C66B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C66B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 4.667ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_eidle_tx (to clk_125_c +)

   Delay: 1.265ns (34.7% logic, 65.3% route), 2 logic levels.

 Constraint Details:

     1.265ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.667ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R11C66C.CLK to   R11C66C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 (from clk_125_c)
ROUTE   4   0.826   R11C66C.Q0 to   R12C66A.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]
CTOF_DEL   ---   0.164   R12C66A.B0 to   R12C66A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0
ROUTE   1   0.000   R12C66A.F0 to   R12C66A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/ltssm_eidle_tx (to clk_125_c)

                    1.265   (34.7% logic, 65.3% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C66C.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R12C66A.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 4.785ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_eidle_tx (to clk_125_c +)

   Delay: 1.147ns (38.3% logic, 61.7% route), 2 logic levels.

 Constraint Details:

     1.147ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.785ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R11C66C.CLK to   R11C66C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 (from clk_125_c)
ROUTE   3   0.708   R11C66C.Q1 to   R12C66A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]
CTOF_DEL   ---   0.164   R12C66A.C0 to   R12C66A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0
ROUTE   1   0.000   R12C66A.F0 to   R12C66A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/ltssm_eidle_tx (to clk_125_c)

                    1.147   (38.3% logic, 61.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C66C.CLK clk_125_c
                    ----
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R12C66A.CLK clk_125_c
                    ----
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 4.867ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1] (to clk_125_c +)

   Delay: 1.065ns (41.2% logic, 58.8% route), 2 logic levels.

 Constraint Details:

      1.065ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.867ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R11C66C.CLK to   R11C66C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 (from clk_125_c)
ROUTE   4   0.626   R11C66C.Q0 to   R11C66C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]
CTOF_DEL   ---   0.164   R11C66C.A0 to   R11C66C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209
ROUTE   1   0.000   R11C66C.F0 to   R11C66C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n1 (to clk_125_c)

                      1.065   (41.2% logic, 58.8% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C66C.CLK clk_125_c
                    ----
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C66C.CLK clk_125_c
                    ----
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 4.882ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2] (to clk_125_c +)

   Delay: 1.050ns (41.8% logic, 58.2% route), 2 logic levels.

 Constraint Details:

      1.050ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.882ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R11C66C.CLK to   R11C66C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 (from clk_125_c)
ROUTE   4   0.611   R11C66C.Q0 to   R11C66C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]
CTOF_DEL   ---   0.164   R11C66C.B1 to   R11C66C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209
ROUTE   1   0.000   R11C66C.F1 to   R11C66C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n2 (to clk_125_c)

                      1.050   (41.8% logic, 58.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C66C.CLK clk_125_c
                    ----
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C66C.CLK clk_125_c
                    ----
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 4.894ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3] (to clk_125_c +)

   Delay: 1.038ns (42.3% logic, 57.7% route), 2 logic levels.

 Constraint Details:

      1.038ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.894ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R11C66C.CLK to   R11C66C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 (from clk_125_c)
ROUTE   4   0.599   R11C66C.Q0 to   R11C66B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]
CTOF_DEL   ---   0.164   R11C66B.B0 to   R11C66B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210
ROUTE   1   0.000   R11C66B.F0 to   R11C66B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n3 (to clk_125_c)

                      1.038   (42.3% logic, 57.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C66C.CLK clk_125_c
                    ----
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C66B.CLK clk_125_c
                    ----
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 4.961ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2] (to clk_125_c +)

   Delay: 0.971ns (45.2% logic, 54.8% route), 2 logic levels.

 Constraint Details:

      0.971ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 meets

```
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.961ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R10C66B.CLK to     R10C66B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 (from clk_125_c)
ROUTE         5     0.532     R10C66B.Q0 to     R11C66C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]
CTOF_DEL    ---     0.164     R11C66C.C1 to     R11C66C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209
ROUTE         1     0.000     R11C66C.F1 to    R11C66C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n2 (to clk_125_c)
                  --------
                    0.971   (45.2% logic, 54.8% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R10C66B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C66C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.961ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]  (to clk_125_c +)

   Delay:               0.971ns  (45.2% logic, 54.8% route), 2 logic levels.

 Constraint Details:

      0.971ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.961ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R10C66B.CLK to     R10C66B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 (from clk_125_c)
ROUTE         5     0.532     R10C66B.Q0 to     R11C66C.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]
CTOF_DEL    ---     0.164     R11C66C.C0 to     R11C66C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209
ROUTE         1     0.000     R11C66C.F0 to    R11C66C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n1 (to clk_125_c)
                  --------
                    0.971   (45.2% logic, 54.8% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R10C66B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C66C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.994ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]  (to clk_125_c +)

   Delay:               0.938ns  (46.8% logic, 53.2% route), 2 logic levels.

 Constraint Details:

      0.938ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.994ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R11C66C.CLK to     R11C66C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 (from clk_125_c)
ROUTE         3     0.499     R11C66C.Q1 to     R11C66B.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]
CTOF_DEL    ---     0.164     R11C66B.C0 to     R11C66B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210
ROUTE         1     0.000     R11C66B.F0 to    R11C66B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n3 (to clk_125_c)
                  --------
                    0.938   (46.8% logic, 53.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C66C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C66B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Report:  739.098MHz is the maximum frequency for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr*" 6.000000 ns ;
            18 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 4.137ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en  (to clk_125_c +)

   Delay:               1.795ns  (33.6% logic, 66.4% route), 3 logic levels.

 Constraint Details:

      1.795ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.137ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R11C67C.CLK to     R11C67C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 (from clk_125_c)
ROUTE         4     0.813     R11C67C.Q0 to     R11C66A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]
CTOF_DEL    ---     0.164     R11C66A.B1 to     R11C66A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207
ROUTE         1     0.379     R11C66A.F1 to     R11C66A.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en4_NE_i
CTOF_DEL    ---     0.164     R11C66A.B0 to     R11C66A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207
ROUTE         1     0.000     R11C66A.F0 to    R11C66A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/N_33323_0 (to clk_125_c)
                  --------
                    1.795   (33.6% logic, 66.4% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:
```

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C67C.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C66A.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.307ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en  (to clk_125_c +)

   Delay:               1.625ns  (37.1% logic, 62.9% route), 3 logic levels.

 Constraint Details:

     1.625ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.307ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R11C67B.CLK to     R11C67B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 (from clk_125_c)
ROUTE         6     0.643     R11C67B.Q0 to     R11C66A.A1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]
CTOF_DEL    ---     0.164     R11C66A.A1 to     R11C66A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207
ROUTE         1     0.379     R11C66A.F1 to     R11C66A.B0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en4_NE_i
CTOF_DEL    ---     0.164     R11C66A.B0 to     R11C66A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207
ROUTE         1     0.000     R11C66A.F0 to    R11C66A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/N_33323_0 (to clk_125_c)
                    --------
                      1.625   (37.1% logic, 62.9% route), 3 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C67B.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C66A.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.368ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en  (to clk_125_c +)

   Delay:               1.564ns  (38.6% logic, 61.4% route), 3 logic levels.

 Constraint Details:

     1.564ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.368ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R11C67C.CLK to     R11C67C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 (from clk_125_c)
ROUTE         3     0.582     R11C67C.Q1 to     R11C66A.D1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]
CTOF_DEL    ---     0.164     R11C66A.D1 to     R11C66A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207
ROUTE         1     0.379     R11C66A.F1 to     R11C66A.B0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en4_NE_i
CTOF_DEL    ---     0.164     R11C66A.B0 to     R11C66A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207
ROUTE         1     0.000     R11C66A.F0 to    R11C66A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/N_33323_0 (to clk_125_c)
                    --------
                      1.564   (38.6% logic, 61.4% route), 3 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C67C.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C66A.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.422ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en  (to clk_125_c +)

   Delay:               1.510ns  (39.9% logic, 60.1% route), 3 logic levels.

 Constraint Details:

     1.510ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.422ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R11C67B.CLK to     R11C67B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 (from clk_125_c)
ROUTE         5     0.528     R11C67B.Q1 to     R11C66A.C1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]
CTOF_DEL    ---     0.164     R11C66A.C1 to     R11C66A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207
ROUTE         1     0.379     R11C66A.F1 to     R11C66A.B0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en4_NE_i
CTOF_DEL    ---     0.164     R11C66A.B0 to     R11C66A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207
ROUTE         1     0.000     R11C66A.F0 to    R11C66A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/N_33323_0 (to clk_125_c)
                    --------
                      1.510   (39.9% logic, 60.1% route), 3 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C67B.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3207:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C66A.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.862ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]  (to clk_125_c +)

   Delay:               1.070ns  (41.0% logic, 59.0% route), 2 logic levels.
```

Constraint Details:

     1.070ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.862ns

Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R11C67B.CLK to   R11C67B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 (from clk_125_c)
ROUTE   6   0.631   R11C67B.Q0 to   R11C67C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]
CTOF_DEL   ---   0.164   R11C67C.A1 to   R11C67C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236
ROUTE   1   0.000   R11C67C.F1 to   R11C67C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[3] (to clk_125_c)

                    1.070   (41.0% logic, 59.0% route), 2 logic levels.

Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C67B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C67C.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 4.865ns

Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2] (to clk_125_c +)

   Delay: 1.067ns (41.1% logic, 58.9% route), 2 logic levels.

Constraint Details:

     1.067ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.865ns

Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R11C67B.CLK to   R11C67B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 (from clk_125_c)
ROUTE   5   0.628   R11C67B.Q1 to   R11C67C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]
CTOF_DEL   ---   0.164   R11C67C.B0 to   R11C67C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236
ROUTE   1   0.000   R11C67C.F0 to   R11C67C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[2] (to clk_125_c)

                    1.067   (41.1% logic, 58.9% route), 2 logic levels.

Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C67B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C67C.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 4.865ns

Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3] (to clk_125_c +)

   Delay: 1.067ns (41.1% logic, 58.9% route), 2 logic levels.

Constraint Details:

     1.067ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.865ns

Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R11C67B.CLK to   R11C67B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 (from clk_125_c)
ROUTE   5   0.628   R11C67B.Q1 to   R11C67C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]
CTOF_DEL   ---   0.164   R11C67C.B1 to   R11C67C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236
ROUTE   1   0.000   R11C67C.F1 to   R11C67C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[3] (to clk_125_c)

                    1.067   (41.1% logic, 58.9% route), 2 logic levels.

Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C67B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C67C.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 4.939ns

Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT +)

   Delay: 1.320ns (20.8% logic, 79.2% route), 2 logic levels.

Constraint Details:

     1.320ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
     6.000ns delay constraint less
     0.000ns skew and
    -0.259ns WAD_SET requirement (totaling 6.259ns) by 4.939ns

Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.275   R11C67B.CLK to   R11C67B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 (from clk_125_c)
ROUTE   6   1.045   R11C67B.Q0 to   R12C66C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]
ZERO_DEL   ---   0.000   R12C66C.A0 to R12C66C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE   1   0.000 R12C66C.WADO0 to   R12C66A.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT)

                    1.320   (20.8% logic, 79.2% route), 2 logic levels.

Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   1.415 *FF_TX_H_CLK_0 to   R11C67B.CLK clk_125_c
                  ----
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R12C66C.CLK clk_125_c
ZERO_DEL    ---     0.000    R12C66C.CLK to   R12C66C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         2     0.000   R12C66C.WCKO to    R12C66A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT
                  --------
                    1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 4.954ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT +)

   Delay:               1.305ns  (21.1% logic, 78.9% route), 2 logic levels.

 Constraint Details:

      1.305ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.259ns WAD_SET requirement (totaling 6.259ns) by 4.954ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R11C67B.CLK to     R11C67B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 (from clk_125_c)
ROUTE         5     1.030     R11C67B.Q1 to     R12C66C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]
ZERO_DEL    ---     0.000     R12C66C.B0 to  R12C66C.WADO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         1     0.000  R12C66C.WADO1 to   R12C66A.WAD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WAD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT)
                  --------
                    1.305   (21.1% logic, 78.9% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C67B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R12C66C.CLK clk_125_c
ZERO_DEL    ---     0.000    R12C66C.CLK to   R12C66C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         2     0.000   R12C66C.WCKO to    R12C66A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT
                  --------
                    1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 5.013ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]  (to clk_125_c +)

   Delay:               0.919ns  (47.8% logic, 52.2% route), 2 logic levels.

 Constraint Details:

      0.919ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 5.013ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R11C67C.CLK to     R11C67C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 (from clk_125_c)
ROUTE         3     0.480     R11C67C.Q1 to     R11C67C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]
CTOF_DEL    ---     0.164     R11C67C.C1 to     R11C67C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236
ROUTE         1     0.000     R11C67C.F1 to    R11C67C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[3] (to clk_125_c)
                  --------
                    0.919   (47.8% logic, 52.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C67C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R11C67C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Report:  536.769MHz is the maximum frequency for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data*" 6.000000 ns ;
            16 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 3.598ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[13]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM0

   Delay:               2.558ns  (17.2% logic, 82.8% route), 3 logic levels.

 Constraint Details:

      2.558ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2770 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1382 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.156ns WD_SET requirement (totaling 6.156ns) by 3.598ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2770 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1382:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R34C60C.CLK to     R34C60C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2770 (from clk_125_c)
ROUTE         1     1.129     R34C60C.Q1 to     R38C58D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[13]
CTOF_DEL    ---     0.164     R38C58D.B0 to     R38C58D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9489
ROUTE         1     0.990     R38C58D.F0 to     R39C58C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_214
ZERO_DEL    ---     0.000     R39C58C.B1 to   R39C58C.WDO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1381
ROUTE         1     0.000   R39C58C.WDO1 to    R39C58A.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT)
                  --------
                    2.558   (17.2% logic, 82.8% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2770:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R34C60C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1382:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R39C58C.CLK clk_125_c
ZERO_DEL    ---     0.000    R39C58C.CLK to   R39C58C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1381
ROUTE         2     0.000   R39C58C.WCKO to    R39C58A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT
                  --------
                    1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 3.671ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[12]  (from clk_125_c +)
```

```
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM0

   Delay:               2.485ns  (17.7% logic, 82.3% route), 3 logic levels.

 Constraint Details:

      2.485ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2770 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1382 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.156ns WD_SET requirement (totaling 6.156ns) by 3.671ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2770 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1382:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R34C60C.CLK to     R34C60C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2770 (from clk_125_c)
ROUTE         1     1.029     R34C60C.Q0 to     R38C59B.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[12]
CTOF_DEL    ---     0.164     R38C59B.C0 to     R38C59B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9490
ROUTE         1     1.017     R38C59B.F0 to     R39C58C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_213
ZERO_DEL    ---     0.000     R39C58C.A1 to   R39C58C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1381
ROUTE         1     0.000   R39C58C.WDO0 to    R39C58A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT)
                  --------
                    2.485   (17.7% logic, 82.3% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2770:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R34C60C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1382:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R39C58C.CLK clk_125_c
ZERO_DEL    ---     0.000    R39C58C.CLK to   R39C58C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1381
ROUTE         2     0.000   R39C58C.WCKO to    R39C58A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT
                  --------
                    1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 4.051ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0

   Delay:               2.105ns  (20.9% logic, 79.1% route), 3 logic levels.

 Constraint Details:

      2.105ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2764 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1393 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.156ns WD_SET requirement (totaling 6.156ns) by 4.051ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2764 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1393:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R33C60C.CLK to     R33C60C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2764 (from clk_125_c)
ROUTE         1     0.588     R33C60C.Q1 to     R32C60D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[1]
CTOF_DEL    ---     0.164     R32C60D.B0 to     R32C60D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9501
ROUTE         1     1.078     R32C60D.F0 to     R34C62C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_202
ZERO_DEL    ---     0.000     R34C62C.B1 to   R34C62C.WDO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE         1     0.000   R34C62C.WDO1 to    R34C62A.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
                  --------
                    2.105   (20.9% logic, 79.1% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2764:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R33C60C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1393:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R34C62C.CLK clk_125_c
ZERO_DEL    ---     0.000    R34C62C.CLK to   R34C62C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE         2     0.000   R34C62C.WCKO to    R34C62A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
                  --------
                    1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 4.076ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[5]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0

   Delay:               2.080ns  (21.1% logic, 78.9% route), 3 logic levels.

 Constraint Details:

      2.080ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2766 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1390 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.156ns WD_SET requirement (totaling 6.156ns) by 4.076ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2766 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1390:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R36C60B.CLK to     R36C60B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2766 (from clk_125_c)
ROUTE         1     0.838     R36C60B.Q1 to     R39C60B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[5]
CTOF_DEL    ---     0.164     R39C60B.B0 to     R39C60B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9497
ROUTE         1     0.803     R39C60B.F0 to     R39C59C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_206
ZERO_DEL    ---     0.000     R39C59C.B1 to   R39C59C.WDO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1389
ROUTE         1     0.000   R39C59C.WDO1 to    R39C59A.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
                  --------
                    2.080   (21.1% logic, 78.9% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2766:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R36C60B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1390:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R39C59C.CLK clk_125_c
ZERO_DEL    ---     0.000    R39C59C.CLK to   R39C59C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1389
ROUTE         2     0.000   R39C59C.WCKO to    R39C59A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
                  --------
                    1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 4.085ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0

   Delay:               2.071ns  (21.2% logic, 78.8% route), 3 logic levels.

 Constraint Details:

      2.071ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2764 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1393 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.156ns WD_SET requirement (totaling 6.156ns) by 4.085ns

 Physical Path Details:
```

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2764 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1393:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275	R33C60C.CLK to	R33C60C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2764 (from clk_125_c)
ROUTE	1	0.615	R33C60C.Q0 to	R34C60A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[0]
CTOF_DEL	---	0.164	R34C60A.A0 to	R34C60A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9502
ROUTE	1	1.017	R34C60A.F0 to	R34C62C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_201
ZERO_DEL	---	0.000	R34C62C.A1 to	R34C62C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE	1	0.000	R34C62C.WDO0 to	R34C62A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
		2.071	(21.2% logic, 78.8% route), 3 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2764:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R33C60C.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1393:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R34C62C.CLK clk_125_c
ZERO_DEL	---	0.000	R34C62C.CLK to	R34C62C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE	2	0.000	R34C62C.WCKO to	R34C62A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
		1.415	(0.0% logic, 100.0% route), 1 logic levels.	

Passed: The following path meets requirements by 4.248ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source:	FF	Q	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[15] (from clk_125_c +)
Destination:	FF	Data in	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM1 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT +)
	FF		pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM1

Delay: 1.908ns (23.0% logic, 77.0% route), 3 logic levels.

Constraint Details:

1.908ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2771 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1383 meets
6.000ns delay constraint less
0.000ns skew and
-0.156ns WD_SET requirement (totaling 6.156ns) by 4.248ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2771 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1383:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275	R32C59A.CLK to	R32C59A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2771 (from clk_125_c)
ROUTE	1	0.898	R32C59A.Q1 to	R38C58A.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[15]
CTOF_DEL	---	0.164	R38C58A.B0 to	R38C58A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9487
ROUTE	1	0.571	R38C58A.F0 to	R39C58C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_216
ZERO_DEL	---	0.000	R39C58C.D1 to	R39C58C.WDO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1381
ROUTE	1	0.000	R39C58C.WDO3 to	R39C58B.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT)
		1.908	(23.0% logic, 77.0% route), 3 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2771:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R32C59A.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1383:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R39C58C.CLK clk_125_c
ZERO_DEL	---	0.000	R39C58C.CLK to	R39C58C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1381
ROUTE	2	0.000	R39C58C.WCKO to	R39C58B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT
		1.415	(0.0% logic, 100.0% route), 1 logic levels.	

Passed: The following path meets requirements by 4.260ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source:	FF	Q	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[14] (from clk_125_c +)
Destination:	FF	Data in	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM1 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT +)
	FF		pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM1

Delay: 1.896ns (23.2% logic, 76.8% route), 3 logic levels.

Constraint Details:

1.896ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2771 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1383 meets
6.000ns delay constraint less
0.000ns skew and
-0.156ns WD_SET requirement (totaling 6.156ns) by 4.260ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2771 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1383:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275	R32C59A.CLK to	R32C59A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2771 (from clk_125_c)
ROUTE	1	1.178	R32C59A.Q0 to	R39C58D.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[14]
CTOF_DEL	---	0.164	R39C58D.A0 to	R39C58D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9488
ROUTE	1	0.279	R39C58D.F0 to	R39C58C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_215
ZERO_DEL	---	0.000	R39C58C.C1 to	R39C58C.WDO2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1381
ROUTE	1	0.000	R39C58C.WDO2 to	R39C58B.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT)
		1.896	(23.2% logic, 76.8% route), 3 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2771:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R32C59A.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1383:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R39C58C.CLK clk_125_c
ZERO_DEL	---	0.000	R39C58C.CLK to	R39C58C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1381
ROUTE	2	0.000	R39C58C.WCKO to	R39C58B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT
		1.415	(0.0% logic, 100.0% route), 1 logic levels.	

Passed: The following path meets requirements by 4.262ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source:	FF	Q	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[8] (from clk_125_c +)
Destination:	FF	Data in	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT +)
	FF		pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0

Delay: 1.894ns (23.2% logic, 76.8% route), 3 logic levels.

Constraint Details:

1.894ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385 meets
6.000ns delay constraint less
0.000ns skew and
-0.156ns WD_SET requirement (totaling 6.156ns) by 4.262ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275	R36C60C.CLK to	R36C60C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768 (from clk_125_c)
ROUTE	1	0.362	R36C60C.Q0 to	R36C60A.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[8]
CTOF_DEL	---	0.164	R36C60A.D0 to	R36C60A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9494
ROUTE	1	1.093	R36C60A.F0 to	R34C61C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m_i_m2[8]
ZERO_DEL	---	0.000	R34C61C.A1 to	R34C61C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE	1	0.000	R34C61C.WDO0 to	R34C61A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT)
		1.894	(23.2% logic, 76.8% route), 3 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R36C60C.CLK	clk_125_c
		1.415 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R34C61C.CLK	clk_125_c
ZERO_DEL	---	0.000 R34C61C.CLK to	R34C61C.WCKO	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE	2	0.000 R34C61C.WCKO to	R34C61A.WCK	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT
		1.415 (0.0% logic, 100.0% route), 1 logic levels.		

Passed: The following path meets requirements by 4.305ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[9] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT +)
FF pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0

Delay: 1.851ns (23.7% logic, 76.3% route), 3 logic levels.

Constraint Details:

1.851ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385 meets
6.000ns delay constraint less
0.000ns skew and
-0.156ns WD_SET requirement (totaling 6.156ns) by 4.305ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275 R36C60C.CLK to	R36C60C.Q1	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768 (from clk_125_c)
ROUTE	1	0.615 R36C60C.Q1 to	R34C60D.D0	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[9]
CTOF_DEL	---	0.164 R34C60D.D0 to	R34C60D.F0	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9493
ROUTE	1	0.797 R34C60D.F0 to	R34C61C.B1	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_210
ZERO_DEL	---	0.000 R34C61C.B1 to	R34C61C.WDO1	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE	1	0.000 R34C61C.WDO1 to	R34C61A.WD1	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT)
		1.851 (23.7% logic, 76.3% route), 3 logic levels.		

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R36C60C.CLK	clk_125_c
		1.415 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R34C61C.CLK	clk_125_c
ZERO_DEL	---	0.000 R34C61C.CLK to	R34C61C.WCKO	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE	2	0.000 R34C61C.WCKO to	R34C61A.WCK	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT
		1.415 (0.0% logic, 100.0% route), 1 logic levels.		

Passed: The following path meets requirements by 4.317ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[6] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT +)
FF pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1

Delay: 1.839ns (23.9% logic, 76.1% route), 3 logic levels.

Constraint Details:

1.839ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2767 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391 meets
6.000ns delay constraint less
0.000ns skew and
-0.156ns WD_SET requirement (totaling 6.156ns) by 4.317ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2767 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275 R36C59A.CLK to	R36C59A.Q0	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2767 (from clk_125_c)
ROUTE	1	0.703 R36C59A.Q0 to	R38C59D.C0	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[6]
CTOF_DEL	---	0.164 R38C59D.C0 to	R38C59D.F0	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9496
ROUTE	1	0.697 R38C59D.F0 to	R39C59C.C1	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_207
ZERO_DEL	---	0.000 R39C59C.C1 to	R39C59C.WDO2	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE	1	0.000 R39C59C.WDO2 to	R39C59B.WD0	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT)
		1.839 (23.9% logic, 76.1% route), 3 logic levels.		

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2767:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R36C59A.CLK	clk_125_c
		1.415 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R39C59C.CLK	clk_125_c
ZERO_DEL	---	0.000 R39C59C.CLK to	R39C59C.WCKO	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE	2	0.000 R39C59C.WCKO to	R39C59B.WCK	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT
		1.415 (0.0% logic, 100.0% route), 1 logic levels.		

Report: 416.320MHz is the maximum frequency for this preference.

==
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl*" 6.000000 ns ;
2 items scored, 0 timing errors detected.

Passed: The following path meets requirements by 3.566ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl[1] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT +)
FF pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM0

Delay: 2.590ns (16.9% logic, 83.1% route), 3 logic levels.

Constraint Details:

2.590ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1379 meets
6.000ns delay constraint less
0.000ns skew and
-0.156ns WD_SET requirement (totaling 6.156ns) by 3.566ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1379:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275 R32C59B.CLK to	R32C59B.Q1	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773 (from clk_125_c)
ROUTE	1	1.280 R32C59B.Q1 to	R36C58D.C0	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_kcntl_16[1]
CTOF_DEL	---	0.164 R36C58D.C0 to	R36C58D.F0	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9503
ROUTE	1	0.871 R36C58D.F0 to	R39C57C.A1	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_200
ZERO_DEL	---	0.000 R39C57C.A1 to	R39C57C.WDO0	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1378
ROUTE	1	0.000 R39C57C.WDO0 to	R39C57A.WD0	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT)
		2.590 (16.9% logic, 83.1% route), 3 logic levels.		

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415 *FF_TX_H_CLK_0 to	R32C59B.CLK	clk_125_c
		1.415 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1379:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R39C57C.CLK clk_125_c
ZERO_DEL	---	0.000	R39C57C.CLK to	R39C57C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1378
ROUTE	2	0.000	R39C57C.WCKO to	R39C57A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT
		1.415	(0.0% logic, 100.0% route), 1 logic levels.	

Passed: The following path meets requirements by 4.299ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source:	FF	Q	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl[0] (from clk_125_c +)
Destination:	FF	Data in	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT +)
	FF		pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/RAM0

Delay: 1.857ns (23.6% logic, 76.4% route), 3 logic levels.

Constraint Details:

1.857ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1388 meets
6.000ns delay constraint less
0.000ns skew and
-0.156ns WD_SET requirement (totaling 6.156ns) by 4.299ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1388:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.275	R32C59B.CLK to	R32C59B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773 (from clk_125_c)
ROUTE	1	0.803	R32C59B.Q0 to	R34C58D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_kcntl_16[0]
CTOF_DEL	---	0.164	R34C58D.B0 to	R34C58D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9504
ROUTE	1	0.615	R34C58D.F0 to	R34C58C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_199
ZERO_DEL	---	0.000	R34C58C.A1 to	R34C58C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1387
ROUTE	1	0.000	R34C58C.WDO0 to	R34C58A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT)
		1.857	(23.6% logic, 76.4% route), 3 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R32C59B.CLK clk_125_c
		1.415	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1388:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	1.415	*FF_TX_H_CLK_0 to	R34C58C.CLK clk_125_c
ZERO_DEL	---	0.000	R34C58C.CLK to	R34C58C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1387
ROUTE	2	0.000	R34C58C.WCKO to	R34C58A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT
		1.415	(0.0% logic, 100.0% route), 1 logic levels.	

Report: 410.846MHz is the maximum frequency for this preference.

Report Summary

Preference	Constraint	Actual	Levels
FREQUENCY NET "clk_125_c" 125.000000 MHz ;	125.000 MHz	125.960 MHz	6
FREQUENCY NET "can_clk_c" 25.000000 MHz ;	25.000 MHz	34.524 MHz	4
FREQUENCY NET "uart_clk_c" 25.000000 MHz ;	25.000 MHz	34.341 MHz	2
FREQUENCY NET "pcie/pclk" 250.000000 MHz ;	250.000 MHz	279.174 MHz	4
FREQUENCY NET "pcie/u1_pcs_pipe/ff_rx_fclk_0" 250.000000 MHz ;	250.000 MHz	412.201 MHz	1
MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*cnt_done_nfts_rx*" 2.000000 X ;	16.000 ns	5.512 ns	6
MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*ltssm_nfts_rx_skp*" 2.000000 X ;	16.000 ns	6.916 ns	7
MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr*" 6.000000 ns ;	166.667 MHz	535.619 MHz	2
MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr*" 6.000000 ns ;	166.667 MHz	279.877 MHz	3
MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr*" 6.000000 ns ;	166.667 MHz	739.098 MHz	2
MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr*" 6.000000 ns ;	166.667 MHz	536.769 MHz	3
MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data*" 6.000000 ns ;	166.667 MHz	416.320 MHz	3
MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl*" 6.000000 ns ;	166.667 MHz	410.846 MHz	3

All preferences were met.

Clock Domains Analysis

Found 8 clocks:

Clock Domain: clk_125_c Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0 Loads: 3188
Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ;
Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr*" 6.000000 ns ;
Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr*" 6.000000 ns ;
Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data*" 6.000000 ns ;
Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl*" 6.000000 ns ;
Covered under: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*cnt_done_nfts_rx*" 2.000000 X ;
Covered under: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*ltssm_nfts_rx_skp*" 2.000000 X ;
Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr*" 6.000000 ns ;
Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr*" 6.000000 ns ;

Data transfers from:
Clock Domain: can_clk_c Source: pll_can/PLLInst_0.CLKOP
Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ; Transfers: 10

Clock Domain: uart_clk_c Source: pll_uarts/PLLInst_0.CLKOP
Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ; Transfers: 60

Clock Domain: pcie/pclk Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_F_CLK_0
Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ; Transfers: 37

Clock Domain: jtaghub16_jtck Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: can_clk_c Source: pll_can/PLLInst_0.CLKOP Loads: 404
Covered under: FREQUENCY NET "can_clk_c" 25.000000 MHz ;

Data transfers from:
Clock Domain: clk_125_c Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
Covered under: FREQUENCY NET "can_clk_c" 25.000000 MHz ; Transfers: 35

Clock Domain: jtaghub16_jtck Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: uart_clk_c Source: pll_uarts/PLLInst_0.CLKOP Loads: 1181
Covered under: FREQUENCY NET "uart_clk_c" 25.000000 MHz ;

Data transfers from:
Clock Domain: clk_125_c Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0

```
      Covered under: FREQUENCY NET "uart_clk_c" 25.000000 MHz ;   Transfers: 22

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: pcie/pclk   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_F_CLK_0   Loads: 192
   Covered under: FREQUENCY NET "pcie/pclk" 250.000000 MHz ;
   Blocked under: BLOCK PATH FROM CELL "*ctc_reset_chx*" ;

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
      Covered under: FREQUENCY NET "pcie/pclk" 250.000000 MHz ;   Transfers: 41

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: pcie/u1_pcs_pipe/ff_rx_fclk_0   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_RX_F_CLK_0   Loads: 1
   Covered under: FREQUENCY NET "pcie/u1_pcs_pipe/ff_rx_fclk_0" 250.000000 MHz ;

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
      Not reported because source and destination domains are unrelated.

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK   Loads: 416
   No transfer within this clock domain is found

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0

   Clock Domain: pcie/pclk   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_F_CLK_0

Clock Domain: ep5cht/rdcnt_inferred_clock_9   Source: ep5cht/SLICE_1095.Q0   Loads: 23
   No transfer within this clock domain is found

Clock Domain: ep5cht/lclk   Source: ep5cht/losc/SLICE_7941.F0   Loads: 10
   No transfer within this clock domain is found


Timing summary (Setup):
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Timing errors: 0  Score: 0
Cumulative negative slack: 0

Constraints cover 184729 paths, 104 nets, and 62958 connections (96.1% coverage)

--------------------------------------------------------------------------------
Lattice TRACE Report - Hold, Version Diamond Version 2.0.0.154
Thu Feb 27 11:57:25 2014

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Report Information
------------------
Command line:    trce -v 10 -gt -sethld -sp 7 -sphld m -o top_impl1.twr top_impl1.ncd top_impl1.prf
Design file:     top_impl1.ncd
Preference file: top_impl1.prf
Device,speed:    LFE3-35EA,m
Report level:    verbose report, limited to 10 items per preference
--------------------------------------------------------------------------------

Preference Summary

• FREQUENCY NET "clk_125_c" 125.000000 MHz (0 errors)
            4096 items scored, 0 timing errors detected.

• FREQUENCY NET "can_clk_c" 25.000000 MHz (0 errors)
            4096 items scored, 0 timing errors detected.

• FREQUENCY NET "uart_clk_c" 25.000000 MHz (0 errors)
            4096 items scored, 0 timing errors detected.

• FREQUENCY NET "pcie/pclk" 250.000000 MHz (0 errors)
            987 items scored, 0 timing errors detected.

• FREQUENCY NET "pcie/u1_pcs_pipe/ff_rx_fclk_0" 250.000000 MHz (0 errors)
            1 item scored, 0 timing errors detected.

• BLOCK PATH FROM PORT "rstn" (0 errors)
            119 items scored, 0 timing errors detected.

• BLOCK PATH TO PORT "OUT*" (0 errors)
            0 items scored, 0 timing errors detected.

• BLOCK PATH FROM PORT "INP*" (0 errors)
            16 items scored, 0 timing errors detected.

• BLOCK PATH FROM PORT "SRAM_A*" (0 errors)
            0 items scored, 0 timing errors detected.

• BLOCK PATH TO PORT "LED*" (0 errors)
            8 items scored, 0 timing errors detected.

• BLOCK PATH FROM CELL "*ctc_reset_chx*" (0 errors)
            14 items scored, 0 timing errors detected.

• MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*cnt_done_nfts_rx*" 2.000000 X (0 errors)
            214 items scored, 0 timing errors detected.

• MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*ltssm_nfts_rx_skp*" 2.000000 X (0 errors)
            244 items scored, 0 timing errors detected.

• MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr*" 6.000000 ns (0 errors)
            33 items scored, 0 timing errors detected.

• MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr*" 6.000000 ns (0 errors)
            147 items scored, 0 timing errors detected.

• MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr*" 6.000000 ns (0 errors)
            14 items scored, 0 timing errors detected.

• MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr*" 6.000000 ns (0 errors)
            18 items scored, 0 timing errors detected.

• MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data*" 6.000000 ns (0 errors)
            16 items scored, 0 timing errors detected.

• MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl*" 6.000000 ns (0 errors)
            2 items scored, 0 timing errors detected.

34 potential circuit loops found in timing analysis.
BLOCK ASYNCPATHS
BLOCK RESETPATHS
BLOCK JTAG PATHS
--------------------------------------------------------------------------------



================================================================================
Preference: FREQUENCY NET "clk_125_c" 125.000000 MHz ;
            4096 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.106ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[215]  (from clk_125_c +)
   Destination:    PDPW16KC   Port           top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_5_2(ASIC)  (to clk_125_c +)

   Delay:               0.272ns  (34.2% logic, 65.8% route), 1 logic levels.

 Constraint Details:

      0.272ns physical path delay top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4664 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_5_2 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.106ns

 Physical Path Details:

      Data path top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4664 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_5_2:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R51C32B.CLK to     R51C32B.Q0 top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4664 (from clk_125_c)
ROUTE         1     0.179     R51C32B.Q0 to *R_R53C32.DI35 top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[215] (to clk_125_c)
                  --------
                    0.272   (34.2% logic, 65.8% route), 1 logic levels.
```

```
 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4664:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R51C32B.CLK clk_125_c
                    -------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_5_2:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to *R_R53C32.CLKW clk_125_c
                    -------
                      0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.106ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[125]  (from clk_125_c +)
   Destination:    PDPW16KC   Port           top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_3_4(ASIC)  (to clk_125_c +)

   Delay:               0.272ns  (34.2% logic, 65.8% route), 1 logic levels.

 Constraint Details:

      0.272ns physical path delay top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4622 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_3_4 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.106ns

 Physical Path Details:

      Data path top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4622 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_3_4:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R34C41A.CLK to     R34C41A.Q0 top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4622 (from clk_125_c)
ROUTE         1     0.179     R34C41A.Q0 to *R_R35C41.DI17 top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[125] (to clk_125_c)
                    -------
                      0.272   (34.2% logic, 65.8% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4622:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R34C41A.CLK clk_125_c
                    -------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_3_4:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to *R_R35C41.CLKW clk_125_c
                    -------
                      0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.106ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[160]  (from clk_125_c +)
   Destination:    PDPW16KC   Port           top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_4_3(ASIC)  (to clk_125_c +)

   Delay:               0.272ns  (34.2% logic, 65.8% route), 1 logic levels.

 Constraint Details:

      0.272ns physical path delay top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4640 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_4_3 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.106ns

 Physical Path Details:

      Data path top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4640 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_4_3:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R34C32B.CLK to     R34C32B.Q0 top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4640 (from clk_125_c)
ROUTE         1     0.179     R34C32B.Q0 to *R_R35C32.DI16 top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[160] (to clk_125_c)
                    -------
                      0.272   (34.2% logic, 65.8% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4640:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R34C32B.CLK clk_125_c
                    -------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_4_3:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to *R_R35C32.CLKW clk_125_c
                    -------
                      0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.106ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[249]  (from clk_125_c +)
   Destination:    PDPW16KC   Port           top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_6_1(ASIC)  (to clk_125_c +)

   Delay:               0.272ns  (34.2% logic, 65.8% route), 1 logic levels.

 Constraint Details:

      0.272ns physical path delay top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4681 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_6_1 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.106ns

 Physical Path Details:

      Data path top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4681 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_6_1:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R52C35B.CLK to     R52C35B.Q0 top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4681 (from clk_125_c)
ROUTE         1     0.179     R52C35B.Q0 to *R_R53C35.DI33 top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[249] (to clk_125_c)
                    -------
                      0.272   (34.2% logic, 65.8% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4681:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R52C35B.CLK clk_125_c
                    -------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_6_1:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to *R_R53C35.CLKW clk_125_c
                    -------
                      0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.108ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/tlp_size[7]  (from clk_125_c +)
   Destination:    PDPW16KC   Port           pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/u1_atbl_mem/pmi_ram_dpEbnonessen208146208146_0_0_0(ASIC)  (to clk_125_c +)

   Delay:               0.274ns  (33.9% logic, 66.1% route), 1 logic levels.

 Constraint Details:

      0.274ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/SLICE_806 to pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/u1_atbl_mem/pmi_ram_dpEbnonessen208146208146_0_0_0 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.108ns

 Physical Path Details:
```

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/SLICE_806 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/u1_atbl_mem/pmi_ram_dpEbnonessen208146208146_0_0_0:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R18C53B.CLK to	R18C53B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/SLICE_806 (from clk_125_c)
ROUTE	3	0.181	R18C53B.Q0 to *R_R17C53.DI17	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/tlp_size[7] (to clk_125_c)
		0.274	(33.9% logic, 66.1% route), 1 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/SLICE_806:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527	*FF_TX_H_CLK_0 to	R18C53B.CLK clk_125_c
		0.527	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/u1_atbl_mem/pmi_ram_dpEbnonessen208146208146_0_0_0:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.586	*FF_TX_H_CLK_0 to	*R_R17C53.CLKW clk_125_c
		0.586	(0.0% logic, 100.0% route), 0 logic levels.	

Passed: The following path meets requirements by 0.114ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_trnc/u1_cfg_top/u1_cfg_resp/wr_ptr[5] (from clk_125_c +)
Destination: DP16KC Port pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_trnc/u1_cfg_top/u1_cfg_resp/u1_resp_mem/pmi_ram_dpEbnonessen168256168256_0_0_0(ASIC) (to clk_125_c +)

Delay: 0.223ns (41.7% logic, 58.3% route), 1 logic levels.

Constraint Details:

0.223ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_trnc/u1_cfg_top/u1_cfg_resp/SLICE_448 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_trnc/u1_cfg_top/u1_cfg_resp/u1_resp_mem/pmi_ram_dpEbnonessen168256168256_0_0_0 meets
0.050ns ADDR_HLD and
0.000ns delay constraint less
-0.059ns skew requirement (totaling 0.109ns) by 0.114ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_trnc/u1_cfg_top/u1_cfg_resp/SLICE_448 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_trnc/u1_cfg_top/u1_cfg_resp/u1_resp_mem/pmi_ram_dpEbnonessen168256168256_0_0_0:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R18C35A.CLK to	R18C35A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_trnc/u1_cfg_top/u1_cfg_resp/SLICE_448 (from clk_125_c)
ROUTE	2	0.130	R18C35A.Q0 to *R_R17C35.ADA9	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_trnc/u1_cfg_top/u1_cfg_resp/wr_ptr[5] (to clk_125_c)
		0.223	(41.7% logic, 58.3% route), 1 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_trnc/u1_cfg_top/u1_cfg_resp/SLICE_448:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527	*FF_TX_H_CLK_0 to	R18C35A.CLK clk_125_c
		0.527	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_trnc/u1_cfg_top/u1_cfg_resp/u1_resp_mem/pmi_ram_dpEbnonessen168256168256_0_0_0:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.586	*FF_TX_H_CLK_0 to	*R_R17C35.CLKA clk_125_c
		0.586	(0.0% logic, 100.0% route), 0 logic levels.	

Passed: The following path meets requirements by 0.115ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[53] (from clk_125_c +)
Destination: PDPW16KC Port top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_1_6(ASIC) (to clk_125_c +)

Delay: 0.281ns (33.1% logic, 66.9% route), 1 logic levels.

Constraint Details:

0.281ns physical path delay top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4586 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_1_6 meets
0.107ns DATA_HLD and
0.000ns delay constraint less
-0.059ns skew requirement (totaling 0.166ns) by 0.115ns

Physical Path Details:

Data path top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4586 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_1_6:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R34C49B.CLK to	R34C49B.Q1 top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4586 (from clk_125_c)
ROUTE	1	0.188	R34C49B.Q1 to *R_R35C50.DI17	top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[53] (to clk_125_c)
		0.281	(33.1% logic, 66.9% route), 1 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4586:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527	*FF_TX_H_CLK_0 to	R34C49B.CLK clk_125_c
		0.527	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr27095122709512_0_1_6:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.586	*FF_TX_H_CLK_0 to	*R_R35C50.CLKW clk_125_c
		0.586	(0.0% logic, 100.0% route), 0 logic levels.	

Passed: The following path meets requirements by 0.115ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_cins/txtp_tdata[11] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtdp/u1_td_mux/tdata7_CR15_ram_1/RAM1 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtdp/u1_td_mux/tdata7_CR15_ram_1/WCK_INT +)
FF pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtdp/u1_td_mux/tdata7_CR15_ram_1/RAM1

Delay: 0.177ns (52.5% logic, 47.5% route), 2 logic levels.

Constraint Details:

0.177ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_cins/SLICE_2125 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtdp/u1_td_mux/tdata7_CR15_ram_1/SLICE_1347 meets
0.062ns WD_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling 0.062ns) by 0.115ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_cins/SLICE_2125 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtdp/u1_td_mux/tdata7_CR15_ram_1/SLICE_1347:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R6C39C.CLK to	R6C39C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_cins/SLICE_2125 (from clk_125_c)
ROUTE	1	0.084	R6C39C.Q1 to	R7C39C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/txtp_tdata[11]
ZERO_DEL	---	0.000	R7C39C.D1 to	R7C39C.WDO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtdp/u1_td_mux/tdata7_CR15_ram_1/SLICE_1345
ROUTE	1	0.000	R7C39C.WDO3 to	R7C39B.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtdp/u1_td_mux/tdata7_CR15_ram_1/WD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtdp/u1_td_mux/tdata7_CR15_ram_1/WCK_INT)
		0.177	(52.5% logic, 47.5% route), 2 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_cins/SLICE_2125:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527	*FF_TX_H_CLK_0 to	R6C39C.CLK clk_125_c
		0.527	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtdp/u1_td_mux/tdata7_CR15_ram_1/SLICE_1347:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527	*FF_TX_H_CLK_0 to	R7C39C.CLK clk_125_c
ZERO_DEL	---	0.000	R7C39C.CLK to	R7C39C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtdp/u1_td_mux/tdata7_CR15_ram_1/SLICE_1345
ROUTE	2	0.000	R7C39C.WCKO to	R7C39B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtdp/u1_td_mux/tdata7_CR15_ram_1/WCK_INT
		0.527	(0.0% logic, 100.0% route), 1 logic levels.	

Passed: The following path meets requirements by 0.120ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q wb_tlc/dec/fifo_dout[12] (from clk_125_c +)

```
   Destination:    DP16KC     Port           wb_tlc/req_fifo/I_async_pkt_fifo/I_pmi_ram_dp/pmi_ram_dpebnonessdr2711204827112048_0_1_1(ASIC)  (to clk_125_c +)

   Delay:              0.286ns  (32.5% logic, 67.5% route), 1 logic levels.

 Constraint Details:

      0.286ns physical path delay wb_tlc/dec/SLICE_6202 to wb_tlc/req_fifo/I_async_pkt_fifo/I_pmi_ram_dp/pmi_ram_dpebnonessdr2711204827112048_0_1_1 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.120ns

 Physical Path Details:

      Data path wb_tlc/dec/SLICE_6202 to wb_tlc/req_fifo/I_async_pkt_fifo/I_pmi_ram_dp/pmi_ram_dpebnonessdr2711204827112048_0_1_1:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R18C32B.CLK to     R18C32B.Q0 wb_tlc/dec/SLICE_6202 (from clk_125_c)
ROUTE         1     0.193     R18C32B.Q0 to *R_R17C32.DIA3 wb_tlc/to_req_fifo_dout[12] (to clk_125_c)
                  --------
                    0.286   (32.5% logic, 67.5% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/dec/SLICE_6202:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R18C32B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/req_fifo/I_async_pkt_fifo/I_pmi_ram_dp/pmi_ram_dpebnonessdr2711204827112048_0_1_1:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to *R_R17C32.CLKA clk_125_c
                  --------
                    0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.120ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/tlp_data_reg[5]  (from clk_125_c +)
   Destination:    DP16KC     Port           pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/u1_tlp_mem/pmi_ram_dpEbnonessen1610102416101024_0_0_0(ASIC)  (to clk_125_c +)

   Delay:              0.286ns  (32.5% logic, 67.5% route), 1 logic levels.

 Constraint Details:

      0.286ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/SLICE_2690 to pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/u1_tlp_mem/pmi_ram_dpEbnonessen1610102416101024_0_0_0 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.120ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/SLICE_2690 to pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/u1_tlp_mem/pmi_ram_dpEbnonessen1610102416101024_0_0_0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R18C47B.CLK to     R18C47B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/SLICE_2690 (from clk_125_c)
ROUTE         1     0.193     R18C47B.Q1 to *R_R17C47.DIA5 pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/tlp_data_reg[5] (to clk_125_c)
                  --------
                    0.286   (32.5% logic, 67.5% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/SLICE_2690:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R18C47B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/u1_tlp_mem/pmi_ram_dpEbnonessen1610102416101024_0_0_0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to *R_R17C47.CLKA clk_125_c
                  --------
                    0.586   (0.0% logic, 100.0% route), 0 logic levels.


================================================================================
Preference: FREQUENCY NET "can_clk_c" 25.000000 MHz ;
            4096 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.069ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              can/i_can_bsp/i_can_fifo/wr_info_pointer[3]  (from can_clk_c +)
   Destination:    FF         Data in        can/i_can_bsp/i_can_fifo/overrun_info_ram_0/RAM0  (to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/WCK_INT +)

   Delay:              0.173ns  (53.8% logic, 46.2% route), 2 logic levels.

 Constraint Details:

      0.173ns physical path delay can/i_can_bsp/i_can_fifo/SLICE_1581 to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1168 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.069ns

 Physical Path Details:

      Data path can/i_can_bsp/i_can_fifo/SLICE_1581 to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1168:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R40C9A.CLK to      R40C9A.Q1 can/i_can_bsp/i_can_fifo/SLICE_1581 (from can_clk_c)
ROUTE        10     0.080      R40C9A.Q1 to      R39C9C.D0 can/i_can_bsp/i_can_fifo/wr_info_pointer[3]
ZERO_DEL    ---     0.000      R39C9C.D0 to   R39C9C.WADO3 can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1167
ROUTE         1     0.000   R39C9C.WADO3 to    R39C9A.WAD3 can/i_can_bsp/i_can_fifo/overrun_info_ram_0/WAD3_INT (to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/WCK_INT)
                  --------
                    0.173   (53.8% logic, 46.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/SLICE_1581:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to     R40C9A.CLK can_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1168:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to     R39C9C.CLK can_clk_c
ZERO_DEL    ---     0.000     R39C9C.CLK to    R39C9C.WCKO can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1167
ROUTE         2     0.000    R39C9C.WCKO to     R39C9A.WCK can/i_can_bsp/i_can_fifo/overrun_info_ram_0/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.097ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              can/i_can_bsp/byte_cnt[2]  (from can_clk_c +)
   Destination:    FF         Data in        can/i_can_bsp/tmp_fifo_ram_0/RAM0  (to can/i_can_bsp/tmp_fifo_ram_0/WCK_INT +)
                   FF                        can/i_can_bsp/tmp_fifo_ram_0/RAM0

   Delay:              0.201ns  (46.3% logic, 53.7% route), 2 logic levels.

 Constraint Details:

      0.201ns physical path delay can/i_can_bsp/SLICE_1527 to can/i_can_bsp/tmp_fifo_ram_0/SLICE_1172 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.097ns

 Physical Path Details:

      Data path can/i_can_bsp/SLICE_1527 to can/i_can_bsp/tmp_fifo_ram_0/SLICE_1172:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R52C18A.CLK to     R52C18A.Q0 can/i_can_bsp/SLICE_1527 (from can_clk_c)
ROUTE         5     0.108     R52C18A.Q0 to     R52C17C.C0 can/i_can_bsp/byte_cnt[2]
ZERO_DEL    ---     0.000     R52C17C.C0 to  R52C17C.WADO2 can/i_can_bsp/tmp_fifo_ram_0/SLICE_1171
ROUTE         2     0.000  R52C17C.WADO2 to   R52C17A.WAD2 can/i_can_bsp/tmp_fifo_ram_0/WAD2_INT (to can/i_can_bsp/tmp_fifo_ram_0/WCK_INT)
                  --------
                    0.201   (46.3% logic, 53.7% route), 2 logic levels.

 Clock Skew Details:
```

```
     Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/SLICE_1527:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to    R52C18A.CLK can_clk_c
                    --------
                     0.488   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/tmp_fifo_ram_0/SLICE_1172:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to    R52C17C.CLK can_clk_c
ZERO_DEL    ---     0.000    R52C17C.CLK to   R52C17C.WCKO can/i_can_bsp/tmp_fifo_ram_0/SLICE_1171
ROUTE         2     0.000   R52C17C.WCKO to    R52C17A.WCK can/i_can_bsp/tmp_fifo_ram_0/WCK_INT
                    --------
                     0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.097ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:          FF         Q             can/i_can_bsp/byte_cnt[2]  (from can_clk_c +)
   Destination:     FF         Data in       can/i_can_bsp/tmp_fifo_ram_0/RAM1  (to can/i_can_bsp/tmp_fifo_ram_0/WCK_INT +)
                    FF                       can/i_can_bsp/tmp_fifo_ram_0/RAM1

   Delay:               0.201ns  (46.3% logic, 53.7% route), 2 logic levels.

 Constraint Details:

     0.201ns physical path delay can/i_can_bsp/SLICE_1527 to can/i_can_bsp/tmp_fifo_ram_0/SLICE_1173 meets
     0.104ns WAD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.104ns) by 0.097ns

 Physical Path Details:

     Data path can/i_can_bsp/SLICE_1527 to can/i_can_bsp/tmp_fifo_ram_0/SLICE_1173:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R52C18A.CLK to     R52C18A.Q0 can/i_can_bsp/SLICE_1527 (from can_clk_c)
ROUTE         5     0.108     R52C18A.Q0 to     R52C17C.C0 can/i_can_bsp/byte_cnt[2]
ZERO_DEL    ---     0.000     R52C17C.C0 to  R52C17C.WADO2 can/i_can_bsp/tmp_fifo_ram_0/SLICE_1171
ROUTE         2     0.000  R52C17C.WADO2 to   R52C17B.WAD2 can/i_can_bsp/tmp_fifo_ram_0/WAD2_INT (to can/i_can_bsp/tmp_fifo_ram_0/WCK_INT)
                    --------
                     0.201   (46.3% logic, 53.7% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/SLICE_1527:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to    R52C18A.CLK can_clk_c
                    --------
                     0.488   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/tmp_fifo_ram_0/SLICE_1173:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to    R52C17C.CLK can_clk_c
ZERO_DEL    ---     0.000    R52C17C.CLK to   R52C17C.WCKO can/i_can_bsp/tmp_fifo_ram_0/SLICE_1171
ROUTE         2     0.000   R52C17C.WCKO to    R52C17B.WCK can/i_can_bsp/tmp_fifo_ram_0/WCK_INT
                    --------
                     0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.127ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:          FF         Q             can/i_can_bsp/i_can_fifo/wr_info_pointer[2]  (from can_clk_c +)
   Destination:     FF         Data in       can/i_can_bsp/i_can_fifo/overrun_info_ram_0/RAM0  (to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/WCK_INT +)

   Delay:               0.231ns  (40.3% logic, 59.7% route), 2 logic levels.

 Constraint Details:

     0.231ns physical path delay can/i_can_bsp/i_can_fifo/SLICE_1581 to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1168 meets
     0.104ns WAD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.104ns) by 0.127ns

 Physical Path Details:

     Data path can/i_can_bsp/i_can_fifo/SLICE_1581 to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1168:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R40C9A.CLK to      R40C9A.Q0 can/i_can_bsp/i_can_fifo/SLICE_1581 (from can_clk_c)
ROUTE        10     0.138      R40C9A.Q0 to      R39C9C.C0 can/i_can_bsp/i_can_fifo/wr_info_pointer[2]
ZERO_DEL    ---     0.000      R39C9C.C0 to   R39C9C.WADO2 can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1167
ROUTE         1     0.000   R39C9C.WADO2 to    R39C9A.WAD2 can/i_can_bsp/i_can_fifo/overrun_info_ram_0/WAD2_INT (to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/WCK_INT)
                    --------
                     0.231   (40.3% logic, 59.7% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/SLICE_1581:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to     R40C9A.CLK can_clk_c
                    --------
                     0.488   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1168:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to     R39C9C.CLK can_clk_c
ZERO_DEL    ---     0.000     R39C9C.CLK to    R39C9C.WCKO can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1167
ROUTE         2     0.000    R39C9C.WCKO to     R39C9A.WCK can/i_can_bsp/i_can_fifo/overrun_info_ram_0/WCK_INT
                    --------
                     0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.135ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:          FF         Q             can/i_can_bsp/i_can_fifo/wr_pointer[3]  (from can_clk_c +)
   Destination:     FF         Data in       can/i_can_bsp/i_can_fifo/fifo_ram_2/RAM0  (to can/i_can_bsp/i_can_fifo/fifo_ram_2/WCK_INT +)
                    FF                       can/i_can_bsp/i_can_fifo/fifo_ram_2/RAM0

   Delay:               0.239ns  (38.9% logic, 61.1% route), 2 logic levels.

 Constraint Details:

     0.239ns physical path delay can/i_can_bsp/i_can_fifo/SLICE_7 to can/i_can_bsp/i_can_fifo/fifo_ram_2/SLICE_1140 meets
     0.104ns WAD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.104ns) by 0.135ns

 Physical Path Details:

     Data path can/i_can_bsp/i_can_fifo/SLICE_7 to can/i_can_bsp/i_can_fifo/fifo_ram_2/SLICE_1140:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R46C26C.CLK to     R46C26C.Q0 can/i_can_bsp/i_can_fifo/SLICE_7 (from can_clk_c)
ROUTE         9     0.146     R46C26C.Q0 to     R48C26C.D0 can/i_can_bsp/i_can_fifo/wr_pointer[3]
ZERO_DEL    ---     0.000     R48C26C.D0 to  R48C26C.WADO3 can/i_can_bsp/i_can_fifo/fifo_ram_2/SLICE_1139
ROUTE         2     0.000  R48C26C.WADO3 to   R48C26A.WAD3 can/i_can_bsp/i_can_fifo/fifo_ram_2/WAD3_INT (to can/i_can_bsp/i_can_fifo/fifo_ram_2/WCK_INT)
                    --------
                     0.239   (38.9% logic, 61.1% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/SLICE_7:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to    R46C26C.CLK can_clk_c
                    --------
                     0.488   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/fifo_ram_2/SLICE_1140:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to    R48C26C.CLK can_clk_c
ZERO_DEL    ---     0.000    R48C26C.CLK to   R48C26C.WCKO can/i_can_bsp/i_can_fifo/fifo_ram_2/SLICE_1139
ROUTE         2     0.000   R48C26C.WCKO to    R48C26A.WCK can/i_can_bsp/i_can_fifo/fifo_ram_2/WCK_INT
                    --------
                     0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.135ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)
```

```
   Source:         FF         Q             can/i_can_bsp/i_can_fifo/wr_pointer[3]  (from can_clk_c +)
   Destination:    FF         Data in       can/i_can_bsp/i_can_fifo/fifo_ram_2/RAM1  (to can/i_can_bsp/i_can_fifo/fifo_ram_2/WCK_INT +)
                   FF                       can/i_can_bsp/i_can_fifo/fifo_ram_2/RAM1

   Delay:               0.239ns  (38.9% logic, 61.1% route), 2 logic levels.

 Constraint Details:

      0.239ns physical path delay can/i_can_bsp/i_can_fifo/SLICE_7 to can/i_can_bsp/i_can_fifo/fifo_ram_2/SLICE_1141 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.135ns

 Physical Path Details:

      Data path can/i_can_bsp/i_can_fifo/SLICE_7 to can/i_can_bsp/i_can_fifo/fifo_ram_2/SLICE_1141:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R46C26C.CLK to     R46C26C.Q0 can/i_can_bsp/i_can_fifo/SLICE_7 (from can_clk_c)
ROUTE         9     0.146     R46C26C.Q0 to     R48C26C.D0 can/i_can_bsp/i_can_fifo/wr_pointer[3]
ZERO_DEL    ---     0.000     R48C26C.D0 to  R48C26C.WADO3 can/i_can_bsp/i_can_fifo/fifo_ram_2/SLICE_1139
ROUTE         2     0.000  R48C26C.WADO3 to   R48C26B.WAD3 can/i_can_bsp/i_can_fifo/fifo_ram_2/WAD3_INT (to can/i_can_bsp/i_can_fifo/fifo_ram_2/WCK_INT)
                   --------
                     0.239   (38.9% logic, 61.1% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/SLICE_7:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to    R46C26C.CLK can_clk_c
                   --------
                     0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/fifo_ram_2/SLICE_1141:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to    R48C26C.CLK can_clk_c
ZERO_DEL    ---     0.000    R48C26C.CLK to   R48C26C.WCKO can/i_can_bsp/i_can_fifo/fifo_ram_2/SLICE_1139
ROUTE         2     0.000   R48C26C.WCKO to    R48C26B.WCK can/i_can_bsp/i_can_fifo/fifo_ram_2/WCK_INT
                   --------
                     0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.142ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             can/i_can_bsp/i_can_fifo/wr_info_pointer[1]  (from can_clk_c +)
   Destination:    FF         Data in       can/i_can_bsp/i_can_fifo/overrun_info_ram_0/RAM0  (to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/WCK_INT +)

   Delay:               0.246ns  (37.8% logic, 62.2% route), 2 logic levels.

 Constraint Details:

      0.246ns physical path delay can/i_can_bsp/i_can_fifo/SLICE_1580 to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1168 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.142ns

 Physical Path Details:

      Data path can/i_can_bsp/i_can_fifo/SLICE_1580 to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1168:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R40C9C.CLK to     R40C9C.Q1 can/i_can_bsp/i_can_fifo/SLICE_1580 (from can_clk_c)
ROUTE        10     0.153      R40C9C.Q1 to     R39C9C.B0 can/i_can_bsp/i_can_fifo/wr_info_pointer[1]
ZERO_DEL    ---     0.000     R39C9C.B0 to   R39C9C.WADO1 can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1167
ROUTE         1     0.000   R39C9C.WADO1 to    R39C9A.WAD1 can/i_can_bsp/i_can_fifo/overrun_info_ram_0/WAD1_INT (to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/WCK_INT)
                   --------
                     0.246   (37.8% logic, 62.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/SLICE_1580:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to     R40C9C.CLK can_clk_c
                   --------
                     0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1168:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to     R39C9C.CLK can_clk_c
ZERO_DEL    ---     0.000     R39C9C.CLK to    R39C9C.WCKO can/i_can_bsp/i_can_fifo/overrun_info_ram_0/SLICE_1167
ROUTE         2     0.000    R39C9C.WCKO to     R39C9A.WCK can/i_can_bsp/i_can_fifo/overrun_info_ram_0/WCK_INT
                   --------
                     0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.144ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             can/i_can_bsp/byte_cnt[0]  (from can_clk_c +)
   Destination:    FF         Data in       can/i_can_bsp/tmp_fifo_ram_0/RAM1  (to can/i_can_bsp/tmp_fifo_ram_0/WCK_INT +)
                   FF                       can/i_can_bsp/tmp_fifo_ram_0/RAM1

   Delay:               0.248ns  (37.5% logic, 62.5% route), 2 logic levels.

 Constraint Details:

      0.248ns physical path delay can/i_can_bsp/SLICE_1526 to can/i_can_bsp/tmp_fifo_ram_0/SLICE_1173 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.144ns

 Physical Path Details:

      Data path can/i_can_bsp/SLICE_1526 to can/i_can_bsp/tmp_fifo_ram_0/SLICE_1173:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R52C18B.CLK to     R52C18B.Q0 can/i_can_bsp/SLICE_1526 (from can_clk_c)
ROUTE         7     0.155     R52C18B.Q0 to     R52C17C.A0 can/i_can_bsp/byte_cnt[0]
ZERO_DEL    ---     0.000     R52C17C.A0 to  R52C17C.WADO0 can/i_can_bsp/tmp_fifo_ram_0/SLICE_1171
ROUTE         2     0.000  R52C17C.WADO0 to   R52C17B.WAD0 can/i_can_bsp/tmp_fifo_ram_0/WAD0_INT (to can/i_can_bsp/tmp_fifo_ram_0/WCK_INT)
                   --------
                     0.248   (37.5% logic, 62.5% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/SLICE_1526:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to    R52C18B.CLK can_clk_c
                   --------
                     0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/tmp_fifo_ram_0/SLICE_1173:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to    R52C17C.CLK can_clk_c
ZERO_DEL    ---     0.000    R52C17C.CLK to   R52C17C.WCKO can/i_can_bsp/tmp_fifo_ram_0/SLICE_1171
ROUTE         2     0.000   R52C17C.WCKO to    R52C17B.WCK can/i_can_bsp/tmp_fifo_ram_0/WCK_INT
                   --------
                     0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.144ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             can/i_can_bsp/byte_cnt[0]  (from can_clk_c +)
   Destination:    FF         Data in       can/i_can_bsp/tmp_fifo_ram_0/RAM0  (to can/i_can_bsp/tmp_fifo_ram_0/WCK_INT +)
                   FF                       can/i_can_bsp/tmp_fifo_ram_0/RAM0

   Delay:               0.248ns  (37.5% logic, 62.5% route), 2 logic levels.

 Constraint Details:

      0.248ns physical path delay can/i_can_bsp/SLICE_1526 to can/i_can_bsp/tmp_fifo_ram_0/SLICE_1172 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.144ns

 Physical Path Details:

      Data path can/i_can_bsp/SLICE_1526 to can/i_can_bsp/tmp_fifo_ram_0/SLICE_1172:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R52C18B.CLK to     R52C18B.Q0 can/i_can_bsp/SLICE_1526 (from can_clk_c)
ROUTE         7     0.155     R52C18B.Q0 to     R52C17C.A0 can/i_can_bsp/byte_cnt[0]
```

```
ZERO_DEL    ---     0.000     R52C17C.A0 to  R52C17C.WADO0 can/i_can_bsp/tmp_fifo_ram_0/SLICE_1171
ROUTE         2     0.000  R52C17C.WADO0 to   R52C17A.WAD0 can/i_can_bsp/tmp_fifo_ram_0/WAD0_INT (to can/i_can_bsp/tmp_fifo_ram_0/WCK_INT)
                  --------
                    0.248   (37.5% logic, 62.5% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/SLICE_1526:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to    R52C18B.CLK can_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/tmp_fifo_ram_0/SLICE_1172:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to    R52C17C.CLK can_clk_c
ZERO_DEL    ---     0.000    R52C17C.CLK to   R52C17C.WCKO can/i_can_bsp/tmp_fifo_ram_0/SLICE_1171
ROUTE         2     0.000   R52C17C.WCKO to    R52C17A.WCK can/i_can_bsp/tmp_fifo_ram_0/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.162ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              can/i_can_bsp/byte_cnt[2]  (from can_clk_c +)
   Destination:    FF         Data in        can/i_can_bsp/tmp_fifo_ram/RAM0  (to can/i_can_bsp/tmp_fifo_ram/WCK_INT +)
                   FF                        can/i_can_bsp/tmp_fifo_ram/RAM0

   Delay:               0.266ns  (35.0% logic, 65.0% route), 2 logic levels.

 Constraint Details:

      0.266ns physical path delay can/i_can_bsp/SLICE_1527 to can/i_can_bsp/tmp_fifo_ram/SLICE_1125 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.162ns

 Physical Path Details:

      Data path can/i_can_bsp/SLICE_1527 to can/i_can_bsp/tmp_fifo_ram/SLICE_1125:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R52C18A.CLK to     R52C18A.Q0 can/i_can_bsp/SLICE_1527 (from can_clk_c)
ROUTE         5     0.173     R52C18A.Q0 to     R52C16C.C0 can/i_can_bsp/byte_cnt[2]
ZERO_DEL    ---     0.000     R52C16C.C0 to  R52C16C.WADO2 can/i_can_bsp/tmp_fifo_ram/SLICE_1124
ROUTE         2     0.000  R52C16C.WADO2 to   R52C16A.WAD2 can/i_can_bsp/tmp_fifo_ram/WAD2_INT (to can/i_can_bsp/tmp_fifo_ram/WCK_INT)
                  --------
                    0.266   (35.0% logic, 65.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/SLICE_1527:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to    R52C18A.CLK can_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/tmp_fifo_ram/SLICE_1125:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       404     0.488 *_R53C70.CLKOP to    R52C16C.CLK can_clk_c
ZERO_DEL    ---     0.000    R52C16C.CLK to   R52C16C.WCKO can/i_can_bsp/tmp_fifo_ram/SLICE_1124
ROUTE         2     0.000   R52C16C.WCKO to    R52C16A.WCK can/i_can_bsp/tmp_fifo_ram/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


================================================================================
Preference: FREQUENCY NET "uart_clk_c" 25.000000 MHz ;
            4096 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.104ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              uart6/regs/transmitter/fifo_tx/top[2]  (from uart_clk_c +)
   Destination:    FF         Data in        uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/RAM1  (to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT +)
                   FF                        uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/RAM1

   Delay:               0.208ns  (44.7% logic, 55.3% route), 2 logic levels.

 Constraint Details:

      0.208ns physical path delay uart6/regs/transmitter/fifo_tx/SLICE_6033 to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1185 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.104ns

 Physical Path Details:

      Data path uart6/regs/transmitter/fifo_tx/SLICE_6033 to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1185:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R62C12C.CLK to     R62C12C.Q0 uart6/regs/transmitter/fifo_tx/SLICE_6033 (from uart_clk_c)
ROUTE         4     0.115     R62C12C.Q0 to     R61C12C.C0 uart6/regs/transmitter/fifo_tx/top[2]
ZERO_DEL    ---     0.000     R61C12C.C0 to  R61C12C.WADO2 uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1183
ROUTE         2     0.000  R61C12C.WADO2 to   R61C12B.WAD2 uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/WAD2_INT (to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT)
                  --------
                    0.208   (44.7% logic, 55.3% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_uarts/PLLInst_0 to uart6/regs/transmitter/fifo_tx/SLICE_6033:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R62C12C.CLK uart_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_uarts/PLLInst_0 to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1185:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R61C12C.CLK uart_clk_c
ZERO_DEL    ---     0.000    R61C12C.CLK to   R61C12C.WCKO uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1183
ROUTE         2     0.000   R61C12C.WCKO to    R61C12B.WCK uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.104ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              uart6/regs/transmitter/fifo_tx/top[2]  (from uart_clk_c +)
   Destination:    FF         Data in        uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/RAM0  (to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT +)
                   FF                        uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/RAM0

   Delay:               0.208ns  (44.7% logic, 55.3% route), 2 logic levels.

 Constraint Details:

      0.208ns physical path delay uart6/regs/transmitter/fifo_tx/SLICE_6033 to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1184 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.104ns

 Physical Path Details:

      Data path uart6/regs/transmitter/fifo_tx/SLICE_6033 to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1184:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R62C12C.CLK to     R62C12C.Q0 uart6/regs/transmitter/fifo_tx/SLICE_6033 (from uart_clk_c)
ROUTE         4     0.115     R62C12C.Q0 to     R61C12C.C0 uart6/regs/transmitter/fifo_tx/top[2]
ZERO_DEL    ---     0.000     R61C12C.C0 to  R61C12C.WADO2 uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1183
ROUTE         2     0.000  R61C12C.WADO2 to   R61C12A.WAD2 uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/WAD2_INT (to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT)
                  --------
                    0.208   (44.7% logic, 55.3% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_uarts/PLLInst_0 to uart6/regs/transmitter/fifo_tx/SLICE_6033:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R62C12C.CLK uart_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.
```

Destination Clock Path pll_uarts/PLLInst_0 to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1184:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.488	*L_R53C5.CLKOP to	R61C12C.CLK uart_clk_c
ZERO_DEL	---	0.000	R61C12C.CLK to	R61C12C.WCKO uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1183
ROUTE	2	0.000	R61C12C.WCKO to	R61C12A.WCK uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT
		0.488	(0.0% logic, 100.0% route), 1 logic levels.	

Passed: The following path meets requirements by 0.128ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source:	FF	Q	uart2/regs/transmitter/fifo_tx/top[2] (from uart_clk_c +)
Destination:	FF	Data in	uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/RAM1 (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT +)
	FF		uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/RAM1

Delay: 0.232ns (40.1% logic, 59.9% route), 2 logic levels.

Constraint Details:

0.232ns physical path delay uart2/regs/transmitter/fifo_tx/SLICE_5313 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1233 meets
0.104ns WAD_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling 0.104ns) by 0.128ns

Physical Path Details:

Data path uart2/regs/transmitter/fifo_tx/SLICE_5313 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1233:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R30C14C.CLK to	R30C14C.Q0 uart2/regs/transmitter/fifo_tx/SLICE_5313 (from uart_clk_c)
ROUTE	4	0.139	R30C14C.Q0 to	R30C13C.C0 uart2/regs/transmitter/fifo_tx/top[2]
ZERO_DEL	---	0.000	R30C13C.C0 to	R30C13C.WADO2 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1231
ROUTE	2	0.000	R30C13C.WADO2 to	R30C13B.WAD2 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/WAD2_INT (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT)
		0.232	(40.1% logic, 59.9% route), 2 logic levels.	

Clock Skew Details:

Source Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/SLICE_5313:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.488	*L_R53C5.CLKOP to	R30C14C.CLK uart_clk_c
		0.488	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1233:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.488	*L_R53C5.CLKOP to	R30C13C.CLK uart_clk_c
ZERO_DEL	---	0.000	R30C13C.CLK to	R30C13C.WCKO uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1231
ROUTE	2	0.000	R30C13C.WCKO to	R30C13B.WCK uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT
		0.488	(0.0% logic, 100.0% route), 1 logic levels.	

Passed: The following path meets requirements by 0.128ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source:	FF	Q	uart2/regs/transmitter/fifo_tx/top[2] (from uart_clk_c +)
Destination:	FF	Data in	uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM1 (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT +)
	FF		uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM1

Delay: 0.232ns (40.1% logic, 59.9% route), 2 logic levels.

Constraint Details:

0.232ns physical path delay uart2/regs/transmitter/fifo_tx/SLICE_5313 to uart2/regs/transmitter/SLICE_1230 meets
0.104ns WAD_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling 0.104ns) by 0.128ns

Physical Path Details:

Data path uart2/regs/transmitter/fifo_tx/SLICE_5313 to uart2/regs/transmitter/SLICE_1230:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R30C14C.CLK to	R30C14C.Q0 uart2/regs/transmitter/fifo_tx/SLICE_5313 (from uart_clk_c)
ROUTE	4	0.139	R30C14C.Q0 to	R30C12C.C0 uart2/regs/transmitter/fifo_tx/top[2]
ZERO_DEL	---	0.000	R30C12C.C0 to	R30C12C.WADO2 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1228
ROUTE	2	0.000	R30C12C.WADO2 to	R30C12B.WAD2 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WAD2_INT (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT)
		0.232	(40.1% logic, 59.9% route), 2 logic levels.	

Clock Skew Details:

Source Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/SLICE_5313:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.488	*L_R53C5.CLKOP to	R30C14C.CLK uart_clk_c
		0.488	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/SLICE_1230:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.488	*L_R53C5.CLKOP to	R30C12C.CLK uart_clk_c
ZERO_DEL	---	0.000	R30C12C.CLK to	R30C12C.WCKO uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1228
ROUTE	2	0.000	R30C12C.WCKO to	R30C12B.WCK uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT
		0.488	(0.0% logic, 100.0% route), 1 logic levels.	

Passed: The following path meets requirements by 0.128ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source:	FF	Q	uart2/regs/transmitter/fifo_tx/top[2] (from uart_clk_c +)
Destination:	FF	Data in	uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM0 (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT +)
	FF		uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM0

Delay: 0.232ns (40.1% logic, 59.9% route), 2 logic levels.

Constraint Details:

0.232ns physical path delay uart2/regs/transmitter/fifo_tx/SLICE_5313 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1229 meets
0.104ns WAD_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling 0.104ns) by 0.128ns

Physical Path Details:

Data path uart2/regs/transmitter/fifo_tx/SLICE_5313 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1229:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R30C14C.CLK to	R30C14C.Q0 uart2/regs/transmitter/fifo_tx/SLICE_5313 (from uart_clk_c)
ROUTE	4	0.139	R30C14C.Q0 to	R30C12C.C0 uart2/regs/transmitter/fifo_tx/top[2]
ZERO_DEL	---	0.000	R30C12C.C0 to	R30C12C.WADO2 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1228
ROUTE	2	0.000	R30C12C.WADO2 to	R30C12A.WAD2 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WAD2_INT (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT)
		0.232	(40.1% logic, 59.9% route), 2 logic levels.	

Clock Skew Details:

Source Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/SLICE_5313:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.488	*L_R53C5.CLKOP to	R30C14C.CLK uart_clk_c
		0.488	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1229:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.488	*L_R53C5.CLKOP to	R30C12C.CLK uart_clk_c
ZERO_DEL	---	0.000	R30C12C.CLK to	R30C12C.WCKO uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1228
ROUTE	2	0.000	R30C12C.WCKO to	R30C12A.WCK uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT
		0.488	(0.0% logic, 100.0% route), 1 logic levels.	

Passed: The following path meets requirements by 0.128ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source:	FF	Q	uart2/regs/transmitter/fifo_tx/top[2] (from uart_clk_c +)
Destination:	FF	Data in	uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM0 (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT +)
	FF		uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/RAM0

Delay: 0.232ns (40.1% logic, 59.9% route), 2 logic levels.

Constraint Details:

     0.232ns physical path delay uart2/regs/transmitter/fifo_tx/SLICE_5313 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1232 meets
     0.104ns WAD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.104ns) by 0.128ns

Physical Path Details:

     Data path uart2/regs/transmitter/fifo_tx/SLICE_5313 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1232:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R30C14C.CLK to   R30C14C.Q0 uart2/regs/transmitter/fifo_tx/SLICE_5313 (from uart_clk_c)
ROUTE   4   0.139   R30C14C.Q0 to   R30C13C.C0 uart2/regs/transmitter/fifo_tx/top[2]
ZERO_DEL   ---   0.000   R30C13C.C0 to R30C13C.WADO2 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1231
ROUTE   2   0.000 R30C13C.WADO2 to   R30C13A.WAD2 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/WAD2_INT (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT)

                    0.232   (40.1% logic, 59.9% route), 2 logic levels.

Clock Skew Details:

     Source Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/SLICE_5313:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.488 *L_R53C5.CLKOP to   R30C14C.CLK uart_clk_c
                  ----
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1232:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.488 *L_R53C5.CLKOP to   R30C13C.CLK uart_clk_c
ZERO_DEL   ---   0.000   R30C13C.CLK to   R30C13C.WCKO uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1231
ROUTE   2   0.000   R30C13C.WCKO to   R30C13A.WCK uart2/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT

                    0.488   (0.0% logic, 100.0% route), 1 logic levels.

Passed: The following path meets requirements by 0.132ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   uart2/regs/transmitter/fifo_tx/top[3] (from uart_clk_c +)
   Destination: FF   Data in   uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM1 (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT +)
                   FF   uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM1

   Delay: 0.236ns (39.4% logic, 60.6% route), 2 logic levels.

 Constraint Details:

     0.236ns physical path delay uart2/regs/transmitter/fifo_tx/SLICE_5313 to uart2/regs/transmitter/SLICE_1230 meets
     0.104ns WAD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.104ns) by 0.132ns

 Physical Path Details:

     Data path uart2/regs/transmitter/fifo_tx/SLICE_5313 to uart2/regs/transmitter/SLICE_1230:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R30C14C.CLK to   R30C14C.Q1 uart2/regs/transmitter/fifo_tx/SLICE_5313 (from uart_clk_c)
ROUTE   3   0.143   R30C14C.Q1 to   R30C12C.D0 uart2/regs/transmitter/fifo_tx/top[3]
ZERO_DEL   ---   0.000   R30C12C.D0 to R30C12C.WADO3 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1228
ROUTE   2   0.000 R30C12C.WADO3 to   R30C12B.WAD3 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WAD3_INT (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT)

                    0.236   (39.4% logic, 60.6% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/SLICE_5313:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.488 *L_R53C5.CLKOP to   R30C14C.CLK uart_clk_c
                  ----
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/SLICE_1230:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.488 *L_R53C5.CLKOP to   R30C12C.CLK uart_clk_c
ZERO_DEL   ---   0.000   R30C12C.CLK to   R30C12C.WCKO uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1228
ROUTE   2   0.000   R30C12C.WCKO to   R30C12B.WCK uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT

                    0.488   (0.0% logic, 100.0% route), 1 logic levels.

Passed: The following path meets requirements by 0.132ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   uart2/regs/transmitter/fifo_tx/top[3] (from uart_clk_c +)
   Destination: FF   Data in   uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM0 (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT +)
                   FF   uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM0

   Delay: 0.236ns (39.4% logic, 60.6% route), 2 logic levels.

 Constraint Details:

     0.236ns physical path delay uart2/regs/transmitter/fifo_tx/SLICE_5313 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1229 meets
     0.104ns WAD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.104ns) by 0.132ns

 Physical Path Details:

     Data path uart2/regs/transmitter/fifo_tx/SLICE_5313 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1229:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R30C14C.CLK to   R30C14C.Q1 uart2/regs/transmitter/fifo_tx/SLICE_5313 (from uart_clk_c)
ROUTE   3   0.143   R30C14C.Q1 to   R30C12C.D0 uart2/regs/transmitter/fifo_tx/top[3]
ZERO_DEL   ---   0.000   R30C12C.D0 to R30C12C.WADO3 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1228
ROUTE   2   0.000 R30C12C.WADO3 to   R30C12A.WAD3 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WAD3_INT (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT)

                    0.236   (39.4% logic, 60.6% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/SLICE_5313:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.488 *L_R53C5.CLKOP to   R30C14C.CLK uart_clk_c
                  ----
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1229:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.488 *L_R53C5.CLKOP to   R30C12C.CLK uart_clk_c
ZERO_DEL   ---   0.000   R30C12C.CLK to   R30C12C.WCKO uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1228
ROUTE   2   0.000   R30C12C.WCKO to   R30C12A.WCK uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT

                    0.488   (0.0% logic, 100.0% route), 1 logic levels.

Passed: The following path meets requirements by 0.134ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   uart2/regs/receiver/rf_data_in[9] (from uart_clk_c +)
   Destination: FF   Data in   uart2/regs/receiver/fifo_rx/rfifo/ram_ram_0/RAM1 (to uart2/regs/receiver/fifo_rx/rfifo/ram_ram_0/WCK_INT +)
                   FF   uart2/regs/receiver/fifo_rx/rfifo/ram_ram_0/RAM1

   Delay: 0.196ns (47.4% logic, 52.6% route), 2 logic levels.

 Constraint Details:

     0.196ns physical path delay uart2/regs/receiver/SLICE_5271 to uart2/regs/receiver/fifo_rx/rfifo/ram_ram_0/SLICE_1224 meets
     0.062ns WD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.062ns) by 0.134ns

 Physical Path Details:

     Data path uart2/regs/receiver/SLICE_5271 to uart2/regs/receiver/fifo_rx/rfifo/ram_ram_0/SLICE_1224:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R30C10B.CLK to   R30C10B.Q1 uart2/regs/receiver/SLICE_5271 (from uart_clk_c)
ROUTE   1   0.103   R30C10B.Q1 to   R30C9C.C1 uart2/regs/receiver/rf_data_in[9]
ZERO_DEL   ---   0.000   R30C9C.C1 to   R30C9C.WDO2 uart2/regs/receiver/fifo_rx/rfifo/ram_ram_0/SLICE_1222
ROUTE   1   0.000   R30C9C.WDO2 to   R30C9B.WD0 uart2/regs/receiver/fifo_rx/rfifo/ram_ram_0/WD2_INT (to uart2/regs/receiver/fifo_rx/rfifo/ram_ram_0/WCK_INT)

                    0.196   (47.4% logic, 52.6% route), 2 logic levels.

 Clock Skew Details:

Source Clock Path pll_uarts/PLLInst_0 to uart2/regs/receiver/SLICE_5271:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.488 *L_R53C5.CLKOP to	R30C10B.CLK	uart_clk_c
		0.488 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pll_uarts/PLLInst_0 to uart2/regs/receiver/fifo_rx/rfifo/ram_ram_0/SLICE_1224:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.488 *L_R53C5.CLKOP to	R30C9C.CLK	uart_clk_c
ZERO_DEL	---	0.000 R30C9C.CLK to	R30C9C.WCKO	uart2/regs/receiver/fifo_rx/rfifo/ram_ram_0/SLICE_1222
ROUTE	2	0.000 R30C9C.WCKO to	R30C9B.WCK	uart2/regs/receiver/fifo_rx/rfifo/ram_ram_0/WCK_INT
		0.488 (0.0% logic, 100.0% route), 1 logic levels.		

Passed: The following path meets requirements by 0.138ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source:	FF	Q	uart2/regs/receiver/fifo_rx/top[3] (from uart_clk_c +)
Destination:	FF	Data in	uart2/regs/receiver/fifo_rx/rfifo/ram_ram/RAM0 (to uart2/regs/receiver/fifo_rx/rfifo/ram_ram/WCK_INT +)
	FF		uart2/regs/receiver/fifo_rx/rfifo/ram_ram/RAM0

Delay: 0.242ns (38.4% logic, 61.6% route), 2 logic levels.

Constraint Details:

0.242ns physical path delay uart2/regs/receiver/fifo_rx/SLICE_5261 to uart2/regs/receiver/fifo_rx/rfifo/ram_ram/SLICE_1226 meets
0.104ns WAD_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling 0.104ns) by 0.138ns

Physical Path Details:

Data path uart2/regs/receiver/fifo_rx/SLICE_5261 to uart2/regs/receiver/fifo_rx/rfifo/ram_ram/SLICE_1226:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093 R28C6A.CLK to	R28C6A.Q1	uart2/regs/receiver/fifo_rx/SLICE_5261 (from uart_clk_c)
ROUTE	17	0.149 R28C6A.Q1 to	R30C7C.D0	uart2/regs/receiver/fifo_rx/top[3]
ZERO_DEL	---	0.000 R30C7C.D0 to	R30C7C.WADO3	uart2/regs/receiver/fifo_rx/rfifo/ram_ram/SLICE_1225
ROUTE	2	0.000 R30C7C.WADO3 to	R30C7A.WAD3	uart2/regs/receiver/fifo_rx/rfifo/ram_ram/WAD3_INT (to uart2/regs/receiver/fifo_rx/rfifo/ram_ram/WCK_INT)
		0.242 (38.4% logic, 61.6% route), 2 logic levels.		

Clock Skew Details:

Source Clock Path pll_uarts/PLLInst_0 to uart2/regs/receiver/fifo_rx/SLICE_5261:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.488 *L_R53C5.CLKOP to	R28C6A.CLK	uart_clk_c
		0.488 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pll_uarts/PLLInst_0 to uart2/regs/receiver/fifo_rx/rfifo/ram_ram/SLICE_1226:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.488 *L_R53C5.CLKOP to	R30C7C.CLK	uart_clk_c
ZERO_DEL	---	0.000 R30C7C.CLK to	R30C7C.WCKO	uart2/regs/receiver/fifo_rx/rfifo/ram_ram/SLICE_1225
ROUTE	2	0.000 R30C7C.WCKO to	R30C7A.WCK	uart2/regs/receiver/fifo_rx/rfifo/ram_ram/WCK_INT
		0.488 (0.0% logic, 100.0% route), 1 logic levels.		

==========
Preference: FREQUENCY NET "pcie/pclk" 250.000000 MHz ;
987 items scored, 0 timing errors detected.

Passed: The following path meets requirements by 0.127ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source:	FF	Q	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/ltssm_fndisp_8 (from pcie/pclk +)
Destination:	PCSD	Port	pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0(ASIC) (to pcie/pclk +)

Delay: 0.473ns (19.7% logic, 80.3% route), 1 logic levels.

Constraint Details:

0.473ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/SLICE_3271 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 meets
0.287ns FFTXD_HLD and
0.000ns delay constraint less
-0.059ns skew requirement (totaling 0.346ns) by 0.127ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/SLICE_3271 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093 R57C56A.CLK to	R57C56A.Q1	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/SLICE_3271 (from pcie/pclk)
ROUTE	1	0.380 R57C56A.Q1 to	*A.FF_TX_D_0_9	pcie/txp_compliance_ln0 (to pcie/pclk)
		0.473 (19.7% logic, 80.3% route), 1 logic levels.		

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/SLICE_3271:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	192	0.527 *FF_TX_F_CLK_0 to	R57C56A.CLK	pcie/pclk
		0.527 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	192	0.586 *FF_TX_F_CLK_0 to	*.FF_TXI_CLK_0	pcie/pclk
		0.586 (0.0% logic, 100.0% route), 0 logic levels.		

Passed: The following path meets requirements by 0.189ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source:	FF	Q	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/asb_lane_sync_reg4_0 (from pcie/pclk +)
Destination:	FF	Data in	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_2/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_2/WCK_INT +)

Delay: 0.251ns (37.1% logic, 62.9% route), 2 logic levels.

Constraint Details:

0.251ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/SLICE_3260 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_2/SLICE_1357 meets
0.062ns WD_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling 0.062ns) by 0.189ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/SLICE_3260 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_2/SLICE_1357:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093 R13C60A.CLK to	R13C60A.Q1	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/SLICE_3260 (from pcie/pclk)
ROUTE	2	0.158 R13C60A.Q1 to	R12C60C.A1	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/asb_lane_sync_reg4
ZERO_DEL	---	0.000 R12C60C.A1 to	R12C60C.WDO0	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_2/SLICE_1356
ROUTE	1	0.000 R12C60C.WDO0 to	R12C60A.WD0	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_2/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_2/WCK_INT)
		0.251 (37.1% logic, 62.9% route), 2 logic levels.		

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/SLICE_3260:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	192	0.527 *FF_TX_F_CLK_0 to	R13C60A.CLK	pcie/pclk
		0.527 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_2/SLICE_1357:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	192	0.527 *FF_TX_F_CLK_0 to	R12C60C.CLK	pcie/pclk
ZERO_DEL	---	0.000 R12C60C.CLK to	R12C60C.WCKO	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_2/SLICE_1356
ROUTE	2	0.000 R12C60C.WCKO to	R12C60A.WCK	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_2/WCK_INT
		0.527 (0.0% logic, 100.0% route), 1 logic levels.		

Passed: The following path meets requirements by 0.201ns

```
 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/ts_active  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/ts_active  (to pcie/pclk +)

   Delay:               0.190ns  (78.4% logic, 21.6% route), 2 logic levels.

 Constraint Details:

     0.190ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3304 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3304 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 0.201ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3304 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3304:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R28C48B.CLK to     R28C48B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3304 (from pcie/pclk)
ROUTE        13     0.041     R28C48B.Q0 to     R28C48B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/ts_active
CTOF_DEL    ---     0.056     R28C48B.D0 to     R28C48B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3304
ROUTE         1     0.000     R28C48B.F0 to    R28C48B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/ts_active5 (to pcie/pclk)
                   --------
                     0.190   (78.4% logic, 21.6% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3304:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R28C48B.CLK pcie/pclk
                   --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3304:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R28C48B.CLK pcie/pclk
                   --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.201ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_pipe/line_active  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_pipe/line_active  (to pcie/pclk +)

   Delay:               0.190ns  (78.4% logic, 21.6% route), 2 logic levels.

 Constraint Details:

     0.190ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_pipe/SLICE_3344 to pcie/u1_dut/u1_dut/u1_dut/u1_pipe/SLICE_3344 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 0.201ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_pipe/SLICE_3344 to pcie/u1_dut/u1_dut/u1_dut/u1_pipe/SLICE_3344:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R27C59A.CLK to     R27C59A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_pipe/SLICE_3344 (from pcie/pclk)
ROUTE         3     0.041     R27C59A.Q0 to     R27C59A.D0 pcie/u1_dut/u1_dut/u1_dut/u1_pipe/line_active
CTOF_DEL    ---     0.056     R27C59A.D0 to     R27C59A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_pipe/SLICE_3344
ROUTE         1     0.000     R27C59A.F0 to    R27C59A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_pipe/line_active_RNO (to pcie/pclk)
                   --------
                     0.190   (78.4% logic, 21.6% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_pipe/SLICE_3344:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R27C59A.CLK pcie/pclk
                   --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_pipe/SLICE_3344:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R27C59A.CLK pcie/pclk
                   --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.202ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_en  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_en  (to pcie/pclk +)

   Delay:               0.191ns  (78.0% logic, 22.0% route), 2 logic levels.

 Constraint Details:

     0.191ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3337 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3337 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 0.202ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3337 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3337:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R36C58B.CLK to     R36C58B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3337 (from pcie/pclk)
ROUTE        14     0.042     R36C58B.Q0 to     R36C58B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_en
CTOF_DEL    ---     0.056     R36C58B.D0 to     R36C58B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3337
ROUTE         1     0.000     R36C58B.F0 to    R36C58B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/un13_data_out_0_a2 (to pcie/pclk)
                   --------
                     0.191   (78.0% logic, 22.0% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3337:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R36C58B.CLK pcie/pclk
                   --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3337:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R36C58B.CLK pcie/pclk
                   --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.202ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/ts_active  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/ts_active  (to pcie/pclk +)

   Delay:               0.191ns  (78.0% logic, 22.0% route), 2 logic levels.

 Constraint Details:

     0.191ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/SLICE_3332 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 0.202ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R34C57B.CLK to     R34C57B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/SLICE_3332 (from pcie/pclk)
ROUTE        13     0.042     R34C57B.Q0 to     R34C57B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/ts_active
CTOF_DEL    ---     0.056     R34C57B.D0 to     R34C57B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/SLICE_3332
ROUTE         1     0.000     R34C57B.F0 to    R34C57B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/ts_active5 (to pcie/pclk)
                   --------
                     0.191   (78.0% logic, 22.0% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/SLICE_3332:
```

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R34C57B.CLK pcie/pclk
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R34C57B.CLK pcie/pclk
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.203ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/wr_en  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/wr_en  (to pcie/pclk +)

   Delay:               0.192ns  (77.6% logic, 22.4% route), 2 logic levels.

 Constraint Details:

      0.192ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3314 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3314 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.203ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3314 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3314:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R19C60B.CLK to     R19C60B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3314 (from pcie/pclk)
ROUTE        19     0.043     R19C60B.Q0 to     R19C60B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/wr_en
CTOF_DEL    ---     0.056     R19C60B.D0 to     R19C60B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3314
ROUTE         1     0.000     R19C60B.F0 to    R19C60B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/wr_en_3 (to pcie/pclk)
                    --------
                      0.192   (77.6% logic, 22.4% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3314:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R19C60B.CLK pcie/pclk
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3314:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R19C60B.CLK pcie/pclk
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.205ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_pcs_pipe/cs_reqdet_sm[1]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_pcs_pipe/cs_reqdet_sm[1]  (to pcie/pclk +)

   Delay:               0.194ns  (76.8% logic, 23.2% route), 2 logic levels.

 Constraint Details:

      0.194ns physical path delay pcie/u1_pcs_pipe/SLICE_4192 to pcie/u1_pcs_pipe/SLICE_4192 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.205ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/SLICE_4192 to pcie/u1_pcs_pipe/SLICE_4192:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R47C65B.CLK to     R47C65B.Q0 pcie/u1_pcs_pipe/SLICE_4192 (from pcie/pclk)
ROUTE         9     0.045     R47C65B.Q0 to     R47C65B.D0 pcie/u1_pcs_pipe/cs_reqdet_sm[1]
CTOF_DEL    ---     0.056     R47C65B.D0 to     R47C65B.F0 pcie/u1_pcs_pipe/SLICE_4192
ROUTE         1     0.000     R47C65B.F0 to    R47C65B.DI0 pcie/u1_pcs_pipe/N_238_i (to pcie/pclk)
                    --------
                      0.194   (76.8% logic, 23.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/SLICE_4192:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R47C65B.CLK pcie/pclk
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/SLICE_4192:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R47C65B.CLK pcie/pclk
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.208ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/wr_pntr[0]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/RAM1

   Delay:               0.312ns  (29.8% logic, 70.2% route), 2 logic levels.

 Constraint Details:

      0.312ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3315 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1377 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.208ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3315 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1377:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R19C60A.CLK to     R19C60A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3315 (from pcie/pclk)
ROUTE        18     0.219     R19C60A.Q0 to     R21C60C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/wr_pntr[0]
ZERO_DEL    ---     0.000     R21C60C.A0 to  R21C60C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1375
ROUTE         2     0.000  R21C60C.WADO0 to   R21C60B.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/WCK_INT)
                    --------
                      0.312   (29.8% logic, 70.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3315:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R19C60A.CLK pcie/pclk
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1377:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R21C60C.CLK pcie/pclk
ZERO_DEL    ---     0.000    R21C60C.CLK to   R21C60C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1375
ROUTE         2     0.000   R21C60C.WCKO to    R21C60B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/WCK_INT
                    --------
                      0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.208ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/wr_pntr[0]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/RAM0

   Delay:               0.312ns  (29.8% logic, 70.2% route), 2 logic levels.

 Constraint Details:
```

0.312ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3315 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1376 meets
0.104ns WAD_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling 0.104ns) by 0.208ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3315 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1376:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R19C60A.CLK to	R19C60A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3315 (from pcie/pclk)
ROUTE	18	0.219	R19C60A.Q0 to	R21C60C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/wr_pntr[0]
ZERO_DEL	---	0.000	R21C60C.A0 to	R21C60C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1375
ROUTE	2	0.000	R21C60C.WADO0 to	R21C60A.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/WCK_INT)
		0.312	(29.8% logic, 70.2% route), 2 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3315:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	192	0.527	*FF_TX_F_CLK_0 to	R19C60A.CLK pcie/pclk
		0.527	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1376:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	192	0.527	*FF_TX_F_CLK_0 to	R21C60C.CLK pcie/pclk
ZERO_DEL	---	0.000	R21C60C.CLK to	R21C60C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1375
ROUTE	2	0.000	R21C60C.WCKO to	R21C60A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/WCK_INT
		0.527	(0.0% logic, 100.0% route), 1 logic levels.	

==
Preference: FREQUENCY NET "pcie/u1_pcs_pipe/ff_rx_fclk_0" 250.000000 MHz ;
1 item scored, 0 timing errors detected.

Passed: The following path meets requirements by 0.227ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_pcs_pipe/pipe_top_0/sync1_RxPolarity (from pcie/u1_pcs_pipe/ff_rx_fclk_0 +)
Destination: FF Data in pcie/u1_pcs_pipe/pipe_top_0/sync2_RxPolarity (to pcie/u1_pcs_pipe/ff_rx_fclk_0 +)

Delay: 0.179ns (52.0% logic, 48.0% route), 1 logic levels.

Constraint Details:

0.179ns physical path delay pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248 meets
-0.048ns M_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.048ns) by 0.227ns

Physical Path Details:

Data path pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R42C62B.CLK to	R42C62B.Q0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248 (from pcie/u1_pcs_pipe/ff_rx_fclk_0)
ROUTE	1	0.086	R42C62B.Q0 to	R42C62B.M1 pcie/u1_pcs_pipe/pipe_top_0/sync1_RxPolarity (to pcie/u1_pcs_pipe/ff_rx_fclk_0)
		0.179	(52.0% logic, 48.0% route), 1 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	1	1.216	*FF_RX_F_CLK_0 to	R42C62B.CLK pcie/u1_pcs_pipe/ff_rx_fclk_0
		1.216	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4248:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	1	1.216	*FF_RX_F_CLK_0 to	R42C62B.CLK pcie/u1_pcs_pipe/ff_rx_fclk_0
		1.216	(0.0% logic, 100.0% route), 0 logic levels.	

==
Preference: BLOCK PATH FROM PORT "rstn" ;
119 items scored, 0 timing errors detected.

==
Preference: BLOCK PATH TO PORT "OUT*" ;
0 items scored, 0 timing errors detected.

==
Preference: BLOCK PATH FROM PORT "INP*" ;
16 items scored, 0 timing errors detected.

==
Preference: BLOCK PATH FROM PORT "SRAM_A*" ;
0 items scored, 0 timing errors detected.

==
Preference: BLOCK PATH TO PORT "LED*" ;
8 items scored, 0 timing errors detected.

==
Preference: BLOCK PATH FROM CELL "*ctc_reset_chx*" ;
14 items scored, 0 timing errors detected.

==
Preference: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*cnt_done_nfts_rx*" 2.000000 X ;
214 items scored, 0 timing errors detected.

Passed: The following path meets requirements by 1.014ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[8] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx (to clk_125_c +)

Delay: 1.003ns (46.5% logic, 53.5% route), 11 logic levels.

Constraint Details:

1.003ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
-0.011ns DIN_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.011ns) by 1.014ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R23C69C.CLK to	R23C69C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962 (from clk_125_c)
ROUTE	3	0.283	R23C69C.Q1 to	R19C69B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[8]
C1TOFCO_DE	---	0.093	R19C69B.B1 to	R19C69B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE	1	0.000	R19C69B.FCO to	R19C69C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
FCITOFCO_D	---	0.022	R19C69C.FCI to	R19C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE	1	0.000	R19C69C.FCO to	R19C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D	---	0.022	R19C70A.FCI to	R19C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE	1	0.000	R19C70A.FCO to	R19C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D	---	0.022	R19C70B.FCI to	R19C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE	1	0.000	R19C70B.FCO to	R19C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D	---	0.022	R19C70C.FCI to	R19C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE	1	0.000	R19C70C.FCO to	R19C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D	---	0.022	R19C71A.FCI to	R19C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1032
ROUTE	1	0.000	R19C71A.FCO to	R19C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D	---	0.022	R19C71B.FCI to	R19C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1033
ROUTE	1	0.000	R19C71B.FCO to	R19C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]

```
FCITOFCO_D  ---     0.022    R19C71C.FCI to    R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE         1     0.000    R19C71C.FCO to    R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070    R19C72A.FCI to     R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE         1     0.254     R19C72A.F1 to     R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056     R23C69B.D0 to     R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE         1     0.000     R23C69B.F0 to    R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.003   (46.5% logic, 53.5% route), 11 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C69C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C69B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.039ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[5]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.028ns  (47.6% logic, 52.4% route), 12 logic levels.

 Constraint Details:

      1.028ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.039ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R23C69C.CLK to     R23C69C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962 (from clk_125_c)
ROUTE         8     0.285     R23C69C.Q0 to     R19C69A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[5]
C0TOFCO_DE  ---     0.094     R19C69A.A0 to    R19C69A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000    R19C69A.FCO to    R19C69B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[6]
FCITOFCO_D  ---     0.022    R19C69B.FCI to    R19C69B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000    R19C69B.FCO to    R19C69C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
FCITOFCO_D  ---     0.022    R19C69C.FCI to    R19C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000    R19C69C.FCO to    R19C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.022    R19C70A.FCI to    R19C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000    R19C70A.FCO to    R19C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.022    R19C70B.FCI to    R19C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000    R19C70B.FCO to    R19C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022    R19C70C.FCI to    R19C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.000    R19C70C.FCO to    R19C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022    R19C71A.FCI to    R19C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1032
ROUTE         1     0.000    R19C71A.FCO to    R19C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022    R19C71B.FCI to    R19C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1033
ROUTE         1     0.000    R19C71B.FCO to    R19C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022    R19C71C.FCI to    R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE         1     0.000    R19C71C.FCO to    R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070    R19C72A.FCI to     R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE         1     0.254     R19C72A.F1 to     R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056     R23C69B.D0 to     R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE         1     0.000     R23C69B.F0 to    R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.028   (47.6% logic, 52.4% route), 12 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C69C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C69B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.069ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[2]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.058ns  (48.3% logic, 51.7% route), 13 logic levels.

 Constraint Details:

      1.058ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.069ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R23C68A.CLK to     R23C68A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 (from clk_125_c)
ROUTE        16     0.293     R23C68A.Q1 to     R19C68C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[2]
C0TOFCO_DE  ---     0.094     R19C68C.B0 to    R19C68C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000    R19C68C.FCO to    R19C69A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[4]
FCITOFCO_D  ---     0.022    R19C69A.FCI to    R19C69A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000    R19C69A.FCO to    R19C69B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[6]
FCITOFCO_D  ---     0.022    R19C69B.FCI to    R19C69B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000    R19C69B.FCO to    R19C69C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
FCITOFCO_D  ---     0.022    R19C69C.FCI to    R19C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000    R19C69C.FCO to    R19C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.022    R19C70A.FCI to    R19C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000    R19C70A.FCO to    R19C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.022    R19C70B.FCI to    R19C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000    R19C70B.FCO to    R19C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022    R19C70C.FCI to    R19C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.000    R19C70C.FCO to    R19C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022    R19C71A.FCI to    R19C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1032
ROUTE         1     0.000    R19C71A.FCO to    R19C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022    R19C71B.FCI to    R19C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1033
ROUTE         1     0.000    R19C71B.FCO to    R19C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022    R19C71C.FCI to    R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE         1     0.000    R19C71C.FCO to    R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070    R19C72A.FCI to     R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE         1     0.254     R19C72A.F1 to     R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056     R23C69B.D0 to     R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE         1     0.000     R23C69B.F0 to    R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.058   (48.3% logic, 51.7% route), 13 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C68A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C69B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.069ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)
```

```
  Delay:               1.058ns  (42.1% logic, 57.9% route), 10 logic levels.

 Constraint Details:

     1.058ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 1.069ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R21C71C.CLK to     R21C71C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 (from clk_125_c)
ROUTE         9     0.359     R21C71C.Q0 to     R19C69C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]
C0TOFCO_DE  ---     0.094     R19C69C.B0 to    R19C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000    R19C69C.FCO to    R19C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.022    R19C70A.FCI to    R19C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000    R19C70A.FCO to    R19C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.022    R19C70B.FCI to    R19C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000    R19C70B.FCO to    R19C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022    R19C70C.FCI to    R19C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.000    R19C70C.FCO to    R19C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022    R19C71A.FCI to    R19C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1032
ROUTE         1     0.000    R19C71A.FCO to    R19C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022    R19C71B.FCI to    R19C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1033
ROUTE         1     0.000    R19C71B.FCO to    R19C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022    R19C71C.FCI to    R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE         1     0.000    R19C71C.FCO to    R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070    R19C72A.FCI to     R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE         1     0.254     R19C72A.F1 to     R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056     R23C69B.D0 to     R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE         1     0.000     R23C69B.F0 to    R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.058   (42.1% logic, 57.9% route), 10 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R21C71C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C69B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.072ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[6]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.061ns  (46.0% logic, 54.0% route), 12 logic levels.

 Constraint Details:

     1.061ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_979 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 1.072ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_979 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R23C71A.CLK to     R23C71A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_979 (from clk_125_c)
ROUTE         6     0.319     R23C71A.Q0 to     R19C69A.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[6]
C1TOFCO_DE  ---     0.093     R19C69A.A1 to    R19C69A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000    R19C69A.FCO to    R19C69B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[6]
FCITOFCO_D  ---     0.022    R19C69B.FCI to    R19C69B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000    R19C69B.FCO to    R19C69C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
FCITOFCO_D  ---     0.022    R19C69C.FCI to    R19C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000    R19C69C.FCO to    R19C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.022    R19C70A.FCI to    R19C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000    R19C70A.FCO to    R19C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.022    R19C70B.FCI to    R19C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000    R19C70B.FCO to    R19C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022    R19C70C.FCI to    R19C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.000    R19C70C.FCO to    R19C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022    R19C71A.FCI to    R19C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1032
ROUTE         1     0.000    R19C71A.FCO to    R19C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022    R19C71B.FCI to    R19C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1033
ROUTE         1     0.000    R19C71B.FCO to    R19C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022    R19C71C.FCI to    R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE         1     0.000    R19C71C.FCO to    R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070    R19C72A.FCI to     R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE         1     0.254     R19C72A.F1 to     R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056     R23C69B.D0 to     R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE         1     0.000     R23C69B.F0 to    R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.061   (46.0% logic, 54.0% route), 12 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_979:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C71A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C69B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.089ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[2]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.078ns  (49.4% logic, 50.6% route), 14 logic levels.

 Constraint Details:

     1.078ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 1.089ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R23C68A.CLK to     R23C68A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 (from clk_125_c)
ROUTE        16     0.292     R23C68A.Q1 to     R19C68B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[2]
C1TOFCO_DE  ---     0.093     R19C68B.A1 to    R19C68B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024
ROUTE         1     0.000    R19C68B.FCO to    R19C68C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[2]
FCITOFCO_D  ---     0.022    R19C68C.FCI to    R19C68C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000    R19C68C.FCO to    R19C69A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[4]
FCITOFCO_D  ---     0.022    R19C69A.FCI to    R19C69A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000    R19C69A.FCO to    R19C69B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[6]
FCITOFCO_D  ---     0.022    R19C69B.FCI to    R19C69B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000    R19C69B.FCO to    R19C69C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
FCITOFCO_D  ---     0.022    R19C69C.FCI to    R19C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000    R19C69C.FCO to    R19C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.022    R19C70A.FCI to    R19C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000    R19C70A.FCO to    R19C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.022    R19C70B.FCI to    R19C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000    R19C70B.FCO to    R19C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022    R19C70C.FCI to    R19C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.000    R19C70C.FCO to    R19C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022    R19C71A.FCI to    R19C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1032
ROUTE         1     0.000    R19C71A.FCO to    R19C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022    R19C71B.FCI to    R19C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1033
ROUTE         1     0.000    R19C71B.FCO to    R19C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022    R19C71C.FCI to    R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
```

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ROUTE         1     0.000    R19C71C.FCO to    R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070    R19C72A.FCI to     R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE         1     0.254     R19C72A.F1 to     R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056     R23C69B.D0 to     R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE         1     0.000     R23C69B.F0 to    R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.078   (49.4% logic, 50.6% route), 14 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C68A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C69B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.091ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.080ns  (49.4% logic, 50.6% route), 14 logic levels.

 Constraint Details:

      1.080ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.091ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R23C68A.CLK to     R23C68A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 (from clk_125_c)
ROUTE        11     0.293     R23C68A.Q0 to     R19C68B.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[1]
C0TOFCO_DE  ---     0.094     R19C68B.A0 to    R19C68B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024
ROUTE         1     0.000    R19C68B.FCO to    R19C68C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[2]
FCITOFCO_D  ---     0.022    R19C68C.FCI to    R19C68C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000    R19C68C.FCO to    R19C69A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[4]
FCITOFCO_D  ---     0.022    R19C69A.FCI to    R19C69A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000    R19C69A.FCO to    R19C69B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[6]
FCITOFCO_D  ---     0.022    R19C69B.FCI to    R19C69B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000    R19C69B.FCO to    R19C69C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
FCITOFCO_D  ---     0.022    R19C69C.FCI to    R19C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000    R19C69C.FCO to    R19C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.022    R19C70A.FCI to    R19C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000    R19C70A.FCO to    R19C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.022    R19C70B.FCI to    R19C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000    R19C70B.FCO to    R19C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022    R19C70C.FCI to    R19C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.000    R19C70C.FCO to    R19C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022    R19C71A.FCI to    R19C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1032
ROUTE         1     0.000    R19C71A.FCO to    R19C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022    R19C71B.FCI to    R19C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1033
ROUTE         1     0.000    R19C71B.FCO to    R19C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022    R19C71C.FCI to    R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE         1     0.000    R19C71C.FCO to    R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070    R19C72A.FCI to     R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE         1     0.254     R19C72A.F1 to     R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056     R23C69B.D0 to     R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE         1     0.000     R23C69B.F0 to    R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.080   (49.4% logic, 50.6% route), 14 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C68A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C69B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.144ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[2]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.133ns  (47.0% logic, 53.0% route), 14 logic levels.

 Constraint Details:

      1.133ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.144ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R23C68A.CLK to     R23C68A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 (from clk_125_c)
ROUTE        16     0.347     R23C68A.Q1 to     R19C68B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[2]
C1TOFCO_DE  ---     0.093     R19C68B.B1 to    R19C68B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024
ROUTE         1     0.000    R19C68B.FCO to    R19C68C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[2]
FCITOFCO_D  ---     0.022    R19C68C.FCI to    R19C68C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000    R19C68C.FCO to    R19C69A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[4]
FCITOFCO_D  ---     0.022    R19C69A.FCI to    R19C69A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000    R19C69A.FCO to    R19C69B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[6]
FCITOFCO_D  ---     0.022    R19C69B.FCI to    R19C69B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000    R19C69B.FCO to    R19C69C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
FCITOFCO_D  ---     0.022    R19C69C.FCI to    R19C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000    R19C69C.FCO to    R19C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.022    R19C70A.FCI to    R19C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000    R19C70A.FCO to    R19C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.022    R19C70B.FCI to    R19C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000    R19C70B.FCO to    R19C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022    R19C70C.FCI to    R19C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.000    R19C70C.FCO to    R19C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022    R19C71A.FCI to    R19C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1032
ROUTE         1     0.000    R19C71A.FCO to    R19C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022    R19C71B.FCI to    R19C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1033
ROUTE         1     0.000    R19C71B.FCO to    R19C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022    R19C71C.FCI to    R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE         1     0.000    R19C71C.FCO to    R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070    R19C72A.FCI to     R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE         1     0.254     R19C72A.F1 to     R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056     R23C69B.D0 to     R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE         1     0.000     R23C69B.F0 to    R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.133   (47.0% logic, 53.0% route), 14 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C68A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C69B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.145ns
```

```
 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[8]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.134ns  (41.4% logic, 58.6% route), 8 logic levels.

 Constraint Details:

     1.134ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_980 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 1.145ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_980 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R23C71B.CLK to     R23C71B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_980 (from clk_125_c)
ROUTE         2     0.137     R23C71B.Q0 to     R22C71D.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[8]
CTOF_DEL    ---     0.056     R22C71D.C1 to     R22C71D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7777
ROUTE        22     0.164     R22C71D.F1 to     R19C71D.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_1_0
CTOF_DEL    ---     0.056     R19C71D.D1 to     R19C71D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8028
ROUTE         1     0.110     R19C71D.F1 to     R19C71A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_df18
C0TOFCO_DE  ---     0.094     R19C71A.A0 to    R19C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1032
ROUTE         1     0.000    R19C71A.FCO to    R19C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022    R19C71B.FCI to    R19C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1033
ROUTE         1     0.000    R19C71B.FCO to    R19C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022    R19C71C.FCI to    R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE         1     0.000    R19C71C.FCO to    R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070    R19C72A.FCI to     R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE         1     0.254     R19C72A.F1 to     R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056     R23C69B.D0 to     R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE         1     0.000     R23C69B.F0 to    R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.134   (41.4% logic, 58.6% route), 8 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_980:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C71B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C69B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.148ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[8]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.137ns  (44.1% logic, 55.9% route), 11 logic levels.

 Constraint Details:

     1.137ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 1.148ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R23C69C.CLK to     R23C69C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962 (from clk_125_c)
ROUTE         3     0.235     R23C69C.Q1 to     R19C69D.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[8]
CTOF_DEL    ---     0.056     R19C69D.C0 to     R19C69D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_9447
ROUTE         1     0.147     R19C69D.F0 to     R19C69C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c7_i
C0TOFCO_DE  ---     0.094     R19C69C.A0 to    R19C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000    R19C69C.FCO to    R19C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.022    R19C70A.FCI to    R19C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000    R19C70A.FCO to    R19C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.022    R19C70B.FCI to    R19C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000    R19C70B.FCO to    R19C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022    R19C70C.FCI to    R19C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.000    R19C70C.FCO to    R19C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022    R19C71A.FCI to    R19C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1032
ROUTE         1     0.000    R19C71A.FCO to    R19C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022    R19C71B.FCI to    R19C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1033
ROUTE         1     0.000    R19C71B.FCO to    R19C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022    R19C71C.FCI to    R19C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1034
ROUTE         1     0.000    R19C71C.FCO to    R19C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070    R19C72A.FCI to     R19C72A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1035
ROUTE         1     0.254     R19C72A.F1 to     R23C69B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056     R23C69B.D0 to     R23C69B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850
ROUTE         1     0.000     R23C69B.F0 to    R23C69B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.137   (44.1% logic, 55.9% route), 11 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C69C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2850:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R23C69B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


================================================================================
Preference: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*ltssm_nfts_rx_skp*" 2.000000 X ;
            244 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 1.021ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               1.010ns  (37.3% logic, 62.7% route), 8 logic levels.

 Constraint Details:

     1.010ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 1.021ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R21C71C.CLK to     R21C71C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 (from clk_125_c)
ROUTE         9     0.294     R21C71C.Q0 to     R18C70B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]
C1TOFCO_DE  ---     0.093     R18C70B.A1 to    R18C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000    R18C70B.FCO to    R18C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D  ---     0.022    R18C70C.FCI to    R18C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     0.000    R18C70C.FCO to    R18C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D  ---     0.022    R18C71A.FCI to    R18C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1006
ROUTE         1     0.000    R18C71A.FCO to    R18C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.022    R18C71B.FCI to    R18C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE         1     0.000    R18C71B.FCO to    R18C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.022    R18C71C.FCI to    R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE         1     0.000    R18C71C.FCO to    R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.047    R18C72A.FCI to     R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE         1     0.339     R18C72A.F0 to     R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.056     R21C70A.A0 to     R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE         1     0.000     R21C70A.F0 to    R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    1.010   (37.3% logic, 62.7% route), 8 logic levels.
```

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527 *FF_TX_H_CLK_0 to	R21C71C.CLK	clk_125_c
		0.527 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527 *FF_TX_H_CLK_0 to	R21C70A.CLK	clk_125_c
		0.527 (0.0% logic, 100.0% route), 0 logic levels.		

Passed: The following path meets requirements by 1.022ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

Delay: 1.011ns (37.4% logic, 62.6% route), 8 logic levels.

Constraint Details:

1.011ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
-0.011ns DIN_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.011ns) by 1.022ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093 R21C71C.CLK to	R21C71C.Q0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 (from clk_125_c)
ROUTE	9	0.294 R21C71C.Q0 to	R18C70B.A0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]
C0TOFCO_DE	---	0.094 R18C70B.A0 to	R18C70B.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE	1	0.000 R18C70B.FCO to	R18C70C.FCI	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D	---	0.022 R18C70C.FCI to	R18C70C.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE	1	0.000 R18C70C.FCO to	R18C71A.FCI	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D	---	0.022 R18C71A.FCI to	R18C71A.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1006
ROUTE	1	0.000 R18C71A.FCO to	R18C71B.FCI	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D	---	0.022 R18C71B.FCI to	R18C71B.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE	1	0.000 R18C71B.FCO to	R18C71C.FCI	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D	---	0.022 R18C71C.FCI to	R18C71C.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE	1	0.000 R18C71C.FCO to	R18C72A.FCI	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE	---	0.047 R18C72A.FCI to	R18C72A.F0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE	1	0.339 R18C72A.F0 to	R21C70A.A0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL	---	0.056 R21C70A.A0 to	R21C70A.F0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE	1	0.000 R21C70A.F0 to	R21C70A.DI0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
		1.011 (37.4% logic, 62.6% route), 8 logic levels.		

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527 *FF_TX_H_CLK_0 to	R21C71C.CLK	clk_125_c
		0.527 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527 *FF_TX_H_CLK_0 to	R21C70A.CLK	clk_125_c
		0.527 (0.0% logic, 100.0% route), 0 logic levels.		

Passed: The following path meets requirements by 1.043ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

Delay: 1.032ns (38.7% logic, 61.3% route), 9 logic levels.

Constraint Details:

1.032ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
-0.011ns DIN_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.011ns) by 1.043ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093 R21C71C.CLK to	R21C71C.Q0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 (from clk_125_c)
ROUTE	9	0.294 R21C71C.Q0 to	R18C70A.A1	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]
C1TOFCO_DE	---	0.093 R18C70A.A1 to	R18C70A.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE	1	0.000 R18C70A.FCO to	R18C70B.FCI	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D	---	0.022 R18C70B.FCI to	R18C70B.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE	1	0.000 R18C70B.FCO to	R18C70C.FCI	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D	---	0.022 R18C70C.FCI to	R18C70C.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE	1	0.000 R18C70C.FCO to	R18C71A.FCI	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D	---	0.022 R18C71A.FCI to	R18C71A.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1006
ROUTE	1	0.000 R18C71A.FCO to	R18C71B.FCI	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D	---	0.022 R18C71B.FCI to	R18C71B.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE	1	0.000 R18C71B.FCO to	R18C71C.FCI	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D	---	0.022 R18C71C.FCI to	R18C71C.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE	1	0.000 R18C71C.FCO to	R18C72A.FCI	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE	---	0.047 R18C72A.FCI to	R18C72A.F0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE	1	0.339 R18C72A.F0 to	R21C70A.A0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL	---	0.056 R21C70A.A0 to	R21C70A.F0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE	1	0.000 R21C70A.F0 to	R21C70A.DI0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
		1.032 (38.7% logic, 61.3% route), 9 logic levels.		

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527 *FF_TX_H_CLK_0 to	R21C71C.CLK	clk_125_c
		0.527 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527 *FF_TX_H_CLK_0 to	R21C70A.CLK	clk_125_c
		0.527 (0.0% logic, 100.0% route), 0 logic levels.		

Passed: The following path meets requirements by 1.044ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

Delay: 1.033ns (38.7% logic, 61.3% route), 9 logic levels.

Constraint Details:

1.033ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
-0.011ns DIN_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.011ns) by 1.044ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093 R21C71C.CLK to	R21C71C.Q0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 (from clk_125_c)
ROUTE	9	0.294 R21C71C.Q0 to	R18C70A.A0	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]
C0TOFCO_DE	---	0.094 R18C70A.A0 to	R18C70A.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE	1	0.000 R18C70A.FCO to	R18C70B.FCI	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D	---	0.022 R18C70B.FCI to	R18C70B.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE	1	0.000 R18C70B.FCO to	R18C70C.FCI	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D	---	0.022 R18C70C.FCI to	R18C70C.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE	1	0.000 R18C70C.FCO to	R18C71A.FCI	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D	---	0.022 R18C71A.FCI to	R18C71A.FCO	pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1006

ROUTE   1   0.000   R18C71A.FCO to   R18C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D ---   0.022   R18C71B.FCI to   R18C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE   1   0.000   R18C71B.FCO to   R18C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D ---   0.022   R18C71C.FCI to   R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE   1   0.000   R18C71C.FCO to   R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE ---   0.047   R18C72A.FCI to   R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE   1   0.339   R18C72A.F0 to   R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL   ---   0.056   R21C70A.A0 to   R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE   1   0.000   R21C70A.F0 to   R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)

                    1.033   (38.7% logic, 61.3% route), 9 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R21C71C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R21C70A.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 1.065ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

   Delay: 1.054ns (39.9% logic, 60.1% route), 10 logic levels.

 Constraint Details:

      1.054ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.065ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R21C71C.CLK to   R21C71C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 (from clk_125_c)
ROUTE   9   0.294   R21C71C.Q0 to   R18C69C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]
C1TOFCO_DE ---   0.093   R18C69C.A1 to   R18C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE   1   0.000   R18C69C.FCO to   R18C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11]
FCITOFCO_D ---   0.022   R18C70A.FCI to   R18C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE   1   0.000   R18C70A.FCO to   R18C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D ---   0.022   R18C70B.FCI to   R18C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE   1   0.000   R18C70B.FCO to   R18C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D ---   0.022   R18C70C.FCI to   R18C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE   1   0.000   R18C70C.FCO to   R18C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D ---   0.022   R18C71A.FCI to   R18C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1006
ROUTE   1   0.000   R18C71A.FCO to   R18C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D ---   0.022   R18C71B.FCI to   R18C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE   1   0.000   R18C71B.FCO to   R18C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D ---   0.022   R18C71C.FCI to   R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE   1   0.000   R18C71C.FCO to   R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE ---   0.047   R18C72A.FCI to   R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE   1   0.339   R18C72A.F0 to   R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL   ---   0.056   R21C70A.A0 to   R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE   1   0.000   R21C70A.F0 to   R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)

                    1.054   (39.9% logic, 60.1% route), 10 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R21C71C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R21C70A.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 1.066ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

   Delay: 1.055ns (40.0% logic, 60.0% route), 10 logic levels.

 Constraint Details:

      1.055ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.066ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R21C71C.CLK to   R21C71C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 (from clk_125_c)
ROUTE   9   0.294   R21C71C.Q0 to   R18C69C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]
C0TOFCO_DE ---   0.094   R18C69C.A0 to   R18C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE   1   0.000   R18C69C.FCO to   R18C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11]
FCITOFCO_D ---   0.022   R18C70A.FCI to   R18C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE   1   0.000   R18C70A.FCO to   R18C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D ---   0.022   R18C70B.FCI to   R18C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE   1   0.000   R18C70B.FCO to   R18C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D ---   0.022   R18C70C.FCI to   R18C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE   1   0.000   R18C70C.FCO to   R18C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D ---   0.022   R18C71A.FCI to   R18C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1006
ROUTE   1   0.000   R18C71A.FCO to   R18C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D ---   0.022   R18C71B.FCI to   R18C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE   1   0.000   R18C71B.FCO to   R18C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D ---   0.022   R18C71C.FCI to   R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE   1   0.000   R18C71C.FCO to   R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE ---   0.047   R18C72A.FCI to   R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE   1   0.339   R18C72A.F0 to   R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL   ---   0.056   R21C70A.A0 to   R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE   1   0.000   R21C70A.F0 to   R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)

                    1.055   (40.0% logic, 60.0% route), 10 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R21C71C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R21C70A.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 1.077ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[8] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

   Delay: 1.066ns (41.7% logic, 58.3% route), 11 logic levels.

 Constraint Details:

      1.066ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     -0.011ns DIN_HLD and

      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.077ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R23C69C.CLK to   R23C69C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962 (from clk_125_c)
ROUTE   3   0.283   R23C69C.Q1 to   R18C69B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[8]
C0TOFCO_DE ---   0.094   R18C69B.B0 to   R18C69B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001
ROUTE   1   0.000   R18C69B.FCO to   R18C69C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[9]
FCITOFCO_D ---   0.022   R18C69C.FCI to   R18C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE   1   0.000   R18C69C.FCO to   R18C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11]
FCITOFCO_D ---   0.022   R18C70A.FCI to   R18C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE   1   0.000   R18C70A.FCO to   R18C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D ---   0.022   R18C70B.FCI to   R18C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE   1   0.000   R18C70B.FCO to   R18C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D ---   0.022   R18C70C.FCI to   R18C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE   1   0.000   R18C70C.FCO to   R18C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D ---   0.022   R18C71A.FCI to   R18C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1006
ROUTE   1   0.000   R18C71A.FCO to   R18C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D ---   0.022   R18C71B.FCI to   R18C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE   1   0.000   R18C71B.FCO to   R18C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D ---   0.022   R18C71C.FCI to   R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE   1   0.000   R18C71C.FCO to   R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE ---   0.047   R18C72A.FCI to   R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE   1   0.339   R18C72A.F0 to   R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL   ---   0.056   R21C70A.A0 to   R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE   1   0.000   R21C70A.F0 to   R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)

                    1.066   (41.7% logic, 58.3% route), 11 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2962:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R23C69C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R21C70A.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 1.087ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

   Delay: 1.076ns (41.2% logic, 58.8% route), 11 logic levels.

 Constraint Details:

      1.076ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.087ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R21C71C.CLK to   R21C71C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780 (from clk_125_c)
ROUTE   9   0.294   R21C71C.Q0 to   R18C69B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]
C1TOFCO_DE ---   0.093   R18C69B.A1 to   R18C69B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001
ROUTE   1   0.000   R18C69B.FCO to   R18C69C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[9]
FCITOFCO_D ---   0.022   R18C69C.FCI to   R18C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE   1   0.000   R18C69C.FCO to   R18C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11]
FCITOFCO_D ---   0.022   R18C70A.FCI to   R18C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE   1   0.000   R18C70A.FCO to   R18C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D ---   0.022   R18C70B.FCI to   R18C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE   1   0.000   R18C70B.FCO to   R18C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D ---   0.022   R18C70C.FCI to   R18C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE   1   0.000   R18C70C.FCO to   R18C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D ---   0.022   R18C71A.FCI to   R18C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1006
ROUTE   1   0.000   R18C71A.FCO to   R18C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D ---   0.022   R18C71B.FCI to   R18C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE   1   0.000   R18C71B.FCO to   R18C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D ---   0.022   R18C71C.FCI to   R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE   1   0.000   R18C71C.FCO to   R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE ---   0.047   R18C72A.FCI to   R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE   1   0.339   R18C72A.F0 to   R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL   ---   0.056   R21C70A.A0 to   R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE   1   0.000   R21C70A.F0 to   R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)

                    1.076   (41.2% logic, 58.8% route), 11 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_7780:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R21C71C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R21C70A.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 1.153ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

   Delay: 1.142ns (44.7% logic, 55.3% route), 14 logic levels.

 Constraint Details:

      1.142ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.153ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R23C68A.CLK to   R23C68A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 (from clk_125_c)
ROUTE   11   0.293   R23C68A.Q0 to   R18C68B.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[1]
C0TOFCO_DE ---   0.094   R18C68B.A0 to   R18C68B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_998
ROUTE   1   0.000   R18C68B.FCO to   R18C68C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[3]
FCITOFCO_D ---   0.022   R18C68C.FCI to   R18C68C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_999
ROUTE   1   0.000   R18C68C.FCO to   R18C69A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[5]
FCITOFCO_D ---   0.022   R18C69A.FCI to   R18C69A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1000
ROUTE   1   0.000   R18C69A.FCO to   R18C69B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[7]
FCITOFCO_D ---   0.022   R18C69B.FCI to   R18C69B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001
ROUTE   1   0.000   R18C69B.FCO to   R18C69C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[9]
FCITOFCO_D ---   0.022   R18C69C.FCI to   R18C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE   1   0.000   R18C69C.FCO to   R18C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11]
FCITOFCO_D ---   0.022   R18C70A.FCI to   R18C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE   1   0.000   R18C70A.FCO to   R18C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D ---   0.022   R18C70B.FCI to   R18C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE   1   0.000   R18C70B.FCO to   R18C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D ---   0.022   R18C70C.FCI to   R18C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE   1   0.000   R18C70C.FCO to   R18C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D ---   0.022   R18C71A.FCI to   R18C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1006
ROUTE   1   0.000   R18C71A.FCO to   R18C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D ---   0.022   R18C71B.FCI to   R18C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE   1   0.000   R18C71B.FCO to   R18C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D ---   0.022   R18C71C.FCI to   R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE   1   0.000   R18C71C.FCO to   R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE ---   0.047   R18C72A.FCI to   R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE   1   0.339   R18C72A.F0 to   R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL   ---   0.056   R21C70A.A0 to   R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE   1   0.000   R21C70A.F0 to   R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)

                    1.142   (44.7% logic, 55.3% route), 14 logic levels.

Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R23C68A.CLK clk_125_c
                    ----
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R21C70A.CLK clk_125_c
                    ----
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 1.174ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

   Delay: 1.163ns (45.7% logic, 54.3% route), 15 logic levels.

 Constraint Details:

     1.163ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 1.174ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R23C68A.CLK to   R23C68A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960 (from clk_125_c)
ROUTE   11   0.293   R23C68A.Q0 to   R18C68A.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[1]
C1TOFCO_DE ---   0.093   R18C68A.A1 to   R18C68A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_997
ROUTE   1   0.000   R18C68A.FCO to   R18C68B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[1]
FCITOFCO_D ---   0.022   R18C68B.FCI to   R18C68B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_998
ROUTE   1   0.000   R18C68B.FCO to   R18C68C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[3]
FCITOFCO_D ---   0.022   R18C68C.FCI to   R18C68C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_999
ROUTE   1   0.000   R18C68C.FCO to   R18C69A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[5]
FCITOFCO_D ---   0.022   R18C69A.FCI to   R18C69A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1000
ROUTE   1   0.000   R18C69A.FCO to   R18C69B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[7]
FCITOFCO_D ---   0.022   R18C69B.FCI to   R18C69B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001
ROUTE   1   0.000   R18C69B.FCO to   R18C69C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[9]
FCITOFCO_D ---   0.022   R18C69C.FCI to   R18C69C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE   1   0.000   R18C69C.FCO to   R18C70A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11]
FCITOFCO_D ---   0.022   R18C70A.FCI to   R18C70A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE   1   0.000   R18C70A.FCO to   R18C70B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D ---   0.022   R18C70B.FCI to   R18C70B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE   1   0.000   R18C70B.FCO to   R18C70C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D ---   0.022   R18C70C.FCI to   R18C70C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE   1   0.000   R18C70C.FCO to   R18C71A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D ---   0.022   R18C71A.FCI to   R18C71A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1006
ROUTE   1   0.000   R18C71A.FCO to   R18C71B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D ---   0.022   R18C71B.FCI to   R18C71B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1007
ROUTE   1   0.000   R18C71B.FCO to   R18C71C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D ---   0.022   R18C71C.FCI to   R18C71C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1008
ROUTE   1   0.000   R18C71C.FCO to   R18C72A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE ---   0.047   R18C72A.FCI to   R18C72A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1009
ROUTE   1   0.339   R18C72A.F0 to   R21C70A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL   ---   0.056   R21C70A.A0 to   R21C70A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944
ROUTE   1   0.000   R21C70A.F0 to   R21C70A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)

                      1.163   (45.7% logic, 54.3% route), 15 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2960:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R23C68A.CLK clk_125_c
                    ----
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2944:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R21C70A.CLK clk_125_c
                    ----
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

==
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr*" 6.000000 ns ;
            33 items scored, 0 timing errors detected.

Passed: The following path meets requirements by 0.205ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT +)
                   FF   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM0

   Delay: 0.309ns (30.1% logic, 69.9% route), 2 logic levels.

 Constraint Details:

     0.309ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1390 meets
     0.104ns WAD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.104ns) by 0.205ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1390:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R37C59C.CLK to   R37C59C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE   12   0.216   R37C59C.Q0 to   R39C59C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL   ---   0.000   R39C59C.A0 to R39C59C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE   2   0.000 R39C59C.WADO0 to   R39C59A.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT)

                      0.309   (30.1% logic, 69.9% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R37C59C.CLK clk_125_c
                    ----
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1390:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R39C59C.CLK clk_125_c
ZERO_DEL   ---   0.000   R39C59C.CLK to   R39C59C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE   2   0.000   R39C59C.WCKO to   R39C59A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT

                      0.527   (0.0% logic, 100.0% route), 1 logic levels.

Passed: The following path meets requirements by 0.205ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT +)
                   FF   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1

   Delay: 0.309ns (30.1% logic, 69.9% route), 2 logic levels.

 Constraint Details:

     0.309ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391 meets
     0.104ns WAD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.104ns) by 0.205ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391:

```
   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R37C59C.CLK to     R37C59C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE        12     0.216     R37C59C.Q0 to     R39C59C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL    ---     0.000     R39C59C.A0 to  R39C59C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE         2     0.000  R39C59C.WADO0 to   R39C59B.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT)
                    --------
                     0.309   (30.1% logic, 69.9% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R37C59C.CLK clk_125_c
                    --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R39C59C.CLK clk_125_c
ZERO_DEL    ---     0.000    R39C59C.CLK to   R39C59C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE         2     0.000   R39C59C.WCKO to    R39C59B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT
                    --------
                     0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.213ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM0

   Delay:               0.317ns  (29.3% logic, 70.7% route), 2 logic levels.

 Constraint Details:

      0.317ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1382 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.213ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1382:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R37C59C.CLK to     R37C59C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE        12     0.224     R37C59C.Q0 to     R39C58C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL    ---     0.000     R39C58C.A0 to  R39C58C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1381
ROUTE         2     0.000  R39C58C.WADO0 to   R39C58A.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT)
                    --------
                     0.317   (29.3% logic, 70.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R37C59C.CLK clk_125_c
                    --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1382:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R39C58C.CLK clk_125_c
ZERO_DEL    ---     0.000    R39C58C.CLK to   R39C58C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1381
ROUTE         2     0.000   R39C58C.WCKO to    R39C58A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT
                    --------
                     0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.213ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM1

   Delay:               0.317ns  (29.3% logic, 70.7% route), 2 logic levels.

 Constraint Details:

      0.317ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1383 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.213ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1383:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R37C59C.CLK to     R37C59C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE        12     0.224     R37C59C.Q0 to     R39C58C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL    ---     0.000     R39C58C.A0 to  R39C58C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1381
ROUTE         2     0.000  R39C58C.WADO0 to   R39C58B.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT)
                    --------
                     0.317   (29.3% logic, 70.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R37C59C.CLK clk_125_c
                    --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1383:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R39C58C.CLK clk_125_c
ZERO_DEL    ---     0.000    R39C58C.CLK to   R39C58C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1381
ROUTE         2     0.000   R39C58C.WCKO to    R39C58B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT
                    --------
                     0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.230ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (to clk_125_c +)

   Delay:               0.219ns  (68.0% logic, 32.0% route), 2 logic levels.

 Constraint Details:

      0.219ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.230ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R37C59C.CLK to     R37C59C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE        12     0.070     R37C59C.Q0 to     R37C59C.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
CTOF_DEL    ---     0.056     R37C59C.C0 to     R37C59C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341
ROUTE         1     0.000     R37C59C.F0 to    R37C59C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_11_i (to clk_125_c)
                    --------
                     0.219   (68.0% logic, 32.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R37C59C.CLK clk_125_c
                    --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R37C59C.CLK clk_125_c
```

                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.263ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT +)
                   FF   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM0

   Delay: 0.367ns (25.3% logic, 74.7% route), 2 logic levels.

 Constraint Details:

      0.367ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1390 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.263ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1390:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R37C59C.CLK to   R37C59C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE   11   0.274   R37C59C.Q1 to   R39C59C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
ZERO_DEL   ---   0.000   R39C59C.B0 to R39C59C.WADO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE   2   0.000 R39C59C.WADO1 to   R39C59A.WAD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WAD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT)

                    0.367   (25.3% logic, 74.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R37C59C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1390:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R39C59C.CLK clk_125_c
ZERO_DEL   ---   0.000   R39C59C.CLK to   R39C59C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE   2   0.000   R39C59C.WCKO to   R39C59A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT

                    0.527   (0.0% logic, 100.0% route), 1 logic levels.

Passed: The following path meets requirements by 0.263ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT +)
                   FF   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1

   Delay: 0.367ns (25.3% logic, 74.7% route), 2 logic levels.

 Constraint Details:

      0.367ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.263ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R37C59C.CLK to   R37C59C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE   11   0.274   R37C59C.Q1 to   R39C59C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
ZERO_DEL   ---   0.000   R39C59C.B0 to R39C59C.WADO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE   2   0.000 R39C59C.WADO1 to   R39C59B.WAD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WAD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT)

                    0.367   (25.3% logic, 74.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R37C59C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R39C59C.CLK clk_125_c
ZERO_DEL   ---   0.000   R39C59C.CLK to   R39C59C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE   2   0.000   R39C59C.WCKO to   R39C59B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT

                    0.527   (0.0% logic, 100.0% route), 1 logic levels.

Passed: The following path meets requirements by 0.269ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0rff_2 (to clk_125_c +)

   Delay: 0.258ns (57.8% logic, 42.2% route), 2 logic levels.

 Constraint Details:

      0.258ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3340 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.269ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3340:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R37C59C.CLK to   R37C59C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE   12   0.109   R37C59C.Q0 to   R37C58C.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
CTOF_DEL   ---   0.056   R37C58C.C0 to   R37C58C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3340
ROUTE   1   0.000   R37C58C.F0 to   R37C58C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_33184_0 (to clk_125_c)

                    0.258   (57.8% logic, 42.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R37C59C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3340:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R37C58C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.274ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1] (to clk_125_c +)

   Delay: 0.263ns (56.7% logic, 43.3% route), 2 logic levels.

 Constraint Details:

      0.263ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.274ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

```
   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R37C59C.CLK to     R37C59C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE        11     0.114     R37C59C.Q1 to     R37C59C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
CTOF_DEL    ---     0.056     R37C59C.A1 to     R37C59C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341
ROUTE         1     0.000     R37C59C.F1 to    R37C59C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_3290_i (to clk_125_c)
                  --------
                    0.263   (56.7% logic, 43.3% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R37C59C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R37C59C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.314ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]  (to clk_125_c +)

   Delay:               0.303ns  (49.2% logic, 50.8% route), 2 logic levels.

 Constraint Details:

      0.303ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.314ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R37C59C.CLK to     R37C59C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341 (from clk_125_c)
ROUTE        12     0.154     R37C59C.Q0 to     R37C59C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
CTOF_DEL    ---     0.056     R37C59C.B1 to     R37C59C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341
ROUTE         1     0.000     R37C59C.F1 to    R37C59C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_3290_i (to clk_125_c)
                  --------
                    0.303   (49.2% logic, 50.8% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R37C59C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3341:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R37C59C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Report:    0.219ns is the minimum delay for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr*" 6.000000 ns ;
            147 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.202ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (to clk_125_c +)

   Delay:               0.191ns  (78.0% logic, 22.0% route), 2 logic levels.

 Constraint Details:

      0.191ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.202ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R21C52B.CLK to     R21C52B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE        30     0.042     R21C52B.Q0 to     R21C52B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL    ---     0.056     R21C52B.D0 to     R21C52B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309
ROUTE         1     0.000     R21C52B.F0 to    R21C52B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/N_9_i (to clk_125_c)
                  --------
                    0.191   (78.0% logic, 22.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.266ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (to clk_125_c +)

   Delay:               0.255ns  (58.4% logic, 41.6% route), 2 logic levels.

 Constraint Details:

      0.255ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.266ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R21C52B.CLK to     R21C52B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE        29     0.106     R21C52B.Q1 to     R21C52B.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL    ---     0.056     R21C52B.C1 to     R21C52B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309
ROUTE         1     0.000     R21C52B.F1 to    R21C52B.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/N_3295_i (to clk_125_c)
                  --------
                    0.255   (58.4% logic, 41.6% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
```

```
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.312ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (to clk_125_c +)

   Delay:               0.301ns  (49.5% logic, 50.5% route), 2 logic levels.

 Constraint Details:

      0.301ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.312ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R21C52B.CLK to     R21C52B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE        30     0.152     R21C52B.Q0 to     R21C52B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL    ---     0.056     R21C52B.B1 to     R21C52B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309
ROUTE         1     0.000     R21C52B.F1 to    R21C52B.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/N_3295_i (to clk_125_c)
                  --------
                    0.301   (49.5% logic, 50.5% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.640ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[1]  (to clk_125_c +)

   Delay:               0.629ns  (32.6% logic, 67.4% route), 3 logic levels.

 Constraint Details:

      0.629ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.640ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R21C52B.CLK to     R21C52B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE        30     0.341     R21C52B.Q0 to     R15C58A.D1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL    ---     0.056     R15C58A.D1 to     R15C58A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2791
ROUTE        12     0.083     R15C58A.F1 to     R15C59A.D1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0ror_0
CTOF_DEL    ---     0.056     R15C59A.D1 to     R15C59A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754
ROUTE         1     0.000     R15C59A.F1 to    R15C59A.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[1] (to clk_125_c)
                  --------
                    0.629   (32.6% logic, 67.4% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R15C59A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.640ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[0]  (to clk_125_c +)

   Delay:               0.629ns  (32.6% logic, 67.4% route), 3 logic levels.

 Constraint Details:

      0.629ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.640ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R21C52B.CLK to     R21C52B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE        30     0.341     R21C52B.Q0 to     R15C58A.D1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL    ---     0.056     R15C58A.D1 to     R15C58A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2791
ROUTE        12     0.083     R15C58A.F1 to     R15C59A.D0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0ror_0
CTOF_DEL    ---     0.056     R15C59A.D0 to     R15C59A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754
ROUTE         1     0.000     R15C59A.F0 to    R15C59A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[0] (to clk_125_c)
                  --------
                    0.629   (32.6% logic, 67.4% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R15C59A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.640ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[12]  (to clk_125_c +)

   Delay:               0.629ns  (32.6% logic, 67.4% route), 3 logic levels.

 Constraint Details:

      0.629ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2761 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.640ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2761:
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```
   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R21C52B.CLK to     R21C52B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE        30     0.341     R21C52B.Q0 to     R15C58A.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL    ---     0.056     R15C58A.D1 to     R15C58A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2791
ROUTE        12     0.083     R15C58A.F1 to     R15C59B.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0ror_0
CTOF_DEL    ---     0.056     R15C59B.D1 to     R15C59B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2761
ROUTE         1     0.000     R15C59B.F1 to    R15C59B.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[12] (to clk_125_c)
                  --------
                    0.629   (32.6% logic, 67.4% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2761:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R15C59B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.649ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[12]  (to clk_125_c +)

   Delay:               0.638ns  (32.1% logic, 67.9% route), 3 logic levels.

 Constraint Details:

      0.638ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2761 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.649ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2761:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R21C52B.CLK to     R21C52B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE        29     0.362     R21C52B.Q1 to     R15C59D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL    ---     0.056     R15C59D.B0 to     R15C59D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_8273
ROUTE        12     0.071     R15C59D.F0 to     R15C59B.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0ror_1
CTOF_DEL    ---     0.056     R15C59B.C1 to     R15C59B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2761
ROUTE         1     0.000     R15C59B.F1 to    R15C59B.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[12] (to clk_125_c)
                  --------
                    0.638   (32.1% logic, 67.9% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2761:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R15C59B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.649ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[1]  (to clk_125_c +)

   Delay:               0.638ns  (32.1% logic, 67.9% route), 3 logic levels.

 Constraint Details:

      0.638ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.649ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R21C52B.CLK to     R21C52B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE        29     0.362     R21C52B.Q1 to     R15C59D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL    ---     0.056     R15C59D.B0 to     R15C59D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_8273
ROUTE        12     0.071     R15C59D.F0 to     R15C59A.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0ror_1
CTOF_DEL    ---     0.056     R15C59A.C1 to     R15C59A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754
ROUTE         1     0.000     R15C59A.F1 to    R15C59A.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[1] (to clk_125_c)
                  --------
                    0.638   (32.1% logic, 67.9% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R15C59A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.649ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[0]  (to clk_125_c +)

   Delay:               0.638ns  (32.1% logic, 67.9% route), 3 logic levels.

 Constraint Details:

      0.638ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.649ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R21C52B.CLK to     R21C52B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE        29     0.362     R21C52B.Q1 to     R15C59D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL    ---     0.056     R15C59D.B0 to     R15C59D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_8273
ROUTE        12     0.071     R15C59D.F0 to     R15C59A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0ror_1
CTOF_DEL    ---     0.056     R15C59A.C0 to     R15C59A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754
ROUTE         1     0.000     R15C59A.F0 to    R15C59A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[0] (to clk_125_c)
                  --------
                    0.638   (32.1% logic, 67.9% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2754:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R15C59A.CLK clk_125_c
```

```
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.666ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[9]  (to clk_125_c +)

   Delay:               0.655ns  (31.3% logic, 68.7% route), 3 logic levels.

 Constraint Details:

      0.655ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2759 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.666ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2759:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R21C52B.CLK to     R21C52B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309 (from clk_125_c)
ROUTE        29     0.362     R21C52B.Q1 to     R15C59D.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL    ---     0.056     R15C59D.B1 to     R15C59D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_8273
ROUTE        12     0.088     R15C59D.F1 to     R15C58B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1ror_1
CTOF_DEL    ---     0.056     R15C58B.D0 to     R15C58B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2759
ROUTE         1     0.000     R15C58B.F0 to    R15C58B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[9] (to clk_125_c)
                  --------
                    0.655   (31.3% logic, 68.7% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3309:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R21C52B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2759:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R15C58B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Report:    0.191ns is the minimum delay for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr*" 6.000000 ns ;
            14 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.200ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]  (to clk_125_c +)

   Delay:               0.189ns  (78.8% logic, 21.2% route), 2 logic levels.

 Constraint Details:

      0.189ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.200ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R10C66B.CLK to     R10C66B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 (from clk_125_c)
ROUTE         5     0.040     R10C66B.Q0 to     R10C66B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]
CTOF_DEL    ---     0.056     R10C66B.D0 to     R10C66B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208
ROUTE         1     0.000     R10C66B.F0 to    R10C66B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_e0 (to clk_125_c)
                  --------
                    0.189   (78.8% logic, 21.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R10C66B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R10C66B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.246ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_eidle_tx  (to clk_125_c +)

   Delay:               0.235ns  (63.4% logic, 36.6% route), 2 logic levels.

 Constraint Details:

      0.235ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.246ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R11C66B.CLK to     R11C66B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210 (from clk_125_c)
ROUTE         2     0.086     R11C66B.Q0 to     R12C66A.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]
CTOF_DEL    ---     0.056     R12C66A.D0 to     R12C66A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0
ROUTE         1     0.000     R12C66A.F0 to    R12C66A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/ltssm_eidle_tx (to clk_125_c)
                  --------
                    0.235   (63.4% logic, 36.6% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R11C66B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R12C66A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.266ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]  (to clk_125_c +)

   Delay:               0.255ns  (58.4% logic, 41.6% route), 2 logic levels.

 Constraint Details:

      0.255ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.266ns
```

```
 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R11C66C.CLK to     R11C66C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 (from clk_125_c)
ROUTE         3     0.106     R11C66C.Q1 to     R11C66B.C0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]
CTOF_DEL    ---     0.056     R11C66B.C0 to     R11C66B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210
ROUTE         1     0.000     R11C66B.F0 to    R11C66B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n3 (to clk_125_c)
                  --------
                    0.255   (58.4% logic, 41.6% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R11C66C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R11C66B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.273ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]  (to clk_125_c +)

   Delay:               0.262ns  (56.9% logic, 43.1% route), 2 logic levels.

 Constraint Details:

      0.262ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.273ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R11C66C.CLK to     R11C66C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 (from clk_125_c)
ROUTE         3     0.113     R11C66C.Q1 to     R11C66C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]
CTOF_DEL    ---     0.056     R11C66C.A1 to     R11C66C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209
ROUTE         1     0.000     R11C66C.F1 to    R11C66C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n2 (to clk_125_c)
                  --------
                    0.262   (56.9% logic, 43.1% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R11C66C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R11C66C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.275ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]  (to clk_125_c +)

   Delay:               0.264ns  (56.4% logic, 43.6% route), 2 logic levels.

 Constraint Details:

      0.264ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.275ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R10C66B.CLK to     R10C66B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 (from clk_125_c)
ROUTE         5     0.115     R10C66B.Q0 to     R11C66B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]
CTOF_DEL    ---     0.056     R11C66B.D0 to     R11C66B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210
ROUTE         1     0.000     R11C66B.F0 to    R11C66B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n3 (to clk_125_c)
                  --------
                    0.264   (56.4% logic, 43.6% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R10C66B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R11C66B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.303ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]  (to clk_125_c +)

   Delay:               0.292ns  (51.0% logic, 49.0% route), 2 logic levels.

 Constraint Details:

      0.292ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.303ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R10C66B.CLK to     R10C66B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 (from clk_125_c)
ROUTE         5     0.143     R10C66B.Q0 to     R11C66C.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]
CTOF_DEL    ---     0.056     R11C66C.C0 to     R11C66C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209
ROUTE         1     0.000     R11C66C.F0 to    R11C66C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n1 (to clk_125_c)
                  --------
                    0.292   (51.0% logic, 49.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R10C66B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R11C66C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.
```

Passed: The following path meets requirements by 0.303ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2] (to clk_125_c +)

   Delay: 0.292ns (51.0% logic, 49.0% route), 2 logic levels.

 Constraint Details:

      0.292ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.303ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R10C66B.CLK to   R10C66B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208 (from clk_125_c)
ROUTE   5   0.143   R10C66B.Q0 to   R11C66C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]
CTOF_DEL   ---   0.056   R11C66C.C1 to   R11C66C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209
ROUTE   1   0.000   R11C66C.F1 to   R11C66C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n2 (to clk_125_c)

                    0.292   (51.0% logic, 49.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3208:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R10C66B.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R11C66C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.310ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1] (to clk_125_c +)

   Delay: 0.299ns (49.8% logic, 50.2% route), 2 logic levels.

 Constraint Details:

      0.299ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.310ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R11C66C.CLK to   R11C66C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 (from clk_125_c)
ROUTE   4   0.150   R11C66C.Q0 to   R11C66C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]
CTOF_DEL   ---   0.056   R11C66C.A0 to   R11C66C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209
ROUTE   1   0.000   R11C66C.F0 to   R11C66C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n1 (to clk_125_c)

                    0.299   (49.8% logic, 50.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R11C66C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R11C66C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.311ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3] (to clk_125_c +)

   Delay: 0.300ns (49.7% logic, 50.3% route), 2 logic levels.

 Constraint Details:

      0.300ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.311ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R11C66C.CLK to   R11C66C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 (from clk_125_c)
ROUTE   4   0.151   R11C66C.Q0 to   R11C66B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]
CTOF_DEL   ---   0.056   R11C66B.B0 to   R11C66B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210
ROUTE   1   0.000   R11C66B.F0 to   R11C66B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n3 (to clk_125_c)

                    0.300   (49.7% logic, 50.3% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R11C66C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3210:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R11C66B.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.313ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2] (to clk_125_c +)

   Delay: 0.302ns (49.3% logic, 50.7% route), 2 logic levels.

 Constraint Details:

      0.302ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.313ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R11C66C.CLK to   R11C66C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209 (from clk_125_c)
ROUTE   4   0.153   R11C66C.Q0 to   R11C66C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]
CTOF_DEL   ---   0.056   R11C66C.B1 to   R11C66C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209
ROUTE   1   0.000   R11C66C.F1 to   R11C66C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n2 (to clk_125_c)

                    0.302   (49.3% logic, 50.7% route), 2 logic levels.

```
 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R11C66C.CLK clk_125_c
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3209:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R11C66C.CLK clk_125_c
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

Report:    0.189ns is the minimum delay for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr*" 6.000000 ns ;
            18 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.191ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT +)

   Delay:               0.295ns  (31.5% logic, 68.5% route), 2 logic levels.

 Constraint Details:

      0.295ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.191ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R11C67C.CLK to     R11C67C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 (from clk_125_c)
ROUTE         4     0.202     R11C67C.Q0 to     R12C66C.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]
ZERO_DEL    ---     0.000     R12C66C.C0 to  R12C66C.WADO2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         1     0.000  R12C66C.WADO2 to   R12C66A.WAD2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WAD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT)
                    --------
                      0.295   (31.5% logic, 68.5% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R11C67C.CLK clk_125_c
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R12C66C.CLK clk_125_c
ZERO_DEL    ---     0.000    R12C66C.CLK to   R12C66C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         2     0.000   R12C66C.WCKO to    R12C66A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT
                    --------
                      0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.195ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT +)

   Delay:               0.299ns  (31.1% logic, 68.9% route), 2 logic levels.

 Constraint Details:

      0.299ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.195ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R11C67C.CLK to     R11C67C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 (from clk_125_c)
ROUTE         3     0.206     R11C67C.Q1 to     R12C66C.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]
ZERO_DEL    ---     0.000     R12C66C.D0 to  R12C66C.WADO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         1     0.000  R12C66C.WADO3 to   R12C66A.WAD3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WAD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT)
                    --------
                      0.299   (31.1% logic, 68.9% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R11C67C.CLK clk_125_c
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R12C66C.CLK clk_125_c
ZERO_DEL    ---     0.000    R12C66C.CLK to   R12C66C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         2     0.000   R12C66C.WCKO to    R12C66A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT
                    --------
                      0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.202ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]  (to clk_125_c +)

   Delay:               0.191ns  (78.0% logic, 22.0% route), 2 logic levels.

 Constraint Details:

      0.191ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.202ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R11C67B.CLK to     R11C67B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 (from clk_125_c)
ROUTE         6     0.042     R11C67B.Q0 to     R11C67B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]
CTOF_DEL    ---     0.056     R11C67B.D0 to     R11C67B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235
ROUTE         1     0.000     R11C67B.F0 to    R11C67B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_i[0] (to clk_125_c)
                    --------
                      0.191   (78.0% logic, 22.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R11C67B.CLK clk_125_c
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R11C67B.CLK clk_125_c
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.
```

Passed: The following path meets requirements by 0.230ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2] (to clk_125_c +)

   Delay: 0.219ns (68.0% logic, 32.0% route), 2 logic levels.

 Constraint Details:

      0.219ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.230ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R11C67C.CLK to   R11C67C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 (from clk_125_c)
ROUTE   4   0.070   R11C67C.Q0 to   R11C67C.C0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]
CTOF_DEL   ---   0.056   R11C67C.C0 to   R11C67C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236
ROUTE   1   0.000   R11C67C.F0 to   R11C67C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[2] (to clk_125_c)

                    0.219   (68.0% logic, 32.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R11C67C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R11C67C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.241ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1] (to clk_125_c +)

   Delay: 0.230ns (64.8% logic, 35.2% route), 2 logic levels.

 Constraint Details:

      0.230ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.241ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R11C67B.CLK to   R11C67B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 (from clk_125_c)
ROUTE   6   0.081   R11C67B.Q0 to   R11C67B.D1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]
CTOF_DEL   ---   0.056   R11C67B.D1 to   R11C67B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235
ROUTE   1   0.000   R11C67B.F1 to   R11C67B.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[1] (to clk_125_c)

                    0.230   (64.8% logic, 35.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R11C67B.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R11C67B.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.241ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2] (to clk_125_c +)

   Delay: 0.230ns (64.8% logic, 35.2% route), 2 logic levels.

 Constraint Details:

      0.230ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.241ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R11C67B.CLK to   R11C67B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 (from clk_125_c)
ROUTE   6   0.081   R11C67B.Q0 to   R11C67C.D0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]
CTOF_DEL   ---   0.056   R11C67C.D0 to   R11C67C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236
ROUTE   1   0.000   R11C67C.F0 to   R11C67C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[2] (to clk_125_c)

                    0.230   (64.8% logic, 35.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R11C67B.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R11C67C.CLK clk_125_c
                  ----
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Passed: The following path meets requirements by 0.260ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3] (to clk_125_c +)

   Delay: 0.249ns (59.8% logic, 40.2% route), 2 logic levels.

 Constraint Details:

      0.249ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.260ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R11C67C.CLK to   R11C67C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236 (from clk_125_c)
ROUTE   4   0.100   R11C67C.Q0 to   R11C67C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]
CTOF_DEL   ---   0.056   R11C67C.D1 to   R11C67C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236
ROUTE   1   0.000   R11C67C.F1 to   R11C67C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[3] (to clk_125_c)

                    0.249   (59.8% logic, 40.2% route), 2 logic levels.

 Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527 *FF_TX_H_CLK_0 to	R11C67C.CLK	clk_125_c
		0.527 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3236:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527 *FF_TX_H_CLK_0 to	R11C67C.CLK	clk_125_c
		0.527 (0.0% logic, 100.0% route), 0 logic levels.		

Passed: The following path meets requirements by 0.261ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT +)

Delay: 0.365ns (25.5% logic, 74.5% route), 2 logic levels.

Constraint Details:

0.365ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
0.104ns WAD_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling 0.104ns) by 0.261ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R11C67B.CLK to	R11C67B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 (from clk_125_c)
ROUTE	6	0.272	R11C67B.Q0 to	R12C66C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]
ZERO_DEL	---	0.000	R12C66C.A0 to	R12C66C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE	1	0.000	R12C66C.WADO0 to	R12C66A.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT)
		0.365 (25.5% logic, 74.5% route), 2 logic levels.		

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527 *FF_TX_H_CLK_0 to	R11C67B.CLK	clk_125_c
		0.527 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527 *FF_TX_H_CLK_0 to	R12C66C.CLK	clk_125_c
ZERO_DEL	---	0.000	R12C66C.CLK to	R12C66C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE	2	0.000	R12C66C.WCKO to	R12C66A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT
		0.527 (0.0% logic, 100.0% route), 1 logic levels.		

Passed: The following path meets requirements by 0.262ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT +)

Delay: 0.366ns (25.4% logic, 74.6% route), 2 logic levels.

Constraint Details:

0.366ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
0.104ns WAD_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling 0.104ns) by 0.262ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R11C67B.CLK to	R11C67B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 (from clk_125_c)
ROUTE	5	0.273	R11C67B.Q1 to	R12C66C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]
ZERO_DEL	---	0.000	R12C66C.B0 to	R12C66C.WADO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE	1	0.000	R12C66C.WADO1 to	R12C66A.WAD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WAD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT)
		0.366 (25.4% logic, 74.6% route), 2 logic levels.		

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527 *FF_TX_H_CLK_0 to	R11C67B.CLK	clk_125_c
		0.527 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527 *FF_TX_H_CLK_0 to	R12C66C.CLK	clk_125_c
ZERO_DEL	---	0.000	R12C66C.CLK to	R12C66C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE	2	0.000	R12C66C.WCKO to	R12C66A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT
		0.527 (0.0% logic, 100.0% route), 1 logic levels.		

Passed: The following path meets requirements by 0.273ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1] (to clk_125_c +)

Delay: 0.262ns (56.9% logic, 43.1% route), 2 logic levels.

Constraint Details:

0.262ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 meets
-0.011ns DIN_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.011ns) by 0.273ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R11C67B.CLK to	R11C67B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235 (from clk_125_c)
ROUTE	5	0.113	R11C67B.Q1 to	R11C67B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]
CTOF_DEL	---	0.056	R11C67B.B1 to	R11C67B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235
ROUTE	1	0.000	R11C67B.F1 to	R11C67B.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[1] (to clk_125_c)
		0.262 (56.9% logic, 43.1% route), 2 logic levels.		

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527 *FF_TX_H_CLK_0 to	R11C67B.CLK	clk_125_c
		0.527 (0.0% logic, 100.0% route), 0 logic levels.		

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3235:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527 *FF_TX_H_CLK_0 to	R11C67B.CLK	clk_125_c
		0.527 (0.0% logic, 100.0% route), 0 logic levels.		

Report: 0.191ns is the minimum delay for this preference.

==
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data*" 6.000000 ns ;
16 items scored, 0 timing errors detected.

Passed: The following path meets requirements by 0.330ns

```
 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[11]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM1

   Delay:               0.392ns  (38.0% logic, 62.0% route), 3 logic levels.

 Constraint Details:

      0.392ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2769 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1386 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.330ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2769 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1386:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R34C59A.CLK to     R34C59A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2769 (from clk_125_c)
ROUTE         1     0.103     R34C59A.Q1 to     R34C59B.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[11]
CTOF_DEL    ---     0.056     R34C59B.C0 to     R34C59B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9491
ROUTE         1     0.140     R34C59B.F0 to     R34C61C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_212
ZERO_DEL    ---     0.000     R34C61C.D1 to   R34C61C.WDO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE         1     0.000   R34C61C.WDO3 to    R34C61B.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT)
                  --------
                    0.392   (38.0% logic, 62.0% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2769:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R34C59A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1386:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R34C61C.CLK clk_125_c
ZERO_DEL    ---     0.000    R34C61C.CLK to   R34C61C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE         2     0.000   R34C61C.WCKO to    R34C61B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.357ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[2]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1

   Delay:               0.419ns  (35.6% logic, 64.4% route), 3 logic levels.

 Constraint Details:

      0.419ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2765 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1394 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.357ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2765 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1394:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R36C61A.CLK to     R36C61A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2765 (from clk_125_c)
ROUTE         1     0.204     R36C61A.Q0 to     R34C62D.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[2]
CTOF_DEL    ---     0.056     R34C62D.C0 to     R34C62D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9500
ROUTE         1     0.066     R34C62D.F0 to     R34C62C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_203
ZERO_DEL    ---     0.000     R34C62C.C1 to   R34C62C.WDO2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE         1     0.000   R34C62C.WDO2 to    R34C62B.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
                  --------
                    0.419   (35.6% logic, 64.4% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2765:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R36C61A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1394:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R34C62C.CLK clk_125_c
ZERO_DEL    ---     0.000    R34C62C.CLK to   R34C62C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE         2     0.000   R34C62C.WCKO to    R34C62B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.375ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[10]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM1

   Delay:               0.437ns  (34.1% logic, 65.9% route), 3 logic levels.

 Constraint Details:

      0.437ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2769 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1386 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.375ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2769 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1386:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R34C59A.CLK to     R34C59A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2769 (from clk_125_c)
ROUTE         1     0.222     R34C59A.Q0 to     R34C61D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[10]
CTOF_DEL    ---     0.056     R34C61D.B0 to     R34C61D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9492
ROUTE         1     0.066     R34C61D.F0 to     R34C61C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_211
ZERO_DEL    ---     0.000     R34C61C.C1 to   R34C61C.WDO2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE         1     0.000   R34C61C.WDO2 to    R34C61B.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT)
                  --------
                    0.437   (34.1% logic, 65.9% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2769:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R34C59A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1386:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R34C61C.CLK clk_125_c
ZERO_DEL    ---     0.000    R34C61C.CLK to   R34C61C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE         2     0.000   R34C61C.WCKO to    R34C61B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.389ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[3]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1

   Delay:               0.451ns  (33.0% logic, 67.0% route), 3 logic levels.

 Constraint Details:

      0.451ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2765 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1394 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
```

0.000ns skew requirement (totaling 0.062ns) by 0.389ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2765 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1394:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R36C61A.CLK to	R36C61A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2765 (from clk_125_c)
ROUTE	1	0.148	R36C61A.Q1 to	R36C62D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[3]
CTOF_DEL	---	0.056	R36C62D.B0 to	R36C62D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9499
ROUTE	1	0.154	R36C62D.F0 to	R34C62C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m_i_m2[3]
ZERO_DEL	---	0.000	R34C62C.D1 to	R34C62C.WDO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE	1	0.000	R34C62C.WDO3 to	R34C62B.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
		0.451	(33.0% logic, 67.0% route), 3 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2765:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527	*FF_TX_H_CLK_0 to	R36C61A.CLK clk_125_c
		0.527	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1394:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527	*FF_TX_H_CLK_0 to	R34C62C.CLK clk_125_c
ZERO_DEL	---	0.000	R34C62C.CLK to	R34C62C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1392
ROUTE	2	0.000	R34C62C.WCKO to	R34C62B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
		0.527	(0.0% logic, 100.0% route), 1 logic levels.	

Passed: The following path meets requirements by 0.425ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source:	FF	Q	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[7] (from clk_125_c +)
Destination:	FF	Data in	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT +)
	FF		pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1

Delay: 0.487ns (30.6% logic, 69.4% route), 3 logic levels.

Constraint Details:

0.487ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2767 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391 meets
0.062ns WD_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling 0.062ns) by 0.425ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2767 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R36C59A.CLK to	R36C59A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2767 (from clk_125_c)
ROUTE	1	0.242	R36C59A.Q1 to	R39C59D.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[7]
CTOF_DEL	---	0.056	R39C59D.A0 to	R39C59D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9495
ROUTE	1	0.096	R39C59D.F0 to	R39C59C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_208
ZERO_DEL	---	0.000	R39C59C.D1 to	R39C59C.WDO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE	1	0.000	R39C59C.WDO3 to	R39C59B.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT)
		0.487	(30.6% logic, 69.4% route), 3 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2767:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527	*FF_TX_H_CLK_0 to	R36C59A.CLK clk_125_c
		0.527	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527	*FF_TX_H_CLK_0 to	R39C59C.CLK clk_125_c
ZERO_DEL	---	0.000	R39C59C.CLK to	R39C59C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE	2	0.000	R39C59C.WCKO to	R39C59B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT
		0.527	(0.0% logic, 100.0% route), 1 logic levels.	

Passed: The following path meets requirements by 0.432ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source:	FF	Q	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[4] (from clk_125_c +)
Destination:	FF	Data in	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT +)
	FF		pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM0

Delay: 0.494ns (30.2% logic, 69.8% route), 3 logic levels.

Constraint Details:

0.494ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2766 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1390 meets
0.062ns WD_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling 0.062ns) by 0.432ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2766 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1390:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R36C60B.CLK to	R36C60B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2766 (from clk_125_c)
ROUTE	1	0.198	R36C60B.Q0 to	R39C60D.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[4]
CTOF_DEL	---	0.056	R39C60D.C0 to	R39C60D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9498
ROUTE	1	0.147	R39C60D.F0 to	R39C59C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_205
ZERO_DEL	---	0.000	R39C59C.A1 to	R39C59C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE	1	0.000	R39C59C.WDO0 to	R39C59A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT)
		0.494	(30.2% logic, 69.8% route), 3 logic levels.	

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2766:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527	*FF_TX_H_CLK_0 to	R36C60B.CLK clk_125_c
		0.527	(0.0% logic, 100.0% route), 0 logic levels.	

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1390:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	999	0.527	*FF_TX_H_CLK_0 to	R39C59C.CLK clk_125_c
ZERO_DEL	---	0.000	R39C59C.CLK to	R39C59C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE	2	0.000	R39C59C.WCKO to	R39C59A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT
		0.527	(0.0% logic, 100.0% route), 1 logic levels.	

Passed: The following path meets requirements by 0.443ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source:	FF	Q	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[6] (from clk_125_c +)
Destination:	FF	Data in	pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT +)
	FF		pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1

Delay: 0.505ns (29.5% logic, 70.5% route), 3 logic levels.

Constraint Details:

0.505ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2767 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391 meets
0.062ns WD_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling 0.062ns) by 0.443ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2767 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.093	R36C59A.CLK to	R36C59A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2767 (from clk_125_c)
ROUTE	1	0.168	R36C59A.Q0 to	R38C59D.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[6]
CTOF_DEL	---	0.056	R38C59D.C0 to	R38C59D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9496
ROUTE	1	0.188	R38C59D.F0 to	R39C59C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_207
ZERO_DEL	---	0.000	R39C59C.C1 to	R39C59C.WDO2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE	1	0.000	R39C59C.WDO2 to	R39C59B.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT)

                    0.505   (29.5% logic, 70.5% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2767:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R36C59A.CLK clk_125_c
                    ----
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1391:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R39C59C.CLK clk_125_c
ZERO_DEL   ---   0.000   R39C59C.CLK to   R39C59C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1389
ROUTE   2   0.000   R39C59C.WCKO to   R39C59B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT

                      0.527   (0.0% logic, 100.0% route), 1 logic levels.

Passed: The following path meets requirements by 0.464ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[8] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT +)
                   FF   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0

   Delay: 0.526ns (28.3% logic, 71.7% route), 3 logic levels.

 Constraint Details:

      0.526ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.464ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R36C60C.CLK to   R36C60C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768 (from clk_125_c)
ROUTE   1   0.075   R36C60C.Q0 to   R36C60A.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[8]
CTOF_DEL   ---   0.056   R36C60A.D0 to   R36C60A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9494
ROUTE   1   0.302   R36C60A.F0 to   R34C61C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m_i_m2[8]
ZERO_DEL   ---   0.000   R34C61C.A1 to   R34C61C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE   1   0.000   R34C61C.WDO0 to   R34C61A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT)

                      0.526   (28.3% logic, 71.7% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R36C60C.CLK clk_125_c
                    ----
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R34C61C.CLK clk_125_c
ZERO_DEL   ---   0.000   R34C61C.CLK to   R34C61C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE   2   0.000   R34C61C.WCKO to   R34C61A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT

                      0.527   (0.0% logic, 100.0% route), 1 logic levels.

Passed: The following path meets requirements by 0.474ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[9] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT +)
                   FF   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0

   Delay: 0.536ns (27.8% logic, 72.2% route), 3 logic levels.

 Constraint Details:

      0.536ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.474ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R36C60C.CLK to   R36C60C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768 (from clk_125_c)
ROUTE   1   0.154   R36C60C.Q1 to   R34C60D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[9]
CTOF_DEL   ---   0.056   R34C60D.D0 to   R34C60D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9493
ROUTE   1   0.233   R34C60D.F0 to   R34C61C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_210
ZERO_DEL   ---   0.000   R34C61C.B1 to   R34C61C.WDO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE   1   0.000   R34C61C.WDO1 to   R34C61A.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT)

                      0.536   (27.8% logic, 72.2% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2768:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R36C60C.CLK clk_125_c
                    ----
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1385:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R34C61C.CLK clk_125_c
ZERO_DEL   ---   0.000   R34C61C.CLK to   R34C61C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1384
ROUTE   2   0.000   R34C61C.WCKO to   R34C61A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT

                      0.527   (0.0% logic, 100.0% route), 1 logic levels.

Passed: The following path meets requirements by 0.475ns

 Logical Details: Cell type Pin type   Cell/ASIC name (clock net +/-)

   Source: FF   Q   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[14] (from clk_125_c +)
   Destination: FF   Data in   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM1 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT +)
                   FF   pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM1

   Delay: 0.537ns (27.7% logic, 72.3% route), 3 logic levels.

 Constraint Details:

      0.537ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2771 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1383 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.475ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2771 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1383:

   Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   ---   0.093   R32C59A.CLK to   R32C59A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2771 (from clk_125_c)
ROUTE   1   0.322   R32C59A.Q0 to   R39C58D.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[14]
CTOF_DEL   ---   0.056   R39C58D.A0 to   R39C58D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9488
ROUTE   1   0.066   R39C58D.F0 to   R39C58C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_215
ZERO_DEL   ---   0.000   R39C58C.C1 to   R39C58C.WDO2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1381
ROUTE   1   0.000   R39C58C.WDO2 to   R39C58B.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT)

                      0.537   (27.7% logic, 72.3% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2771:

   Name   Fanout   Delay (ns)   Site   Resource
ROUTE   999   0.527 *FF_TX_H_CLK_0 to   R32C59A.CLK clk_125_c
                    ----
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1383:

   Name   Fanout   Delay (ns)   Site   Resource

```
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R39C58C.CLK clk_125_c
ZERO_DEL    ---     0.000    R39C58C.CLK to   R39C58C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1381
ROUTE         2     0.000   R39C58C.WCKO to    R39C58B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.

Report:    0.392ns is the minimum delay for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl*" 6.000000 ns ;
            2 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.447ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/RAM0

   Delay:               0.509ns  (29.3% logic, 70.7% route), 3 logic levels.

 Constraint Details:

      0.509ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1388 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.447ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1388:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R32C59B.CLK to     R32C59B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773 (from clk_125_c)
ROUTE         1     0.213     R32C59B.Q0 to     R34C58D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_kcntl_16[0]
CTOF_DEL    ---     0.056     R34C58D.B0 to     R34C58D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9504
ROUTE         1     0.147     R34C58D.F0 to     R34C58C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_199
ZERO_DEL    ---     0.000     R34C58C.A1 to   R34C58C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1387
ROUTE         1     0.000   R34C58C.WDO0 to    R34C58A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT)
                  --------
                    0.509   (29.3% logic, 70.7% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R32C59B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1388:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R34C58C.CLK clk_125_c
ZERO_DEL    ---     0.000    R34C58C.CLK to   R34C58C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1387
ROUTE         2     0.000   R34C58C.WCKO to    R34C58A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.685ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM0

   Delay:               0.747ns  (19.9% logic, 80.1% route), 3 logic levels.

 Constraint Details:

      0.747ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1379 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.685ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1379:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R32C59B.CLK to     R32C59B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773 (from clk_125_c)
ROUTE         1     0.346     R32C59B.Q1 to     R36C58D.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_kcntl_16[1]
CTOF_DEL    ---     0.056     R36C58D.C0 to     R36C58D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9503
ROUTE         1     0.252     R36C58D.F0 to     R39C57C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/N_200
ZERO_DEL    ---     0.000     R39C57C.A1 to   R39C57C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1378
ROUTE         1     0.000   R39C57C.WDO0 to    R39C57A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT)
                  --------
                    0.747   (19.9% logic, 80.1% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2773:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R32C59B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1379:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R39C57C.CLK clk_125_c
ZERO_DEL    ---     0.000    R39C57C.CLK to   R39C57C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1378
ROUTE         2     0.000   R39C57C.WCKO to    R39C57A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.

Report:    0.509ns is the minimum delay for this preference.
```

Report Summary

```
--------------
------------------------------------------------------------------------------
Preference(MIN Delays)                  |   Constraint|       Actual|Levels
------------------------------------------------------------------------------
                                        |             |             |
FREQUENCY NET "clk_125_c" 125.000000    |             |             |
MHz ;                                   |           -|           -|   1
                                        |             |             |
FREQUENCY NET "can_clk_c" 25.000000 MHz |             |             |
;                                       |           -|           -|   2
                                        |             |             |
FREQUENCY NET "uart_clk_c" 25.000000    |             |             |
MHz ;                                   |           -|           -|   2
                                        |             |             |
FREQUENCY NET "pcie/pclk" 250.000000    |             |             |
MHz ;                                   |           -|           -|   1
                                        |             |             |
FREQUENCY NET                           |             |             |
"pcie/u1_pcs_pipe/ff_rx_fclk_0"         |             |             |
250.000000 MHz ;                        |           -|           -|   1
                                        |             |             |
MULTICYCLE FROM CELL                    |             |             |
"*nfts_rx_skp_cnt*" TO CELL             |             |             |
"*cnt_done_nfts_rx*" 2.000000 X ;       |           -|           -|  11
                                        |             |             |
MULTICYCLE FROM CELL                    |             |             |
"*nfts_rx_skp_cnt*" TO CELL             |             |             |
"*ltssm_nfts_rx_skp*" 2.000000 X ;      |           -|           -|   8
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr|             |             |
*" 6.000000 ns ;                        |     0.000 ns|     0.219 ns|   2
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr|             |             |
*" 6.000000 ns ;                        |     0.000 ns|     0.191 ns|   2
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr|             |             |
*" 6.000000 ns ;                        |     0.000 ns|     0.189 ns|   2
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr|             |             |
*" 6.000000 ns ;                        |     0.000 ns|     0.191 ns|   2
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_da|             |             |
```

```
ta*" 6.000000 ns ;                      |     0.000 ns|     0.392 ns|   3
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kc|             |             |
ntl*" 6.000000 ns ;                     |     0.000 ns|     0.509 ns|   3
                                        |             |             |
--------------------------------------------------------------------------------


All preferences were met.
```

Clock Domains Analysis

```
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Found 8 clocks:

Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0   Loads: 3188
   Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl*" 6.000000 ns ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data*" 6.000000 ns ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr*" 6.000000 ns ;
   Covered under: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*cnt_done_nfts_rx*" 2.000000 X ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr*" 6.000000 ns ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr*" 6.000000 ns ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr*" 6.000000 ns ;
   Covered under: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*ltssm_nfts_rx_skp*" 2.000000 X ;

   Data transfers from:
   Clock Domain: can_clk_c   Source: pll_can/PLLInst_0.CLKOP
      Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ;   Transfers: 10

   Clock Domain: uart_clk_c   Source: pll_uarts/PLLInst_0.CLKOP
      Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ;   Transfers: 60

   Clock Domain: pcie/pclk   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_F_CLK_0
      Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ;   Transfers: 37

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: can_clk_c   Source: pll_can/PLLInst_0.CLKOP   Loads: 404
   Covered under: FREQUENCY NET "can_clk_c" 25.000000 MHz ;

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
      Covered under: FREQUENCY NET "can_clk_c" 25.000000 MHz ;   Transfers: 35

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: uart_clk_c   Source: pll_uarts/PLLInst_0.CLKOP   Loads: 1181
   Covered under: FREQUENCY NET "uart_clk_c" 25.000000 MHz ;

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
      Covered under: FREQUENCY NET "uart_clk_c" 25.000000 MHz ;   Transfers: 22

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: pcie/pclk   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_F_CLK_0   Loads: 192
   Covered under: FREQUENCY NET "pcie/pclk" 250.000000 MHz ;
   Blocked under: BLOCK PATH FROM CELL "*ctc_reset_chx*" ;

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
      Covered under: FREQUENCY NET "pcie/pclk" 250.000000 MHz ;   Transfers: 41

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: pcie/u1_pcs_pipe/ff_rx_fclk_0   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_RX_F_CLK_0   Loads: 1
   Covered under: FREQUENCY NET "pcie/u1_pcs_pipe/ff_rx_fclk_0" 250.000000 MHz ;

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
      Not reported because source and destination domains are unrelated.

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK   Loads: 416
   No transfer within this clock domain is found

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0

   Clock Domain: pcie/pclk   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_F_CLK_0

Clock Domain: ep5cht/rdcnt_inferred_clock_9   Source: ep5cht/SLICE_1095.Q0   Loads: 23
   No transfer within this clock domain is found

Clock Domain: ep5cht/lclk   Source: ep5cht/losc/SLICE_7941.F0   Loads: 10
   No transfer within this clock domain is found
```

Timing summary (Hold):

```
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Timing errors: 0  Score: 0
Cumulative negative slack: 0

Constraints cover 184537 paths, 104 nets, and 62958 connections (96.1% coverage)
```

Timing summary (Setup and Hold):

```
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Timing errors: 0 (setup), 0 (hold)
Score: 0 (setup), 0 (hold)
Cumulative negative slack: 0 (0+0)
--------------------------------------------------------------------------------

--------------------------------------------------------------------------------
```