19.2 Capture Mode

In Capture mode, the CCPRxH:CCPRxL register pair captures the 16-bit value of the Timer register selected in the CCPTMRS when an event occurs on the CCPx pin. An event is defined as one of the following:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

Note: For CCP2 only, the Capture mode can use the CCP2 input pin as the capture trigger for CCP2 or the input can function as a time-stamp through the CAN module. The CAN module provides the necessary control and trigger signals.

The event is selected by the mode select bits, CCPxM<3:0> (CCPxCON<3:0>). When a capture is made, the interrupt request flag bit, CCPxIF (PIR4<x>), is set; it must be cleared in software. If another capture occurs before the value in CCPRx is read, the old captured value is overwritten by the new captured value.

Figure 19-1 shows the Capture mode block diagram.

19.2.1 CCP PIN CONFIGURATION

In Capture mode, the appropriate CCPx pin should be configured as an input by setting the corresponding TRIS direction bit.

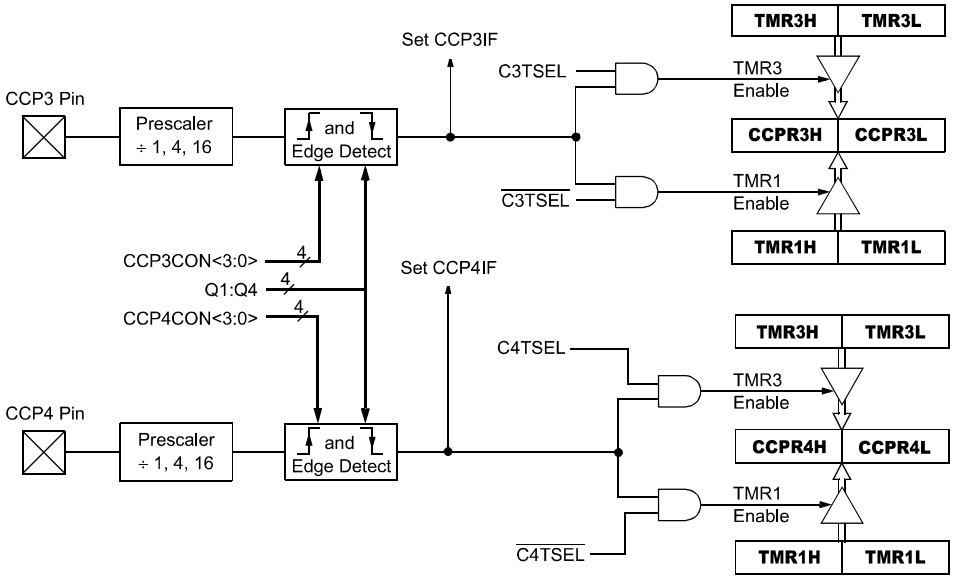
19.2.2 TIMER1/3 MODE SELECTION

For the available timers (1/3) to be used for the capture feature, the used timers must be running in Timer mode or Synchronized Counter mode. In Asynchronous Counter mode, the capture operation may not work.

The timer to be used with each CCP module is selected in the CCPTMRS register. (See **Section 19.1.1 "CCP Modules and Timer Resources"**.)

Details of the timer assignments for the CCP modules are given in Table 19-2.

FIGURE 19-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



Note: This block diagram uses CCP3 and CCP4, and their appropriate timers as an example. For details on all of the CCP modules and their timer assignments, see Table 19-2.