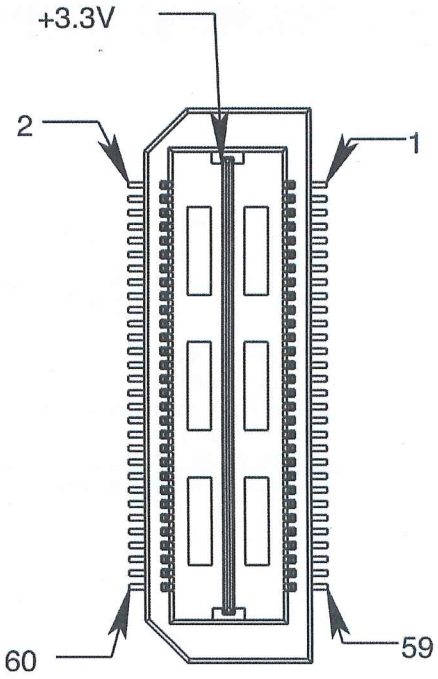
J1 – User I/O and Power



Connector J1 has 48 user definable I/O pins and 4 user definable FPGA global clocks.

The 48 user I/O pins can be setup as either 48 single-ended I/O signals or 24 LVDS differential pairs. The I/O signals are restricted to I/O standards that operate on the selected User I/O voltage. See Xilinx document DS202 for details. The 4 user clock signals are single-ended clock signals connected to the Xilinx Virtex-5 global clock resources.

The module 3.3V main power is provided via the center power plane. Additionally, the User I/O voltage (UIO_VCC) is provided either by the user design to the module, or the module to the user design depending on the configuration options chosen when ordering the module.

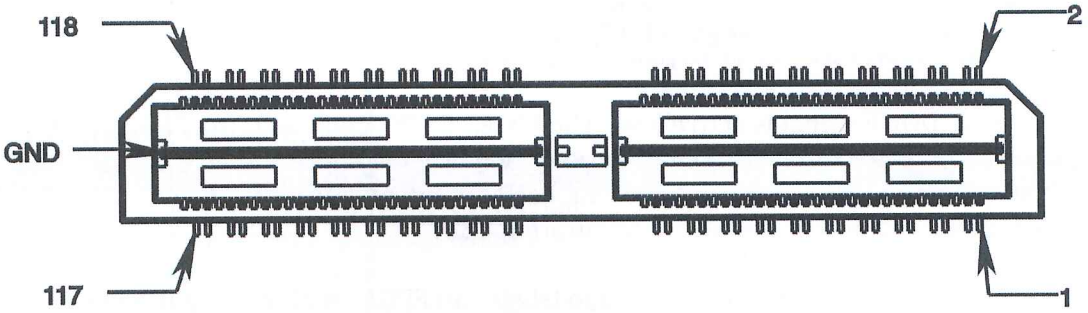
UIO_VREF is an optional reference voltage provided by the user design for HSTL and SSTL signaling.

Signal	FPGA Pin	Pin	Pin	FPGA Pin	Signal
USERIO_0P	H7	1	2	G21	USERIO_23N
USERIO_0N	G7	3	4	F20	USERIO_23P
USERIO_1P	F7	5	6	F10	USERIO_22N
USERIO_1N	F8	7	8	E10	USERIO_22P
USERIO_2P	F9	9	10	E21	USERIO_21N
USERIO_2N	G9	11	12	E20	USERIO_21P
USERIO_3P	H8	13	14	E11	USERIO_20N
USERIO_3N	J8	15	16	F12	USERIO_20P
UIO_VCC	-	17	18	-	UIO_VCC
UIO_VCC	-	19	20	-	UIO_VCC
USERCLK_0	D15	21	22	E18	USERCLK_3
USERCLK_1	E17	23	24	E13	USERCLK_2
UIO_VCC	-	25	26	-	UIO_VCC
UIO_VCC	-	27	28	D13(2)	USERIO_19N
USERIO_4P	E8	29	30	D14(1)	USERIO_19P
USERIO_4N	E7	31	32	E16	USERIO_18N
USERIO_5P	B9	33	34	D16	USERIO_18P
USERIO_5N	C8	35	36	D11	USERIO_17N
USERIO_6P	E6	37	38	C11	USERIO_17P
USERIO_6N	D6	39	40	E5	USERIO_16N
USERIO_7P	C9	41	42	D5	USERIO_16P

J2 – Multi-Gigabit SerDes I/O and Ground

Connector J2 on the MLX-1000-XC5V module contains Multi-Gigabit SerDes I/O, JTAG signals, configuration signals, and ground plane connection. There are 8 Multi-Gigabit SerDes transceivers on the Virtex-5 modules arranged in 4 pairs. Each pair contains two RX/TX differential pairs and a shared REFCLK differential pair.

Refer to Xilinx documents DS202, UG196 and UG198 for electrical specifications and capabilities of Xilinx Virtex-5 GTP and GTX transceiver pairs.



J2 as viewed from bottom of the module.

Signal	FPGA Pin	Pin	Pin	FPGA Pin	Signal
SERDESPAIR0_TXP0	H2	1	2	P2	SERDESPAIR1_TXP0
SERDESPAIR0_TXN0	J2	3	4	R2	SERDESPAIR1_TXN0
SERDESPAIR0_REFCLKP0	K4	7	8	T4	SERDESPAIR1_REFCLKP0
SERDESPAIR0_REFCLKN0	K3	9	10	T3	SERDESPAIR1_REFCLKN0
SERDESPAIR0_RXP0	J1	13	14	R1	SERDESPAIR1_RXP0
SERDESPAIR0_RXN0	K1	15	16	T1	SERDESPAIR1_RXN0
SERDESPAIR0_RXN1	L1	19	20	U1	SERDESPAIR1_RXN1
SERDESPAIR0_RXP1	M1	21	22	V1	SERDESPAIR1_RXP1
SERDESPAIR0_REFCLKN1(1)	-	25	26	-	SERDESPAIR1_REFCLKN1(1)
SERDESPAIR0_REFCLKP1(1)	-	27	28	-	SERDESPAIR1_REFCLKP1(1)
SERDESPAIR0_TXN1	M2	31	32	V2	SERDESPAIR1_TXN1
SERDESPAIR0_TXP1	N2	33	34	W2	SERDESPAIR1_TXP1
SERDESPAIR2_TXP0	B2	37	38	Y2	SERDESPAIR3_TXP0
SERDESPAIR2_TXN0	C2	39	40	AA2	SERDESPAIR3_TXN0
SERDESPAIR2_REFCLKP0	D4	43	44	AB4	SERDESPAIR3_REFCLKP0
SERDESPAIR2_REFCLKN0	D3	45	46	AB3	SERDESPAIR3_REFCLKN0
SERDESPAIR2_RXP0	C1	49	50	AA1	SERDESPAIR3_RXP0
SERDESPAIR2_RXN0	D1	51	52	AB1	SERDESPAIR3_RXN0
SERDESPAIR2_RXN1	E1	55	56	AC1	SERDESPAIR3_RXN1
SERDESPAIR2_RXP1	F1	57	58	AD1	SERDESPAIR3_RXP1
SERDESPAIR2_REFCLKN1(1)	-	61	62	-	SERDESPAIR3_REFCLKN1(1)
SERDESPAIR2_REFCLKP1(1)	-	63	64	-	SERDESPAIR3_REFCLKP1(1)
SERDESPAIR2_TXN1	F2	67	68	AD2	SERDESPAIR3_TXN1
SERDESPAIR2_TXP1	G2	69	70	AE2	SERDESPAIR3_TXP1
SERDESPAIR4_TXP0(2)	-	73	74	-	SERDESPAIR5_TXP0(2)
SERDESPAIR4_TXN0(2)	-	75	76	-	SERDESPAIR5_TXN0(2)
SERDESPAIR4_REFCLKP0(2)	-	79	80	-	SERDESPAIR5_REFCLKP0(2)
SERDESPAIR4_REFCLKN0(2)	-	81	82	-	SERDESPAIR5_REFCLKN0(2)