**Place & Route TRACE Report**

```
Loading design for application trce from file top_impl1.ncd.
Design name: top
NCD version: 3.2
Vendor:      LATTICE
Device:      LFE3-35EA
Package:     FTBGA256
Performance: 7
Loading device for application trce from file 'ec5a71x74.nph' in environment: D:/Diamond2_0/diamond/2.0/ispfpga.
Package Status:                     Final          Version 1.60
Performance Hardware Data Status:   Final          Version 31.22
Setup and Hold Report

--------------------------------------------------------------------------------
```

**Lattice TRACE Report - Setup, Version Diamond Version 2.0.0.154**

```
Thu Jun 26 08:10:19 2014

Copyright (c) 1991-1994 by NeoCAD Inc. All rights reserved.
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Copyright (c) 1995-2001 Lucent Technologies Inc.  All rights reserved.
Copyright (c) 2001 Agere Systems   All rights reserved.
Copyright (c) 2002-2012 Lattice Semiconductor Corporation,  All rights reserved.
```

**Report Information**

```
------------------
Command line:    trce -v 10 -gt -sethld -sp 7 -sphld m -o top_impl1.twr top_impl1.ncd top_impl1.prf
Design file:     top_impl1.ncd
Preference file: top_impl1.prf
Device,speed:    LFE3-35EA,7
Report level:    verbose report, limited to 10 items per preference
--------------------------------------------------------------------------------
```

**Preference Summary**

```
+ FREQUENCY NET "clk_125_c" 125.000000 MHz (0 errors)
            4096 items scored, 0 timing errors detected.
Report:  132.031MHz is the maximum frequency for this preference.

+ FREQUENCY NET "can_clk_c" 25.000000 MHz (0 errors)
            4096 items scored, 0 timing errors detected.
Report:   30.534MHz is the maximum frequency for this preference.

+ FREQUENCY NET "uart_clk_c" 25.000000 MHz (0 errors)
            4096 items scored, 0 timing errors detected.
Report:   39.801MHz is the maximum frequency for this preference.

+ FREQUENCY NET "pcie/pclk" 250.000000 MHz (0 errors)
            987 items scored, 0 timing errors detected.
Report:  314.762MHz is the maximum frequency for this preference.

+ FREQUENCY NET "pcie/u1_pcs_pipe/ff_rx_fclk_0" 250.000000 MHz (0 errors)
            1 item scored, 0 timing errors detected.
Report:  412.201MHz is the maximum frequency for this preference.

+ BLOCK PATH FROM PORT "rstn" (0 errors)
            119 items scored, 0 timing errors detected.

+ BLOCK PATH TO PORT "OUT*" (0 errors)
            0 items scored, 0 timing errors detected.

+ BLOCK PATH FROM PORT "INP*" (0 errors)
            16 items scored, 0 timing errors detected.

+ BLOCK PATH FROM PORT "SRAM_A*" (0 errors)
            0 items scored, 0 timing errors detected.

+ BLOCK PATH TO PORT "LED*" (0 errors)
            8 items scored, 0 timing errors detected.

+ BLOCK PATH FROM CELL "*ctc_reset_chx*" (0 errors)
            14 items scored, 0 timing errors detected.

+ MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*cnt_done_nfts_rx*" 2.000000 X (0 errors)
            214 items scored, 0 timing errors detected.

+ MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*ltssm_nfts_rx_skp*" 2.000000 X (0 errors)
            244 items scored, 0 timing errors detected.

+ MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr*" 6.000000 ns (0 errors)
            33 items scored, 0 timing errors detected.
Report:  635.728MHz is the maximum frequency for this preference.

+ MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr*" 6.000000 ns (0 errors)
            147 items scored, 0 timing errors detected.
Report:  267.094MHz is the maximum frequency for this preference.

+ MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr*" 6.000000 ns (0 errors)
            14 items scored, 0 timing errors detected.
Report:  739.098MHz is the maximum frequency for this preference.

+ MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr*" 6.000000 ns (0 errors)
            18 items scored, 0 timing errors detected.
Report:  603.500MHz is the maximum frequency for this preference.

+ MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data*" 6.000000 ns (0 errors)
            16 items scored, 0 timing errors detected.
Report:  453.515MHz is the maximum frequency for this preference.

+ MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl*" 6.000000 ns (0 errors)
            2 items scored, 0 timing errors detected.
Report:  474.158MHz is the maximum frequency for this preference.

42 potential circuit loops found in timing analysis.
BLOCK ASYNCPATHS
BLOCK RESETPATHS
BLOCK JTAG PATHS
--------------------------------------------------------------------------------



================================================================================
Preference: FREQUENCY NET "clk_125_c" 125.000000 MHz ;
            4096 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.426ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_arb/s7_sel  (from clk_125_c +)
   Destination:    FF         Data in       wb_tlc/intf/wb_adr_o_1[19]  (to clk_125_c +)

   Delay:               7.506ns  (32.2% logic, 67.8% route), 17 logic levels.

 Constraint Details:

      7.506ns physical path delay wb_arb/SLICE_6337 to wb_tlc/intf/SLICE_4284 meets
      8.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 0.426ns

 Physical Path Details:

      Data path wb_arb/SLICE_6337 to wb_tlc/intf/SLICE_4284:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R31C42B.CLK to     R31C42B.Q0 wb_arb/SLICE_6337 (from clk_125_c)
ROUTE        37     0.791     R31C42B.Q0 to     R30C45D.C0 wb_arb.s7_sel
CTOF_DEL    ---     0.164     R30C45D.C0 to     R30C45D.F0 wb_arb/SLICE_7632
ROUTE         1     0.279     R30C45D.F0 to     R30C45D.C1 wb_arb/s_ack_12_iv_0_1_1
CTOF_DEL    ---     0.164     R30C45D.C1 to     R30C45D.F1 wb_arb/SLICE_7632
ROUTE         1     0.703     R30C45D.F1 to     R30C48A.C0 wb_arb/s_ack_12_iv_0_1
CTOF_DEL    ---     0.164     R30C48A.C0 to     R30C48A.F0 SLICE_8751
ROUTE         1     0.824     R30C48A.F0 to     R29C40B.D0 wb_arb/s_ack_12_iv_0_1_2
CTOF_DEL    ---     0.164     R29C40B.D0 to     R29C40B.F0 SLICE_4827
ROUTE         7     0.899     R29C40B.F0 to     R23C39D.D0 reveal_ist_131
CTOF_DEL    ---     0.164     R23C39D.D0 to     R23C39D.F0 wb_tlc/intf/SLICE_6972
ROUTE         1     0.803     R23C39D.F0 to     R23C37A.B0 wb_tlc/intf/un1_sm_10_i
C0TOFCO_DE  ---     0.423     R23C37A.B0 to    R23C37A.FCO wb_tlc/intf/SLICE_361
ROUTE         1     0.000    R23C37A.FCO to    R23C37B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_0
FCITOFCO_D  ---     0.064    R23C37B.FCI to    R23C37B.FCO wb_tlc/intf/SLICE_362
ROUTE         1     0.000    R23C37B.FCO to    R23C37C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_2
FCITOFCO_D  ---     0.064    R23C37C.FCI to    R23C37C.FCO wb_tlc/intf/SLICE_363
ROUTE         1     0.000    R23C37C.FCO to    R23C38A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_4
FCITOFCO_D  ---     0.064    R23C38A.FCI to    R23C38A.FCO wb_tlc/intf/SLICE_364
ROUTE         1     0.000    R23C38A.FCO to    R23C38B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_6
FCITOFCO_D  ---     0.064    R23C38B.FCI to    R23C38B.FCO wb_tlc/intf/SLICE_365
ROUTE         1     0.000    R23C38B.FCO to    R23C38C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_8
FCITOFCO_D  ---     0.064    R23C38C.FCI to    R23C38C.FCO wb_tlc/intf/SLICE_366
ROUTE         1     0.000    R23C38C.FCO to    R23C39A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_10
FCITOFCO_D  ---     0.064    R23C39A.FCI to    R23C39A.FCO wb_tlc/intf/SLICE_367
```

```
ROUTE         1     0.000    R23C39A.FCO to    R23C39B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_12
FCITOFCO_D  ---     0.064    R23C39B.FCI to    R23C39B.FCO wb_tlc/intf/SLICE_368
ROUTE         1     0.000    R23C39B.FCO to    R23C39C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_14
FCITOFCO_D  ---     0.064    R23C39C.FCI to    R23C39C.FCO wb_tlc/intf/SLICE_369
ROUTE         1     0.000    R23C39C.FCO to    R23C40A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_16
FCITOF1_DE  ---     0.220    R23C40A.FCI to     R23C40A.F1 wb_tlc/intf/SLICE_370
ROUTE         1     0.793     R23C40A.F1 to     R27C40B.C1 wb_tlc/intf/un1_wb_adr_o_4_cry_17_0_S1
CTOF_DEL    ---     0.164     R27C40B.C1 to     R27C40B.F1 wb_tlc/intf/SLICE_4284
ROUTE         1     0.000     R27C40B.F1 to    R27C40B.DI1 wb_tlc/intf/wb_adr_o_32[19] (to clk_125_c)
                  --------
                    7.506   (32.2% logic, 67.8% route), 17 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_arb/SLICE_6337:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R31C42B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4284:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R27C40B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.485ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_arb/s7_sel  (from clk_125_c +)
   Destination:    FF         Data in       wb_tlc/intf/wb_adr_o_1[17]  (to clk_125_c +)

   Delay:               7.447ns  (31.6% logic, 68.4% route), 16 logic levels.

 Constraint Details:

      7.447ns physical path delay wb_arb/SLICE_6337 to wb_tlc/intf/SLICE_4283 meets
      8.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 0.485ns

 Physical Path Details:

      Data path wb_arb/SLICE_6337 to wb_tlc/intf/SLICE_4283:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R31C42B.CLK to     R31C42B.Q0 wb_arb/SLICE_6337 (from clk_125_c)
ROUTE        37     0.791     R31C42B.Q0 to     R30C45D.C0 wb_arb.s7_sel
CTOF_DEL    ---     0.164     R30C45D.C0 to     R30C45D.F0 wb_arb/SLICE_7632
ROUTE         1     0.279     R30C45D.F0 to     R30C45D.C1 wb_arb/s_ack_12_iv_0_1_1
CTOF_DEL    ---     0.164     R30C45D.C1 to     R30C45D.F1 wb_arb/SLICE_7632
ROUTE         1     0.703     R30C45D.F1 to     R30C48A.C0 wb_arb/s_ack_12_iv_0_1
CTOF_DEL    ---     0.164     R30C48A.C0 to     R30C48A.F0 SLICE_8751
ROUTE         1     0.824     R30C48A.F0 to     R29C40B.D0 wb_arb/s_ack_12_iv_0_1_2
CTOF_DEL    ---     0.164     R29C40B.D0 to     R29C40B.F0 SLICE_4827
ROUTE         7     0.899     R29C40B.F0 to     R23C39D.D0 reveal_ist_131
CTOF_DEL    ---     0.164     R23C39D.D0 to     R23C39D.F0 wb_tlc/intf/SLICE_6972
ROUTE         1     0.803     R23C39D.F0 to     R23C37A.B0 wb_tlc/intf/un1_sm_10_i
C0TOFCO_DE  ---     0.423     R23C37A.B0 to    R23C37A.FCO wb_tlc/intf/SLICE_361
ROUTE         1     0.000    R23C37A.FCO to    R23C37B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_0
FCITOFCO_D  ---     0.064    R23C37B.FCI to    R23C37B.FCO wb_tlc/intf/SLICE_362
ROUTE         1     0.000    R23C37B.FCO to    R23C37C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_2
FCITOFCO_D  ---     0.064    R23C37C.FCI to    R23C37C.FCO wb_tlc/intf/SLICE_363
ROUTE         1     0.000    R23C37C.FCO to    R23C38A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_4
FCITOFCO_D  ---     0.064    R23C38A.FCI to    R23C38A.FCO wb_tlc/intf/SLICE_364
ROUTE         1     0.000    R23C38A.FCO to    R23C38B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_6
FCITOFCO_D  ---     0.064    R23C38B.FCI to    R23C38B.FCO wb_tlc/intf/SLICE_365
ROUTE         1     0.000    R23C38B.FCO to    R23C38C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_8
FCITOFCO_D  ---     0.064    R23C38C.FCI to    R23C38C.FCO wb_tlc/intf/SLICE_366
ROUTE         1     0.000    R23C38C.FCO to    R23C39A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_10
FCITOFCO_D  ---     0.064    R23C39A.FCI to    R23C39A.FCO wb_tlc/intf/SLICE_367
ROUTE         1     0.000    R23C39A.FCO to    R23C39B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_12
FCITOFCO_D  ---     0.064    R23C39B.FCI to    R23C39B.FCO wb_tlc/intf/SLICE_368
ROUTE         1     0.000    R23C39B.FCO to    R23C39C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_14
FCITOF1_DE  ---     0.220    R23C39C.FCI to     R23C39C.F1 wb_tlc/intf/SLICE_369
ROUTE         1     0.798     R23C39C.F1 to     R29C40C.C1 wb_tlc/intf/un1_wb_adr_o_4_cry_15_0_S1
CTOF_DEL    ---     0.164     R29C40C.C1 to     R29C40C.F1 wb_tlc/intf/SLICE_4283
ROUTE         1     0.000     R29C40C.F1 to    R29C40C.DI1 wb_tlc/intf/wb_adr_o_32[17] (to clk_125_c)
                  --------
                    7.447   (31.6% logic, 68.4% route), 16 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_arb/SLICE_6337:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R31C42B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4283:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R29C40C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.488ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_arb/s7_sel  (from clk_125_c +)
   Destination:    FF         Data in       wb_tlc/intf/wb_adr_o_1[20]  (to clk_125_c +)

   Delay:               7.444ns  (32.3% logic, 67.7% route), 18 logic levels.

 Constraint Details:

      7.444ns physical path delay wb_arb/SLICE_6337 to wb_tlc/intf/SLICE_4285 meets
      8.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 0.488ns

 Physical Path Details:

      Data path wb_arb/SLICE_6337 to wb_tlc/intf/SLICE_4285:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R31C42B.CLK to     R31C42B.Q0 wb_arb/SLICE_6337 (from clk_125_c)
ROUTE        37     0.791     R31C42B.Q0 to     R30C45D.C0 wb_arb.s7_sel
CTOF_DEL    ---     0.164     R30C45D.C0 to     R30C45D.F0 wb_arb/SLICE_7632
ROUTE         1     0.279     R30C45D.F0 to     R30C45D.C1 wb_arb/s_ack_12_iv_0_1_1
CTOF_DEL    ---     0.164     R30C45D.C1 to     R30C45D.F1 wb_arb/SLICE_7632
ROUTE         1     0.703     R30C45D.F1 to     R30C48A.C0 wb_arb/s_ack_12_iv_0_1
CTOF_DEL    ---     0.164     R30C48A.C0 to     R30C48A.F0 SLICE_8751
ROUTE         1     0.824     R30C48A.F0 to     R29C40B.D0 wb_arb/s_ack_12_iv_0_1_2
CTOF_DEL    ---     0.164     R29C40B.D0 to     R29C40B.F0 SLICE_4827
ROUTE         7     0.899     R29C40B.F0 to     R23C39D.D0 reveal_ist_131
CTOF_DEL    ---     0.164     R23C39D.D0 to     R23C39D.F0 wb_tlc/intf/SLICE_6972
ROUTE         1     0.803     R23C39D.F0 to     R23C37A.B0 wb_tlc/intf/un1_sm_10_i
C0TOFCO_DE  ---     0.423     R23C37A.B0 to    R23C37A.FCO wb_tlc/intf/SLICE_361
ROUTE         1     0.000    R23C37A.FCO to    R23C37B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_0
FCITOFCO_D  ---     0.064    R23C37B.FCI to    R23C37B.FCO wb_tlc/intf/SLICE_362
ROUTE         1     0.000    R23C37B.FCO to    R23C37C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_2
FCITOFCO_D  ---     0.064    R23C37C.FCI to    R23C37C.FCO wb_tlc/intf/SLICE_363
ROUTE         1     0.000    R23C37C.FCO to    R23C38A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_4
FCITOFCO_D  ---     0.064    R23C38A.FCI to    R23C38A.FCO wb_tlc/intf/SLICE_364
ROUTE         1     0.000    R23C38A.FCO to    R23C38B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_6
FCITOFCO_D  ---     0.064    R23C38B.FCI to    R23C38B.FCO wb_tlc/intf/SLICE_365
ROUTE         1     0.000    R23C38B.FCO to    R23C38C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_8
FCITOFCO_D  ---     0.064    R23C38C.FCI to    R23C38C.FCO wb_tlc/intf/SLICE_366
ROUTE         1     0.000    R23C38C.FCO to    R23C39A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_10
FCITOFCO_D  ---     0.064    R23C39A.FCI to    R23C39A.FCO wb_tlc/intf/SLICE_367
ROUTE         1     0.000    R23C39A.FCO to    R23C39B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_12
FCITOFCO_D  ---     0.064    R23C39B.FCI to    R23C39B.FCO wb_tlc/intf/SLICE_368
ROUTE         1     0.000    R23C39B.FCO to    R23C39C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_14
FCITOFCO_D  ---     0.064    R23C39C.FCI to    R23C39C.FCO wb_tlc/intf/SLICE_369
ROUTE         1     0.000    R23C39C.FCO to    R23C40A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_16
FCITOFCO_D  ---     0.064    R23C40A.FCI to    R23C40A.FCO wb_tlc/intf/SLICE_370
ROUTE         1     0.000    R23C40A.FCO to    R23C40B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_18
FCITOF0_DE  ---     0.149    R23C40B.FCI to     R23C40B.F0 wb_tlc/intf/SLICE_371
ROUTE         1     0.738     R23C40B.F0 to     R22C38C.C0 wb_tlc/intf/un1_wb_adr_o_4_cry_19_0_S0
CTOF_DEL    ---     0.164     R22C38C.C0 to     R22C38C.F0 wb_tlc/intf/SLICE_4285
ROUTE         1     0.000     R22C38C.F0 to    R22C38C.DI0 wb_tlc/intf/wb_adr_o_32[20] (to clk_125_c)
                  --------
                    7.444   (32.3% logic, 67.7% route), 18 logic levels.

 Clock Skew Details:
```

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_arb/SLICE_6337:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R31C42B.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4285:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R22C38C.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 0.521ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q wb_arb/s5_sel (from clk_125_c +)
Destination: FF Data in wb_tlc/intf/wb_adr_o_1[19] (to clk_125_c +)

Delay: 7.411ns (32.6% logic, 67.4% route), 17 logic levels.

Constraint Details:

7.411ns physical path delay wb_arb/SLICE_6335 to wb_tlc/intf/SLICE_4284 meets
8.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 7.932ns) by 0.521ns

Physical Path Details:

Data path wb_arb/SLICE_6335 to wb_tlc/intf/SLICE_4284:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 R30C43A.CLK to | R30C43A.Q0 | wb_arb/SLICE_6335 (from clk_125_c) |
| ROUTE | 22 | 0.537 R30C43A.Q0 to | R30C42D.C1 | wb_arb.s5_sel |
| CTOF_DEL | --- | 0.164 R30C42D.C1 to | R30C42D.F1 | wb_arb/SLICE_7625 |
| ROUTE | 3 | 0.592 R30C42D.F1 to | R30C44C.D1 | wb_arb/s0_cyc_o20[0] |
| CTOF_DEL | --- | 0.164 R30C44C.D1 to | R30C44C.F1 | SLICE_6960 |
| ROUTE | 1 | 0.342 R30C44C.F1 to | R30C44C.D0 | wb_arb/s_ack_12_iv_0_0 |
| CTOF_DEL | --- | 0.164 R30C44C.D0 to | R30C44C.F0 | SLICE_6960 |
| ROUTE | 1 | 1.031 R30C44C.F0 to | R29C40B.B0 | wb_arb/s_ack_12_iv_0_3 |
| CTOF_DEL | --- | 0.164 R29C40B.B0 to | R29C40B.F0 | SLICE_4827 |
| ROUTE | 7 | 0.899 R29C40B.F0 to | R23C39D.D0 | reveal_ist_131 |
| CTOF_DEL | --- | 0.164 R23C39D.D0 to | R23C39D.F0 | wb_tlc/intf/SLICE_6972 |
| ROUTE | 1 | 0.803 R23C39D.F0 to | R23C37A.B0 | wb_tlc/intf/un1_sm_10_i |
| C0TOFCO_DE | --- | 0.423 R23C37A.B0 to | R23C37A.FCO | wb_tlc/intf/SLICE_361 |
| ROUTE | 1 | 0.000 R23C37A.FCO to | R23C37B.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_0 |
| FCITOFCO_D | --- | 0.064 R23C37B.FCI to | R23C37B.FCO | wb_tlc/intf/SLICE_362 |
| ROUTE | 1 | 0.000 R23C37B.FCO to | R23C37C.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_2 |
| FCITOFCO_D | --- | 0.064 R23C37C.FCI to | R23C37C.FCO | wb_tlc/intf/SLICE_363 |
| ROUTE | 1 | 0.000 R23C37C.FCO to | R23C38A.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_4 |
| FCITOFCO_D | --- | 0.064 R23C38A.FCI to | R23C38A.FCO | wb_tlc/intf/SLICE_364 |
| ROUTE | 1 | 0.000 R23C38A.FCO to | R23C38B.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_6 |
| FCITOFCO_D | --- | 0.064 R23C38B.FCI to | R23C38B.FCO | wb_tlc/intf/SLICE_365 |
| ROUTE | 1 | 0.000 R23C38B.FCO to | R23C38C.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_8 |
| FCITOFCO_D | --- | 0.064 R23C38C.FCI to | R23C38C.FCO | wb_tlc/intf/SLICE_366 |
| ROUTE | 1 | 0.000 R23C38C.FCO to | R23C39A.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_10 |
| FCITOFCO_D | --- | 0.064 R23C39A.FCI to | R23C39A.FCO | wb_tlc/intf/SLICE_367 |
| ROUTE | 1 | 0.000 R23C39A.FCO to | R23C39B.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_12 |
| FCITOFCO_D | --- | 0.064 R23C39B.FCI to | R23C39B.FCO | wb_tlc/intf/SLICE_368 |
| ROUTE | 1 | 0.000 R23C39B.FCO to | R23C39C.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_14 |
| FCITOFCO_D | --- | 0.064 R23C39C.FCI to | R23C39C.FCO | wb_tlc/intf/SLICE_369 |
| ROUTE | 1 | 0.000 R23C39C.FCO to | R23C40A.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_16 |
| FCITOF1_DE | --- | 0.220 R23C40A.FCI to | R23C40A.F1 | wb_tlc/intf/SLICE_370 |
| ROUTE | 1 | 0.793 R23C40A.F1 to | R27C40B.C1 | wb_tlc/intf/un1_wb_adr_o_4_cry_17_0_S1 |
| CTOF_DEL | --- | 0.164 R27C40B.C1 to | R27C40B.F1 | wb_tlc/intf/SLICE_4284 |
| ROUTE | 1 | 0.000 R27C40B.F1 to | R27C40B.DI1 | wb_tlc/intf/wb_adr_o_32[19] (to clk_125_c) |
| | | 7.411 (32.6% logic, 67.4% route), 17 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_arb/SLICE_6335:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R30C43A.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4284:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R27C40B.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 0.533ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q wb_arb/s7_sel (from clk_125_c +)
Destination: FF Data in wb_tlc/intf/wb_adr_o_1[13] (to clk_125_c +)

Delay: 7.399ns (30.0% logic, 70.0% route), 14 logic levels.

Constraint Details:

7.399ns physical path delay wb_arb/SLICE_6337 to wb_tlc/intf/SLICE_4281 meets
8.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 7.932ns) by 0.533ns

Physical Path Details:

Data path wb_arb/SLICE_6337 to wb_tlc/intf/SLICE_4281:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 R31C42B.CLK to | R31C42B.Q0 | wb_arb/SLICE_6337 (from clk_125_c) |
| ROUTE | 37 | 0.791 R31C42B.Q0 to | R30C45D.C0 | wb_arb.s7_sel |
| CTOF_DEL | --- | 0.164 R30C45D.C0 to | R30C45D.F0 | wb_arb/SLICE_7632 |
| ROUTE | 1 | 0.279 R30C45D.F0 to | R30C45D.C1 | wb_arb/s_ack_12_iv_0_1_1 |
| CTOF_DEL | --- | 0.164 R30C45D.C1 to | R30C45D.F1 | wb_arb/SLICE_7632 |
| ROUTE | 1 | 0.703 R30C45D.F1 to | R30C48A.C0 | wb_arb/s_ack_12_iv_0_1 |
| CTOF_DEL | --- | 0.164 R30C48A.C0 to | R30C48A.F0 | SLICE_8751 |
| ROUTE | 1 | 0.824 R30C48A.F0 to | R29C40B.D0 | wb_arb/s_ack_12_iv_0_1_2 |
| CTOF_DEL | --- | 0.164 R29C40B.D0 to | R29C40B.F0 | SLICE_4827 |
| ROUTE | 7 | 0.899 R29C40B.F0 to | R23C39D.D0 | reveal_ist_131 |
| CTOF_DEL | --- | 0.164 R23C39D.D0 to | R23C39D.F0 | wb_tlc/intf/SLICE_6972 |
| ROUTE | 1 | 0.803 R23C39D.F0 to | R23C37A.B0 | wb_tlc/intf/un1_sm_10_i |
| C0TOFCO_DE | --- | 0.423 R23C37A.B0 to | R23C37A.FCO | wb_tlc/intf/SLICE_361 |
| ROUTE | 1 | 0.000 R23C37A.FCO to | R23C37B.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_0 |
| FCITOFCO_D | --- | 0.064 R23C37B.FCI to | R23C37B.FCO | wb_tlc/intf/SLICE_362 |
| ROUTE | 1 | 0.000 R23C37B.FCO to | R23C37C.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_2 |
| FCITOFCO_D | --- | 0.064 R23C37C.FCI to | R23C37C.FCO | wb_tlc/intf/SLICE_363 |
| ROUTE | 1 | 0.000 R23C37C.FCO to | R23C38A.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_4 |
| FCITOFCO_D | --- | 0.064 R23C38A.FCI to | R23C38A.FCO | wb_tlc/intf/SLICE_364 |
| ROUTE | 1 | 0.000 R23C38A.FCO to | R23C38B.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_6 |
| FCITOFCO_D | --- | 0.064 R23C38B.FCI to | R23C38B.FCO | wb_tlc/intf/SLICE_365 |
| ROUTE | 1 | 0.000 R23C38B.FCO to | R23C38C.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_8 |
| FCITOFCO_D | --- | 0.064 R23C38C.FCI to | R23C38C.FCO | wb_tlc/intf/SLICE_366 |
| ROUTE | 1 | 0.000 R23C38C.FCO to | R23C39A.FCI | wb_tlc/intf/un1_wb_adr_o_4_cry_10 |
| FCITOF1_DE | --- | 0.220 R23C39A.FCI to | R23C39A.F1 | wb_tlc/intf/SLICE_367 |
| ROUTE | 1 | 0.878 R23C39A.F1 to | R28C39B.D1 | wb_tlc/intf/un1_wb_adr_o_4_cry_11_0_S1 |
| CTOF_DEL | --- | 0.164 R28C39B.D1 to | R28C39B.F1 | wb_tlc/intf/SLICE_4281 |
| ROUTE | 1 | 0.000 R28C39B.F1 to | R28C39B.DI1 | wb_tlc/intf/wb_adr_o_32[13] (to clk_125_c) |
| | | 7.399 (30.0% logic, 70.0% route), 14 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_arb/SLICE_6337:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R31C42B.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4281:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R28C39B.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 0.556ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q wb_arb/s7_sel (from clk_125_c +)

```
   Destination:    FF         Data in        wb_tlc/intf/wb_adr_o_1[16]  (to clk_125_c +)

   Delay:               7.376ns  (30.9% logic, 69.1% route), 16 logic levels.

 Constraint Details:

      7.376ns physical path delay wb_arb/SLICE_6337 to wb_tlc/intf/SLICE_4283 meets
      8.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 0.556ns

 Physical Path Details:

      Data path wb_arb/SLICE_6337 to wb_tlc/intf/SLICE_4283:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R31C42B.CLK to     R31C42B.Q0 wb_arb/SLICE_6337 (from clk_125_c)
ROUTE        37     0.791     R31C42B.Q0 to     R30C45D.C0 wb_arb.s7_sel
CTOF_DEL    ---     0.164     R30C45D.C0 to     R30C45D.F0 wb_arb/SLICE_7632
ROUTE         1     0.279     R30C45D.F0 to     R30C45D.C1 wb_arb/s_ack_12_iv_0_1_1
CTOF_DEL    ---     0.164     R30C45D.C1 to     R30C45D.F1 wb_arb/SLICE_7632
ROUTE         1     0.703     R30C45D.F1 to     R30C48A.C0 wb_arb/s_ack_12_iv_0_1
CTOF_DEL    ---     0.164     R30C48A.C0 to     R30C48A.F0 SLICE_8751
ROUTE         1     0.824     R30C48A.F0 to     R29C40B.D0 wb_arb/s_ack_12_iv_0_1_2
CTOF_DEL    ---     0.164     R29C40B.D0 to     R29C40B.F0 SLICE_4827
ROUTE         7     0.899     R29C40B.F0 to     R23C39D.D0 reveal_ist_131
CTOF_DEL    ---     0.164     R23C39D.D0 to     R23C39D.F0 wb_tlc/intf/SLICE_6972
ROUTE         1     0.803     R23C39D.F0 to     R23C37A.B0 wb_tlc/intf/un1_sm_10_i
C0TOFCO_DE  ---     0.423     R23C37A.B0 to    R23C37A.FCO wb_tlc/intf/SLICE_361
ROUTE         1     0.000    R23C37A.FCO to    R23C37B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_0
FCITOFCO_D  ---     0.064    R23C37B.FCI to    R23C37B.FCO wb_tlc/intf/SLICE_362
ROUTE         1     0.000    R23C37B.FCO to    R23C37C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_2
FCITOFCO_D  ---     0.064    R23C37C.FCI to    R23C37C.FCO wb_tlc/intf/SLICE_363
ROUTE         1     0.000    R23C37C.FCO to    R23C38A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_4
FCITOFCO_D  ---     0.064    R23C38A.FCI to    R23C38A.FCO wb_tlc/intf/SLICE_364
ROUTE         1     0.000    R23C38A.FCO to    R23C38B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_6
FCITOFCO_D  ---     0.064    R23C38B.FCI to    R23C38B.FCO wb_tlc/intf/SLICE_365
ROUTE         1     0.000    R23C38B.FCO to    R23C38C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_8
FCITOFCO_D  ---     0.064    R23C38C.FCI to    R23C38C.FCO wb_tlc/intf/SLICE_366
ROUTE         1     0.000    R23C38C.FCO to    R23C39A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_10
FCITOFCO_D  ---     0.064    R23C39A.FCI to    R23C39A.FCO wb_tlc/intf/SLICE_367
ROUTE         1     0.000    R23C39A.FCO to    R23C39B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_12
FCITOFCO_D  ---     0.064    R23C39B.FCI to    R23C39B.FCO wb_tlc/intf/SLICE_368
ROUTE         1     0.000    R23C39B.FCO to    R23C39C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_14
FCITOF0_DE  ---     0.149    R23C39C.FCI to     R23C39C.F0 wb_tlc/intf/SLICE_369
ROUTE         1     0.798     R23C39C.F0 to     R29C40C.C0 wb_tlc/intf/un1_wb_adr_o_4_cry_15_0_S0
CTOF_DEL    ---     0.164     R29C40C.C0 to     R29C40C.F0 wb_tlc/intf/SLICE_4283
ROUTE         1     0.000     R29C40C.F0 to    R29C40C.DI0 wb_tlc/intf/wb_adr_o_32[16] (to clk_125_c)
                  --------
                    7.376   (30.9% logic, 69.1% route), 16 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_arb/SLICE_6337:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R31C42B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4283:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R29C40C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.557ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_arb/s7_sel  (from clk_125_c +)
   Destination:    FF         Data in        wb_tlc/intf/wb_adr_o_1[23]  (to clk_125_c +)

   Delay:               7.375ns  (34.5% logic, 65.5% route), 19 logic levels.

 Constraint Details:

      7.375ns physical path delay wb_arb/SLICE_6337 to wb_tlc/intf/SLICE_4286 meets
      8.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 0.557ns

 Physical Path Details:

      Data path wb_arb/SLICE_6337 to wb_tlc/intf/SLICE_4286:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R31C42B.CLK to     R31C42B.Q0 wb_arb/SLICE_6337 (from clk_125_c)
ROUTE        37     0.791     R31C42B.Q0 to     R30C45D.C0 wb_arb.s7_sel
CTOF_DEL    ---     0.164     R30C45D.C0 to     R30C45D.F0 wb_arb/SLICE_7632
ROUTE         1     0.279     R30C45D.F0 to     R30C45D.C1 wb_arb/s_ack_12_iv_0_1_1
CTOF_DEL    ---     0.164     R30C45D.C1 to     R30C45D.F1 wb_arb/SLICE_7632
ROUTE         1     0.703     R30C45D.F1 to     R30C48A.C0 wb_arb/s_ack_12_iv_0_1
CTOF_DEL    ---     0.164     R30C48A.C0 to     R30C48A.F0 SLICE_8751
ROUTE         1     0.824     R30C48A.F0 to     R29C40B.D0 wb_arb/s_ack_12_iv_0_1_2
CTOF_DEL    ---     0.164     R29C40B.D0 to     R29C40B.F0 SLICE_4827
ROUTE         7     0.899     R29C40B.F0 to     R23C39D.D0 reveal_ist_131
CTOF_DEL    ---     0.164     R23C39D.D0 to     R23C39D.F0 wb_tlc/intf/SLICE_6972
ROUTE         1     0.803     R23C39D.F0 to     R23C37A.B0 wb_tlc/intf/un1_sm_10_i
C0TOFCO_DE  ---     0.423     R23C37A.B0 to    R23C37A.FCO wb_tlc/intf/SLICE_361
ROUTE         1     0.000    R23C37A.FCO to    R23C37B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_0
FCITOFCO_D  ---     0.064    R23C37B.FCI to    R23C37B.FCO wb_tlc/intf/SLICE_362
ROUTE         1     0.000    R23C37B.FCO to    R23C37C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_2
FCITOFCO_D  ---     0.064    R23C37C.FCI to    R23C37C.FCO wb_tlc/intf/SLICE_363
ROUTE         1     0.000    R23C37C.FCO to    R23C38A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_4
FCITOFCO_D  ---     0.064    R23C38A.FCI to    R23C38A.FCO wb_tlc/intf/SLICE_364
ROUTE         1     0.000    R23C38A.FCO to    R23C38B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_6
FCITOFCO_D  ---     0.064    R23C38B.FCI to    R23C38B.FCO wb_tlc/intf/SLICE_365
ROUTE         1     0.000    R23C38B.FCO to    R23C38C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_8
FCITOFCO_D  ---     0.064    R23C38C.FCI to    R23C38C.FCO wb_tlc/intf/SLICE_366
ROUTE         1     0.000    R23C38C.FCO to    R23C39A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_10
FCITOFCO_D  ---     0.064    R23C39A.FCI to    R23C39A.FCO wb_tlc/intf/SLICE_367
ROUTE         1     0.000    R23C39A.FCO to    R23C39B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_12
FCITOFCO_D  ---     0.064    R23C39B.FCI to    R23C39B.FCO wb_tlc/intf/SLICE_368
ROUTE         1     0.000    R23C39B.FCO to    R23C39C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_14
FCITOFCO_D  ---     0.064    R23C39C.FCI to    R23C39C.FCO wb_tlc/intf/SLICE_369
ROUTE         1     0.000    R23C39C.FCO to    R23C40A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_16
FCITOFCO_D  ---     0.064    R23C40A.FCI to    R23C40A.FCO wb_tlc/intf/SLICE_370
ROUTE         1     0.000    R23C40A.FCO to    R23C40B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_18
FCITOFCO_D  ---     0.064    R23C40B.FCI to    R23C40B.FCO wb_tlc/intf/SLICE_371
ROUTE         1     0.000    R23C40B.FCO to    R23C40C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_20
FCITOF1_DE  ---     0.220    R23C40C.FCI to     R23C40C.F1 wb_tlc/intf/SLICE_372
ROUTE         1     0.534     R23C40C.F1 to     R22C40B.C1 wb_tlc/intf/un1_wb_adr_o_4_cry_21_0_S1
CTOF_DEL    ---     0.164     R22C40B.C1 to     R22C40B.F1 wb_tlc/intf/SLICE_4286
ROUTE         1     0.000     R22C40B.F1 to    R22C40B.DI1 wb_tlc/intf/wb_adr_o_32[23] (to clk_125_c)
                  --------
                    7.375   (34.5% logic, 65.5% route), 19 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_arb/SLICE_6337:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R31C42B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4286:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C40B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.578ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_arb/s7_sel  (from clk_125_c +)
   Destination:    FF         Data in        wb_tlc/intf/wb_adr_o_1[21]  (to clk_125_c +)

   Delay:               7.354ns  (33.7% logic, 66.3% route), 18 logic levels.

 Constraint Details:

      7.354ns physical path delay wb_arb/SLICE_6337 to wb_tlc/intf/SLICE_4285 meets
      8.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 0.578ns

 Physical Path Details:
```

Data path wb_arb/SLICE_6337 to wb_tlc/intf/SLICE_4285:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 | R31C42B.CLK to | R31C42B.Q0 wb_arb/SLICE_6337 (from clk_125_c) |
| ROUTE | 37 | 0.791 | R31C42B.Q0 to | R30C45D.C0 wb_arb.s7_sel |
| CTOF_DEL | --- | 0.164 | R30C45D.C0 to | R30C45D.F0 wb_arb/SLICE_7632 |
| ROUTE | 1 | 0.279 | R30C45D.F0 to | R30C45D.C1 wb_arb/s_ack_12_iv_0_1_1 |
| CTOF_DEL | --- | 0.164 | R30C45D.C1 to | R30C45D.F1 wb_arb/SLICE_7632 |
| ROUTE | 1 | 0.703 | R30C45D.F1 to | R30C48A.C0 wb_arb/s_ack_12_iv_0_1 |
| CTOF_DEL | --- | 0.164 | R30C48A.C0 to | R30C48A.F0 SLICE_8751 |
| ROUTE | 1 | 0.824 | R30C48A.F0 to | R29C40B.D0 wb_arb/s_ack_12_iv_0_1_2 |
| CTOF_DEL | --- | 0.164 | R29C40B.D0 to | R29C40B.F0 SLICE_4827 |
| ROUTE | 7 | 0.899 | R29C40B.F0 to | R23C39D.D0 reveal_ist_131 |
| CTOF_DEL | --- | 0.164 | R23C39D.D0 to | R23C39D.F0 wb_tlc/intf/SLICE_6972 |
| ROUTE | 1 | 0.803 | R23C39D.F0 to | R23C37A.B0 wb_tlc/intf/un1_sm_10_i |
| C0TOFCO_DE | --- | 0.423 | R23C37A.B0 to | R23C37A.FCO wb_tlc/intf/SLICE_361 |
| ROUTE | 1 | 0.000 | R23C37A.FCO to | R23C37B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_0 |
| FCITOFCO_D | --- | 0.064 | R23C37B.FCI to | R23C37B.FCO wb_tlc/intf/SLICE_362 |
| ROUTE | 1 | 0.000 | R23C37B.FCO to | R23C37C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_2 |
| FCITOFCO_D | --- | 0.064 | R23C37C.FCI to | R23C37C.FCO wb_tlc/intf/SLICE_363 |
| ROUTE | 1 | 0.000 | R23C37C.FCO to | R23C38A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_4 |
| FCITOFCO_D | --- | 0.064 | R23C38A.FCI to | R23C38A.FCO wb_tlc/intf/SLICE_364 |
| ROUTE | 1 | 0.000 | R23C38A.FCO to | R23C38B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_6 |
| FCITOFCO_D | --- | 0.064 | R23C38B.FCI to | R23C38B.FCO wb_tlc/intf/SLICE_365 |
| ROUTE | 1 | 0.000 | R23C38B.FCO to | R23C38C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_8 |
| FCITOFCO_D | --- | 0.064 | R23C38C.FCI to | R23C38C.FCO wb_tlc/intf/SLICE_366 |
| ROUTE | 1 | 0.000 | R23C38C.FCO to | R23C39A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_10 |
| FCITOFCO_D | --- | 0.064 | R23C39A.FCI to | R23C39A.FCO wb_tlc/intf/SLICE_367 |
| ROUTE | 1 | 0.000 | R23C39A.FCO to | R23C39B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_12 |
| FCITOFCO_D | --- | 0.064 | R23C39B.FCI to | R23C39B.FCO wb_tlc/intf/SLICE_368 |
| ROUTE | 1 | 0.000 | R23C39B.FCO to | R23C39C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_14 |
| FCITOFCO_D | --- | 0.064 | R23C39C.FCI to | R23C39C.FCO wb_tlc/intf/SLICE_369 |
| ROUTE | 1 | 0.000 | R23C39C.FCO to | R23C40A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_16 |
| FCITOFCO_D | --- | 0.064 | R23C40A.FCI to | R23C40A.FCO wb_tlc/intf/SLICE_370 |
| ROUTE | 1 | 0.000 | R23C40A.FCO to | R23C40B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_18 |
| FCITOF1_DE | --- | 0.220 | R23C40B.FCI to | R23C40B.F1 wb_tlc/intf/SLICE_371 |
| ROUTE | 1 | 0.577 | R23C40B.F1 to | R22C38C.D1 wb_tlc/intf/un1_wb_adr_o_4_cry_19_0_S1 |
| CTOF_DEL | --- | 0.164 | R22C38C.D1 to | R22C38C.F1 wb_tlc/intf/SLICE_4285 |
| ROUTE | 1 | 0.000 | R22C38C.F1 to | R22C38C.DI1 wb_tlc/intf/wb_adr_o_32[21] (to clk_125_c) |
| | | 7.354 | (33.7% logic, 66.3% route), 18 logic levels. | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_arb/SLICE_6337:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R31C42B.CLK clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4285:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R22C38C.CLK clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | |

Passed: The following path meets requirements by 0.580ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q wb_arb/s5_sel (from clk_125_c +)
Destination: FF Data in wb_tlc/intf/wb_adr_o_1[17] (to clk_125_c +)

Delay: 7.352ns (32.0% logic, 68.0% route), 16 logic levels.

Constraint Details:

7.352ns physical path delay wb_arb/SLICE_6335 to wb_tlc/intf/SLICE_4283 meets
8.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 7.932ns) by 0.580ns

Physical Path Details:

Data path wb_arb/SLICE_6335 to wb_tlc/intf/SLICE_4283:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 | R30C43A.CLK to | R30C43A.Q0 wb_arb/SLICE_6335 (from clk_125_c) |
| ROUTE | 22 | 0.537 | R30C43A.Q0 to | R30C42D.C1 wb_arb.s5_sel |
| CTOF_DEL | --- | 0.164 | R30C42D.C1 to | R30C42D.F1 wb_arb/SLICE_7625 |
| ROUTE | 3 | 0.592 | R30C42D.F1 to | R30C44C.D1 wb_arb/s0_cyc_o20[0] |
| CTOF_DEL | --- | 0.164 | R30C44C.D1 to | R30C44C.F1 SLICE_6960 |
| ROUTE | 1 | 0.342 | R30C44C.F1 to | R30C44C.D0 wb_arb/s_ack_12_iv_0_0 |
| CTOF_DEL | --- | 0.164 | R30C44C.D0 to | R30C44C.F0 SLICE_6960 |
| ROUTE | 1 | 1.031 | R30C44C.F0 to | R29C40B.B0 wb_arb/s_ack_12_iv_0_3 |
| CTOF_DEL | --- | 0.164 | R29C40B.B0 to | R29C40B.F0 SLICE_4827 |
| ROUTE | 7 | 0.899 | R29C40B.F0 to | R23C39D.D0 reveal_ist_131 |
| CTOF_DEL | --- | 0.164 | R23C39D.D0 to | R23C39D.F0 wb_tlc/intf/SLICE_6972 |
| ROUTE | 1 | 0.803 | R23C39D.F0 to | R23C37A.B0 wb_tlc/intf/un1_sm_10_i |
| C0TOFCO_DE | --- | 0.423 | R23C37A.B0 to | R23C37A.FCO wb_tlc/intf/SLICE_361 |
| ROUTE | 1 | 0.000 | R23C37A.FCO to | R23C37B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_0 |
| FCITOFCO_D | --- | 0.064 | R23C37B.FCI to | R23C37B.FCO wb_tlc/intf/SLICE_362 |
| ROUTE | 1 | 0.000 | R23C37B.FCO to | R23C37C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_2 |
| FCITOFCO_D | --- | 0.064 | R23C37C.FCI to | R23C37C.FCO wb_tlc/intf/SLICE_363 |
| ROUTE | 1 | 0.000 | R23C37C.FCO to | R23C38A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_4 |
| FCITOFCO_D | --- | 0.064 | R23C38A.FCI to | R23C38A.FCO wb_tlc/intf/SLICE_364 |
| ROUTE | 1 | 0.000 | R23C38A.FCO to | R23C38B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_6 |
| FCITOFCO_D | --- | 0.064 | R23C38B.FCI to | R23C38B.FCO wb_tlc/intf/SLICE_365 |
| ROUTE | 1 | 0.000 | R23C38B.FCO to | R23C38C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_8 |
| FCITOFCO_D | --- | 0.064 | R23C38C.FCI to | R23C38C.FCO wb_tlc/intf/SLICE_366 |
| ROUTE | 1 | 0.000 | R23C38C.FCO to | R23C39A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_10 |
| FCITOFCO_D | --- | 0.064 | R23C39A.FCI to | R23C39A.FCO wb_tlc/intf/SLICE_367 |
| ROUTE | 1 | 0.000 | R23C39A.FCO to | R23C39B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_12 |
| FCITOFCO_D | --- | 0.064 | R23C39B.FCI to | R23C39B.FCO wb_tlc/intf/SLICE_368 |
| ROUTE | 1 | 0.000 | R23C39B.FCO to | R23C39C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_14 |
| FCITOF1_DE | --- | 0.220 | R23C39C.FCI to | R23C39C.F1 wb_tlc/intf/SLICE_369 |
| ROUTE | 1 | 0.798 | R23C39C.F1 to | R29C40C.C1 wb_tlc/intf/un1_wb_adr_o_4_cry_15_0_S1 |
| CTOF_DEL | --- | 0.164 | R29C40C.C1 to | R29C40C.F1 wb_tlc/intf/SLICE_4283 |
| ROUTE | 1 | 0.000 | R29C40C.F1 to | R29C40C.DI1 wb_tlc/intf/wb_adr_o_32[17] (to clk_125_c) |
| | | 7.352 | (32.0% logic, 68.0% route), 16 logic levels. | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_arb/SLICE_6335:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R30C43A.CLK clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4283:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R29C40C.CLK clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | |

Passed: The following path meets requirements by 0.583ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q wb_arb/s5_sel (from clk_125_c +)
Destination: FF Data in wb_tlc/intf/wb_adr_o_1[20] (to clk_125_c +)

Delay: 7.349ns (32.8% logic, 67.2% route), 18 logic levels.

Constraint Details:

7.349ns physical path delay wb_arb/SLICE_6335 to wb_tlc/intf/SLICE_4285 meets
8.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 7.932ns) by 0.583ns

Physical Path Details:

Data path wb_arb/SLICE_6335 to wb_tlc/intf/SLICE_4285:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 | R30C43A.CLK to | R30C43A.Q0 wb_arb/SLICE_6335 (from clk_125_c) |
| ROUTE | 22 | 0.537 | R30C43A.Q0 to | R30C42D.C1 wb_arb.s5_sel |
| CTOF_DEL | --- | 0.164 | R30C42D.C1 to | R30C42D.F1 wb_arb/SLICE_7625 |
| ROUTE | 3 | 0.592 | R30C42D.F1 to | R30C44C.D1 wb_arb/s0_cyc_o20[0] |
| CTOF_DEL | --- | 0.164 | R30C44C.D1 to | R30C44C.F1 SLICE_6960 |
| ROUTE | 1 | 0.342 | R30C44C.F1 to | R30C44C.D0 wb_arb/s_ack_12_iv_0_0 |
| CTOF_DEL | --- | 0.164 | R30C44C.D0 to | R30C44C.F0 SLICE_6960 |
| ROUTE | 1 | 1.031 | R30C44C.F0 to | R29C40B.B0 wb_arb/s_ack_12_iv_0_3 |
| CTOF_DEL | --- | 0.164 | R29C40B.B0 to | R29C40B.F0 SLICE_4827 |
| ROUTE | 7 | 0.899 | R29C40B.F0 to | R23C39D.D0 reveal_ist_131 |

```
CTOF_DEL    ---     0.164     R23C39D.D0 to     R23C39D.F0 wb_tlc/intf/SLICE_6972
ROUTE         1     0.803     R23C39D.F0 to     R23C37A.B0 wb_tlc/intf/un1_sm_10_i
C0TOFCO_DE  ---     0.423     R23C37A.B0 to    R23C37A.FCO wb_tlc/intf/SLICE_361
ROUTE         1     0.000    R23C37A.FCO to    R23C37B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_0
FCITOFCO_D  ---     0.064    R23C37B.FCI to    R23C37B.FCO wb_tlc/intf/SLICE_362
ROUTE         1     0.000    R23C37B.FCO to    R23C37C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_2
FCITOFCO_D  ---     0.064    R23C37C.FCI to    R23C37C.FCO wb_tlc/intf/SLICE_363
ROUTE         1     0.000    R23C37C.FCO to    R23C38A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_4
FCITOFCO_D  ---     0.064    R23C38A.FCI to    R23C38A.FCO wb_tlc/intf/SLICE_364
ROUTE         1     0.000    R23C38A.FCO to    R23C38B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_6
FCITOFCO_D  ---     0.064    R23C38B.FCI to    R23C38B.FCO wb_tlc/intf/SLICE_365
ROUTE         1     0.000    R23C38B.FCO to    R23C38C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_8
FCITOFCO_D  ---     0.064    R23C38C.FCI to    R23C38C.FCO wb_tlc/intf/SLICE_366
ROUTE         1     0.000    R23C38C.FCO to    R23C39A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_10
FCITOFCO_D  ---     0.064    R23C39A.FCI to    R23C39A.FCO wb_tlc/intf/SLICE_367
ROUTE         1     0.000    R23C39A.FCO to    R23C39B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_12
FCITOFCO_D  ---     0.064    R23C39B.FCI to    R23C39B.FCO wb_tlc/intf/SLICE_368
ROUTE         1     0.000    R23C39B.FCO to    R23C39C.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_14
FCITOFCO_D  ---     0.064    R23C39C.FCI to    R23C39C.FCO wb_tlc/intf/SLICE_369
ROUTE         1     0.000    R23C39C.FCO to    R23C40A.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_16
FCITOFCO_D  ---     0.064    R23C40A.FCI to    R23C40A.FCO wb_tlc/intf/SLICE_370
ROUTE         1     0.000    R23C40A.FCO to    R23C40B.FCI wb_tlc/intf/un1_wb_adr_o_4_cry_18
FCITOF0_DE  ---     0.149     R23C40B.FCI to     R23C40B.F0 wb_tlc/intf/SLICE_371
ROUTE         1     0.738     R23C40B.F0 to     R22C38C.C0 wb_tlc/intf/un1_wb_adr_o_4_cry_19_0_S0
CTOF_DEL    ---     0.164     R22C38C.C0 to     R22C38C.F0 wb_tlc/intf/SLICE_4285
ROUTE         1     0.000     R22C38C.F0 to    R22C38C.DI0 wb_tlc/intf/wb_adr_o_32[20] (to clk_125_c)
                  --------
                    7.349   (32.8% logic, 67.2% route), 18 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_arb/SLICE_6335:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C43A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4285:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C38C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Report:  132.031MHz is the maximum frequency for this preference.


================================================================================
Preference: FREQUENCY NET "can_clk_c" 25.000000 MHz ;
            4096 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 1.450ns (weighted slack = 7.250ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in       can/i_can_registers/TX_DATA_REG6/data_out[3]  (to can_clk_c +)
                   FF                       can/i_can_registers/TX_DATA_REG6/data_out[2]

   Delay:               6.253ns  (12.3% logic, 87.7% route), 4 logic levels.

 Constraint Details:

      6.253ns physical path delay SLICE_4320 to can/i_can_registers/TX_DATA_REG6/SLICE_1816 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.297ns CE_SET requirement (totaling 7.703ns) by 1.450ns

 Physical Path Details:

      Data path SLICE_4320 to can/i_can_registers/TX_DATA_REG6/SLICE_1816:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     0.911     R22C42C.Q0 to     R24C45B.C1 reveal_ist_135
CTOF_DEL    ---     0.164     R24C45B.C1 to     R24C45B.F1 can/i_can_registers/SLICE_7258
ROUTE         9     1.938     R24C45B.F1 to     R13C49D.C1 can/i_can_registers/N_654
CTOF_DEL    ---     0.164     R13C49D.C1 to     R13C49D.F1 can/i_can_registers/SLICE_7055
ROUTE         4     1.251     R13C49D.F1 to     R13C50D.D1 can/i_can_registers/N_658
CTOF_DEL    ---     0.164     R13C50D.D1 to     R13C50D.F1 can/i_can_registers/SLICE_7272
ROUTE         4     1.386     R13C50D.F1 to     R12C50A.CE can/i_can_registers/we_tx_data_6 (to can_clk_c)
                  --------
                    6.253   (12.3% logic, 87.7% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/i_can_registers/TX_DATA_REG6/SLICE_1816:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.314 *_R53C70.CLKOP to    R12C50A.CLK can_clk_c
                  --------
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                  --------
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:


Passed: The following path meets requirements by 1.450ns (weighted slack = 7.250ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in       can/i_can_registers/TX_DATA_REG6/data_out[7]  (to can_clk_c +)
                   FF                       can/i_can_registers/TX_DATA_REG6/data_out[6]

   Delay:               6.253ns  (12.3% logic, 87.7% route), 4 logic levels.

 Constraint Details:

      6.253ns physical path delay SLICE_4320 to can/i_can_registers/TX_DATA_REG6/SLICE_1818 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.297ns CE_SET requirement (totaling 7.703ns) by 1.450ns

 Physical Path Details:

      Data path SLICE_4320 to can/i_can_registers/TX_DATA_REG6/SLICE_1818:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     0.911     R22C42C.Q0 to     R24C45B.C1 reveal_ist_135
CTOF_DEL    ---     0.164     R24C45B.C1 to     R24C45B.F1 can/i_can_registers/SLICE_7258
ROUTE         9     1.938     R24C45B.F1 to     R13C49D.C1 can/i_can_registers/N_654
CTOF_DEL    ---     0.164     R13C49D.C1 to     R13C49D.F1 can/i_can_registers/SLICE_7055
ROUTE         4     1.251     R13C49D.F1 to     R13C50D.D1 can/i_can_registers/N_658
CTOF_DEL    ---     0.164     R13C50D.D1 to     R13C50D.F1 can/i_can_registers/SLICE_7272
ROUTE         4     1.386     R13C50D.F1 to     R12C50B.CE can/i_can_registers/we_tx_data_6 (to can_clk_c)
                  --------
                    6.253   (12.3% logic, 87.7% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/i_can_registers/TX_DATA_REG6/SLICE_1818:
```

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.314 *_R53C70.CLKOP to    R12C50B.CLK can_clk_c
                  --------
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                  --------
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:


Passed: The following path meets requirements by 1.642ns (weighted slack = 8.210ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_tlc/intf/wb_adr_o_1[0]  (from clk_125_c +)
   Destination:    FF         Data in        can/data_out[1]  (to can_clk_c +)

   Delay:               6.290ns  (25.3% logic, 74.7% route), 7 logic levels.

 Constraint Details:

      6.290ns physical path delay wb_tlc/intf/SLICE_4275 to can/SLICE_1841 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 1.642ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_4275 to can/SLICE_1841:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R23C42C.CLK to     R23C42C.Q0 wb_tlc/intf/SLICE_4275 (from clk_125_c)
ROUTE        67     0.901     R23C42C.Q0 to     R22C45C.B0 pcie_adr[0]
CTOF_DEL    ---     0.164     R22C45C.B0 to     R22C45C.F0 SLICE_4797
ROUTE       124     1.220     R22C45C.F0 to     R21C52D.A0 msi_adr[0]
CTOF_DEL    ---     0.164     R21C52D.A0 to     R21C52D.F0 can/i_can_registers/SLICE_8909
ROUTE         1     0.931     R21C52D.F0 to     R22C49A.C1 can/i_can_registers/data_out_57_bm_1[1]
CTOOFX_DEL  ---     0.338     R22C49A.C1 to   R22C49A.OFX0 can/i_can_registers/data_out_57[1]/SLICE_6640
ROUTE         1     0.000   R22C49A.OFX0 to    R22C49A.FXB can/i_can_registers/N_890
FXTOOFX_DE  ---     0.146    R22C49A.FXB to   R22C49A.OFX1 can/i_can_registers/data_out_57[1]/SLICE_6640
ROUTE         1     1.078   R22C49A.OFX1 to     R24C48D.B1 can/i_can_registers/N_898
CTOOFX_DEL  ---     0.338     R24C48D.B1 to   R24C48D.OFX0 can/i_can_registers/data_out_83[1]/SLICE_6597
ROUTE         1     0.571   R24C48D.OFX0 to     R24C46A.D1 can/data_out_regs[1]
CTOF_DEL    ---     0.164     R24C46A.D1 to     R24C46A.F1 can/SLICE_1841
ROUTE         1     0.000     R24C46A.F1 to    R24C46A.DI1 can/N_276_i (to can_clk_c)
                  --------
                    6.290   (25.3% logic, 74.7% route), 7 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4275:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C42C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/SLICE_1841:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.314 *_R53C70.CLKOP to    R24C46A.CLK can_clk_c
                  --------
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                  --------
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:


Passed: The following path meets requirements by 1.685ns (weighted slack = 8.425ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in        can/i_can_registers/TX_DATA_REG6/data_out[1]  (to can_clk_c +)
                   FF                        can/i_can_registers/TX_DATA_REG6/data_out[0]

   Delay:               6.018ns  (12.7% logic, 87.3% route), 4 logic levels.

 Constraint Details:

      6.018ns physical path delay SLICE_4320 to can/i_can_registers/TX_DATA_REG6/SLICE_1815 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.297ns CE_SET requirement (totaling 7.703ns) by 1.685ns

 Physical Path Details:

      Data path SLICE_4320 to can/i_can_registers/TX_DATA_REG6/SLICE_1815:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     0.911     R22C42C.Q0 to     R24C45B.C1 reveal_ist_135
CTOF_DEL    ---     0.164     R24C45B.C1 to     R24C45B.F1 can/i_can_registers/SLICE_7258
ROUTE         9     1.938     R24C45B.F1 to     R13C49D.C1 can/i_can_registers/N_654
CTOF_DEL    ---     0.164     R13C49D.C1 to     R13C49D.F1 can/i_can_registers/SLICE_7055
ROUTE         4     1.251     R13C49D.F1 to     R13C50D.D1 can/i_can_registers/N_658
CTOF_DEL    ---     0.164     R13C50D.D1 to     R13C50D.F1 can/i_can_registers/SLICE_7272
ROUTE         4     1.151     R13C50D.F1 to     R12C47B.CE can/i_can_registers/we_tx_data_6 (to can_clk_c)
                  --------
                    6.018   (12.7% logic, 87.3% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/i_can_registers/TX_DATA_REG6/SLICE_1815:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.314 *_R53C70.CLKOP to    R12C47B.CLK can_clk_c
                  --------
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                  --------
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:


Passed: The following path meets requirements by 1.825ns (weighted slack = 9.125ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in        can/i_can_registers/TX_DATA_REG6/data_out[5]  (to can_clk_c +)
                   FF                        can/i_can_registers/TX_DATA_REG6/data_out[4]

   Delay:               5.878ns  (13.0% logic, 87.0% route), 4 logic levels.
```

```
 Constraint Details:

      5.878ns physical path delay SLICE_4320 to can/i_can_registers/TX_DATA_REG6/SLICE_1817 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.297ns CE_SET requirement (totaling 7.703ns) by 1.825ns

 Physical Path Details:

      Data path SLICE_4320 to can/i_can_registers/TX_DATA_REG6/SLICE_1817:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     0.911     R22C42C.Q0 to     R24C45B.C1 reveal_ist_135
CTOF_DEL    ---     0.164     R24C45B.C1 to     R24C45B.F1 can/i_can_registers/SLICE_7258
ROUTE         9     1.938     R24C45B.F1 to     R13C49D.C1 can/i_can_registers/N_654
CTOF_DEL    ---     0.164     R13C49D.C1 to     R13C49D.F1 can/i_can_registers/SLICE_7055
ROUTE         4     1.251     R13C49D.F1 to     R13C50D.D1 can/i_can_registers/N_658
CTOF_DEL    ---     0.164     R13C50D.D1 to     R13C50D.F1 can/i_can_registers/SLICE_7272
ROUTE         4     1.011     R13C50D.F1 to     R12C46A.CE can/i_can_registers/we_tx_data_6 (to can_clk_c)
                  --------
                    5.878   (13.0% logic, 87.0% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/i_can_registers/TX_DATA_REG6/SLICE_1817:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.314 *_R53C70.CLKOP to    R12C46A.CLK can_clk_c
                  --------
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                  --------
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:


Passed: The following path meets requirements by 1.825ns (weighted slack = 9.125ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in       can/i_can_bsp/tx_err_cnt[8]  (to can_clk_c +)

   Delay:               6.107ns  (15.2% logic, 84.8% route), 5 logic levels.

 Constraint Details:

      6.107ns physical path delay SLICE_4320 to can/i_can_bsp/SLICE_1689 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 1.825ns

 Physical Path Details:

      Data path SLICE_4320 to can/i_can_bsp/SLICE_1689:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     0.921     R22C42C.Q0 to     R19C43A.D1 reveal_ist_135
CTOF_DEL    ---     0.164     R19C43A.D1 to     R19C43A.F1 SLICE_4798
ROUTE        33     0.861     R19C43A.F1 to     R24C44A.D1 msi_adr[3]
CTOF_DEL    ---     0.164     R24C44A.D1 to     R24C44A.F1 can/SLICE_7163
ROUTE        11     1.023     R24C44A.F1 to     R19C41D.C1 can/N_699
CTOF_DEL    ---     0.164     R19C41D.C1 to     R19C41D.F1 can/SLICE_7168
ROUTE        12     2.371     R19C41D.F1 to     R16C56C.B0 can/we_tx_err_cnt
CTOF_DEL    ---     0.164     R16C56C.B0 to     R16C56C.F0 can/i_can_bsp/SLICE_1689
ROUTE         1     0.000     R16C56C.F0 to    R16C56C.DI0 can/i_can_bsp/tx_err_cnt_7[8] (to can_clk_c)
                  --------
                    6.107   (15.2% logic, 84.8% route), 5 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/i_can_bsp/SLICE_1689:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.314 *_R53C70.CLKOP to    R16C56C.CLK can_clk_c
                  --------
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                  --------
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:


Passed: The following path meets requirements by 1.826ns (weighted slack = 9.130ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_tlc/intf/wb_adr_o_1[0]  (from clk_125_c +)
   Destination:    FF         Data in       can/data_out[0]  (to can_clk_c +)

   Delay:               6.106ns  (23.5% logic, 76.5% route), 7 logic levels.

 Constraint Details:

      6.106ns physical path delay wb_tlc/intf/SLICE_4275 to can/SLICE_1525 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 1.826ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_4275 to can/SLICE_1525:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R23C42C.CLK to     R23C42C.Q0 wb_tlc/intf/SLICE_4275 (from clk_125_c)
ROUTE        67     0.901     R23C42C.Q0 to     R22C45C.B0 pcie_adr[0]
CTOF_DEL    ---     0.164     R22C45C.B0 to     R22C45C.F0 SLICE_4797
ROUTE       124     0.910     R22C45C.F0 to     R19C46A.C0 msi_adr[0]
CTOF_DEL    ---     0.164     R19C46A.C0 to     R19C46A.F0 can/i_can_registers/SLICE_8900
ROUTE         1     1.082     R19C46A.F0 to     R23C46D.B1 can/i_can_registers/N_641
CTOF_DEL    ---     0.164     R23C46D.B1 to     R23C46D.F1 can/i_can_registers/SLICE_7264
ROUTE         1     0.406     R23C46D.F1 to     R23C46D.A0 can/i_can_registers/N_673_0
CTOF_DEL    ---     0.164     R23C46D.A0 to     R23C46D.F0 can/i_can_registers/SLICE_7264
ROUTE         1     0.803     R23C46D.F0 to     R23C47D.B0 can/i_can_registers/N_697
CTOOFX_DEL  ---     0.338     R23C47D.B0 to   R23C47D.OFX0 can/i_can_registers/data_out_83[0]/SLICE_6593
ROUTE         1     0.571   R23C47D.OFX0 to     R23C45B.D1 can/data_out_regs[0]
CTOF_DEL    ---     0.164     R23C45B.D1 to     R23C45B.F1 can/SLICE_1525
ROUTE         1     0.000     R23C45B.F1 to    R23C45B.DI1 can/N_272_i (to can_clk_c)
                  --------
                    6.106   (23.5% logic, 76.5% route), 7 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4275:
```

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C42C.CLK clk_125_c
                    --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/SLICE_1525:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.314 *_R53C70.CLKOP to    R23C45B.CLK can_clk_c
                    --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

     Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                    --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:


Passed: The following path meets requirements by 1.829ns (weighted slack = 9.145ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_tlc/intf/wb_adr_o_1[0]  (from clk_125_c +)
   Destination:    FF         Data in        can/data_out[7]  (to can_clk_c +)

   Delay:               6.103ns  (25.6% logic, 74.4% route), 7 logic levels.

 Constraint Details:

     6.103ns physical path delay wb_tlc/intf/SLICE_4275 to can/SLICE_1841 meets
     8.000ns delay constraint less
    -1.466ns skew and
     1.466ns feedback compensation and
     0.068ns DIN_SET requirement (totaling 7.932ns) by 1.829ns

 Physical Path Details:

     Data path wb_tlc/intf/SLICE_4275 to can/SLICE_1841:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R23C42C.CLK to     R23C42C.Q0 wb_tlc/intf/SLICE_4275 (from clk_125_c)
ROUTE        67     0.901     R23C42C.Q0 to     R22C45C.B0 pcie_adr[0]
CTOF_DEL    ---     0.164     R22C45C.B0 to     R22C45C.F0 SLICE_4797
ROUTE       124     0.891     R22C45C.F0 to     R23C43A.B1 msi_adr[0]
C1TOFCO_DE  ---     0.310     R23C43A.B1 to    R23C43A.FCO can/i_can_bsp/i_can_fifo/SLICE_25
ROUTE         1     0.000    R23C43A.FCO to    R23C43B.FCI can/i_can_bsp/i_can_fifo/un1_rd_pointer_0_cry_0
FCITOF0_DE  ---     0.149    R23C43B.FCI to     R23C43B.F0 can/i_can_bsp/i_can_fifo/SLICE_26
ROUTE        32     1.131     R23C43B.F0 to     R21C46B.B1 can/i_can_bsp/i_can_fifo/un1_rd_pointer_0_cry_1_0_S0
CTOF_DEL    ---     0.164     R21C46B.B1 to     R21C46B.F1 can/i_can_bsp/i_can_fifo/fifo_ram_2/SLICE_1144
ROUTE         1     0.852     R21C46B.F1 to     R25C46D.C1 can/i_can_bsp/i_can_fifo/fifo_ram_14
CTOOFX_DEL  ---     0.338     R25C46D.C1 to   R25C46D.OFX0 can/i_can_bsp/i_can_fifo/un1_rd_pointer_0_cry_3_0_RNIFABT1/SLICE_6509
ROUTE         1     0.764   R25C46D.OFX0 to     R24C46A.D0 can/data_out_fifo[7]
CTOF_DEL    ---     0.164     R24C46A.D0 to     R24C46A.F0 can/SLICE_1841
ROUTE         1     0.000     R24C46A.F0 to    R24C46A.DI0 can/N_288_i (to can_clk_c)
                    --------
                     6.103   (25.6% logic, 74.4% route), 7 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4275:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C42C.CLK clk_125_c
                    --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/SLICE_1841:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.314 *_R53C70.CLKOP to    R24C46A.CLK can_clk_c
                    --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

     Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                    --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:


Passed: The following path meets requirements by 1.838ns (weighted slack = 9.190ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_tlc/intf/wb_adr_o_1[0]  (from clk_125_c +)
   Destination:    FF         Data in        can/data_out[6]  (to can_clk_c +)

   Delay:               6.094ns  (25.7% logic, 74.3% route), 7 logic levels.

 Constraint Details:

     6.094ns physical path delay wb_tlc/intf/SLICE_4275 to can/SLICE_1840 meets
     8.000ns delay constraint less
    -1.466ns skew and
     1.466ns feedback compensation and
     0.068ns DIN_SET requirement (totaling 7.932ns) by 1.838ns

 Physical Path Details:

     Data path wb_tlc/intf/SLICE_4275 to can/SLICE_1840:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R23C42C.CLK to     R23C42C.Q0 wb_tlc/intf/SLICE_4275 (from clk_125_c)
ROUTE        67     0.901     R23C42C.Q0 to     R22C45C.B0 pcie_adr[0]
CTOF_DEL    ---     0.164     R22C45C.B0 to     R22C45C.F0 SLICE_4797
ROUTE       124     0.891     R22C45C.F0 to     R23C43A.B1 msi_adr[0]
C1TOFCO_DE  ---     0.310     R23C43A.B1 to    R23C43A.FCO can/i_can_bsp/i_can_fifo/SLICE_25
ROUTE         1     0.000    R23C43A.FCO to    R23C43B.FCI can/i_can_bsp/i_can_fifo/un1_rd_pointer_0_cry_0
FCITOF0_DE  ---     0.149    R23C43B.FCI to     R23C43B.F0 can/i_can_bsp/i_can_fifo/SLICE_26
ROUTE        32     1.092     R23C43B.F0 to     R25C45B.B0 can/i_can_bsp/i_can_fifo/un1_rd_pointer_0_cry_1_0_S0
CTOF_DEL    ---     0.164     R25C45B.B0 to     R25C45B.F0 can/i_can_bsp/i_can_fifo/fifo_ram_4/SLICE_1138
ROUTE         1     0.843     R25C45B.F0 to     R22C44A.B0 can/i_can_bsp/i_can_fifo/fifo_ram_21
CTOOFX_DEL  ---     0.338     R22C44A.B0 to   R22C44A.OFX0 can/i_can_bsp/i_can_fifo/un1_rd_pointer_0_cry_3_0_RNIFABT1_0/SLICE_6508
ROUTE         1     0.803   R22C44A.OFX0 to     R22C45B.B1 can/data_out_fifo[6]
CTOF_DEL    ---     0.164     R22C45B.B1 to     R22C45B.F1 can/SLICE_1840
ROUTE         1     0.000     R22C45B.F1 to    R22C45B.DI1 can/N_286_i (to can_clk_c)
                    --------
                     6.094   (25.7% logic, 74.3% route), 7 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4275:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R23C42C.CLK clk_125_c
                    --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/SLICE_1840:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.314 *_R53C70.CLKOP to    R22C45B.CLK can_clk_c
                    --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

     Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                    --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.
```

PLL_R53C70.CLKOP attributes:


Passed: The following path meets requirements by 1.842ns (weighted slack = 9.210ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in        can/i_can_bsp/node_bus_off  (to can_clk_c +)

   Delay:               5.861ns  (21.5% logic, 78.5% route), 7 logic levels.

 Constraint Details:

      5.861ns physical path delay SLICE_4320 to can/i_can_bsp/SLICE_1746 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.297ns CE_SET requirement (totaling 7.703ns) by 1.842ns

 Physical Path Details:

      Data path SLICE_4320 to can/i_can_bsp/SLICE_1746:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     0.921     R22C42C.Q0 to     R19C43A.D1 reveal_ist_135
CTOF_DEL    ---     0.164     R19C43A.D1 to     R19C43A.F1 SLICE_4798
ROUTE        33     0.861     R19C43A.F1 to     R24C44A.D1 msi_adr[3]
CTOF_DEL    ---     0.164     R24C44A.D1 to     R24C44A.F1 can/SLICE_7163
ROUTE        11     1.023     R24C44A.F1 to     R19C41D.C1 can/N_699
CTOF_DEL    ---     0.164     R19C41D.C1 to     R19C41D.F1 can/SLICE_7168
ROUTE        12     0.358     R19C41D.F1 to     R19C41D.D0 can/we_tx_err_cnt
CTOF_DEL    ---     0.164     R19C41D.D0 to     R19C41D.F0 can/SLICE_7168
ROUTE         1     0.798     R19C41D.F0 to     R16C43C.C0 can/i_can_bsp/un1_we_tx_err_cnt
CTOF_DEL    ---     0.164     R16C43C.C0 to     R16C43C.F0 can/i_can_bsp/SLICE_1746
ROUTE         2     0.287     R16C43C.F0 to     R16C43C.C1 can/i_can_bsp/un1_bit_err_19_2
CTOF_DEL    ---     0.164     R16C43C.C1 to     R16C43C.F1 can/i_can_bsp/SLICE_1746
ROUTE         1     0.354     R16C43C.F1 to     R16C43C.CE can/i_can_bsp/un1_bit_err_19_i (to can_clk_c)
                  --------
                    5.861   (21.5% logic, 78.5% route), 7 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to can/i_can_bsp/SLICE_1746:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to *L_R53C70.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 *L_R53C70.CLKI to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.314 *_R53C70.CLKOP to    R16C43C.CLK can_clk_c
                  --------
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *_R53C70.CLKFB to *_R53C70.CLKOP pll_can/PLLInst_0
ROUTE       399     1.466 *_R53C70.CLKOP to *_R53C70.CLKFB can_clk_c
                  --------
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C70.CLKOP attributes:

Report:   30.534MHz is the maximum frequency for this preference.


================================================================================
Preference: FREQUENCY NET "uart_clk_c" 25.000000 MHz ;
            4096 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 2.975ns (weighted slack = 14.875ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_tlc/intf/wb_sel_o_0[1]  (from clk_125_c +)
   Destination:    FF         Data in        uart3/regs/dl[15]  (to uart_clk_c +)

   Delay:               4.880ns  (9.0% logic, 91.0% route), 2 logic levels.

 Constraint Details:

      4.880ns physical path delay wb_tlc/intf/SLICE_4297 to uart3/regs/SLICE_5612 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 2.975ns

 Physical Path Details:

      Data path wb_tlc/intf/SLICE_4297 to uart3/regs/SLICE_5612:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R25C39A.CLK to     R25C39A.Q1 wb_tlc/intf/SLICE_4297 (from clk_125_c)
ROUTE        30     1.217     R25C39A.Q1 to     R24C34B.C1 pcie_sel[1]
CTOF_DEL    ---     0.164     R24C34B.C1 to     R24C34B.F1 SLICE_5248
ROUTE        25     3.224     R24C34B.F1 to     R33C62B.M1 I_1014.t1 (to uart_clk_c)
                  --------
                    4.880   (9.0% logic, 91.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to wb_tlc/intf/SLICE_4297:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R25C39A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart3/regs/SLICE_5612:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R33C62B.CLK uart_clk_c
                  --------
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                  --------
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 2.976ns (weighted slack = 14.880ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in        uart3/regs/dl[15]  (to uart_clk_c +)

   Delay:               4.879ns  (9.0% logic, 91.0% route), 2 logic levels.

 Constraint Details:

      4.879ns physical path delay SLICE_4320 to uart3/regs/SLICE_5612 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 2.976ns

 Physical Path Details:

      Data path SLICE_4320 to uart3/regs/SLICE_5612:

   Name    Fanout   Delay (ns)          Site               Resource

```
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     1.216     R22C42C.Q0 to     R24C34B.A1 reveal_ist_135
CTOF_DEL    ---     0.164     R24C34B.A1 to     R24C34B.F1 SLICE_5248
ROUTE        25     3.224     R24C34B.F1 to     R33C62B.M1 I_1014.t1 (to uart_clk_c)
                   --------
                     4.879   (9.0% logic, 91.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart3/regs/SLICE_5612:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R33C62B.CLK uart_clk_c
                   --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                   --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 2.986ns (weighted slack = 14.930ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in        uart3/regs/mcr[4]  (to uart_clk_c +)

   Delay:               4.869ns  (9.0% logic, 91.0% route), 2 logic levels.

 Constraint Details:

      4.869ns physical path delay SLICE_4320 to uart3/regs/SLICE_5676 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 2.986ns

 Physical Path Details:

      Data path SLICE_4320 to uart3/regs/SLICE_5676:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     1.433     R22C42C.Q0 to     R23C34C.B0 reveal_ist_135
CTOF_DEL    ---     0.164     R23C34C.B0 to     R23C34C.F0 SLICE_5247
ROUTE        25     2.997     R23C34C.F0 to     R34C62B.M0 I_1011.t1 (to uart_clk_c)
                   --------
                     4.869   (9.0% logic, 91.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart3/regs/SLICE_5676:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R34C62B.CLK uart_clk_c
                   --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                   --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 2.986ns (weighted slack = 14.930ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in        uart3/regs/scratch[4]  (to uart_clk_c +)

   Delay:               4.869ns  (9.0% logic, 91.0% route), 2 logic levels.

 Constraint Details:

      4.869ns physical path delay SLICE_4320 to uart3/regs/SLICE_5729 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 2.986ns

 Physical Path Details:

      Data path SLICE_4320 to uart3/regs/SLICE_5729:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     1.433     R22C42C.Q0 to     R23C34C.B0 reveal_ist_135
CTOF_DEL    ---     0.164     R23C34C.B0 to     R23C34C.F0 SLICE_5247
ROUTE        25     2.997     R23C34C.F0 to     R34C62A.M0 I_1011.t1 (to uart_clk_c)
                   --------
                     4.869   (9.0% logic, 91.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart3/regs/SLICE_5729:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R34C62A.CLK uart_clk_c
                   --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                   --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 2.997ns (weighted slack = 14.985ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in        uart3/regs/lcr[5]  (to uart_clk_c +)
```

```
   Delay:               4.935ns  (12.2% logic, 87.8% route), 3 logic levels.

 Constraint Details:

      4.935ns physical path delay SLICE_4320 to uart3/regs/SLICE_5656 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 2.997ns

 Physical Path Details:

      Data path SLICE_4320 to uart3/regs/SLICE_5656:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     1.433     R22C42C.Q0 to     R23C34C.B1 reveal_ist_135
CTOF_DEL    ---     0.164     R23C34C.B1 to     R23C34C.F1 SLICE_5247
ROUTE        21     2.899     R23C34C.F1 to     R34C63C.A1 I_1012.t1
CTOF_DEL    ---     0.164     R34C63C.A1 to     R34C63C.F1 uart3/regs/SLICE_5656
ROUTE         1     0.000     R34C63C.F1 to    R34C63C.DI1 uart3/regs/lcr_4[5] (to uart_clk_c)
                  --------
                    4.935   (12.2% logic, 87.8% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart3/regs/SLICE_5656:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R34C63C.CLK uart_clk_c
                  --------
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                  --------
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 3.024ns (weighted slack = 15.120ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in       uart3/regs/lcr[2]  (to uart_clk_c +)

   Delay:               4.908ns  (12.3% logic, 87.7% route), 3 logic levels.

 Constraint Details:

      4.908ns physical path delay SLICE_4320 to uart3/regs/SLICE_5655 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 3.024ns

 Physical Path Details:

      Data path SLICE_4320 to uart3/regs/SLICE_5655:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     1.460     R22C42C.Q0 to     R23C34B.A0 reveal_ist_135
CTOF_DEL    ---     0.164     R23C34B.A0 to     R23C34B.F0 SLICE_5246
ROUTE        33     2.845     R23C34B.F0 to     R34C63A.D0 I_1009.t1
CTOF_DEL    ---     0.164     R34C63A.D0 to     R34C63A.F0 uart3/regs/SLICE_5655
ROUTE         1     0.000     R34C63A.F0 to    R34C63A.DI0 uart3/regs/lcr_4[2] (to uart_clk_c)
                  --------
                    4.908   (12.3% logic, 87.7% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart3/regs/SLICE_5655:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R34C63A.CLK uart_clk_c
                  --------
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                  --------
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 3.026ns (weighted slack = 15.130ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in       uart3/regs/dl[5]  (to uart_clk_c +)

   Delay:               4.829ns  (9.1% logic, 90.9% route), 2 logic levels.

 Constraint Details:

      4.829ns physical path delay SLICE_4320 to uart3/regs/SLICE_5607 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.145ns M_SET requirement (totaling 7.855ns) by 3.026ns

 Physical Path Details:

      Data path SLICE_4320 to uart3/regs/SLICE_5607:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     1.433     R22C42C.Q0 to     R23C34C.B1 reveal_ist_135
CTOF_DEL    ---     0.164     R23C34C.B1 to     R23C34C.F1 SLICE_5247
ROUTE        21     2.957     R23C34C.F1 to     R33C59B.M1 I_1012.t1 (to uart_clk_c)
                  --------
                    4.829   (9.1% logic, 90.9% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart3/regs/SLICE_5607:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R33C59B.CLK uart_clk_c
                  --------
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.
```

```
PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                    --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 3.071ns (weighted slack = 15.355ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in       uart3/regs/lcr[6]  (to uart_clk_c +)

   Delay:               4.861ns  (12.4% logic, 87.6% route), 3 logic levels.

 Constraint Details:

      4.861ns physical path delay SLICE_4320 to uart3/regs/SLICE_5657 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 3.071ns

 Physical Path Details:

      Data path SLICE_4320 to uart3/regs/SLICE_5657:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     1.216     R22C42C.Q0 to     R24C34B.A0 reveal_ist_135
CTOF_DEL    ---     0.164     R24C34B.A0 to     R24C34B.F0 SLICE_5248
ROUTE        25     3.042     R24C34B.F0 to     R33C63C.B0 I_1013.t1
CTOF_DEL    ---     0.164     R33C63C.B0 to     R33C63C.F0 uart3/regs/SLICE_5657
ROUTE         1     0.000     R33C63C.F0 to    R33C63C.DI0 uart3/regs/lcr_4[6] (to uart_clk_c)
                    --------
                     4.861   (12.4% logic, 87.6% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                    --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart3/regs/SLICE_5657:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R33C63C.CLK uart_clk_c
                    --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                    --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 3.074ns (weighted slack = 15.370ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in       uart3/regs/ier[3]  (to uart_clk_c +)

   Delay:               4.858ns  (12.4% logic, 87.6% route), 3 logic levels.

 Constraint Details:

      4.858ns physical path delay SLICE_4320 to uart3/regs/SLICE_5649 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 3.074ns

 Physical Path Details:

      Data path SLICE_4320 to uart3/regs/SLICE_5649:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     1.460     R22C42C.Q0 to     R23C34B.A1 reveal_ist_135
CTOF_DEL    ---     0.164     R23C34B.A1 to     R23C34B.F1 SLICE_5246
ROUTE        29     2.795     R23C34B.F1 to     R33C61C.B1 I_1010.t1
CTOF_DEL    ---     0.164     R33C61C.B1 to     R33C61C.F1 uart3/regs/SLICE_5649
ROUTE         1     0.000     R33C61C.F1 to    R33C61C.DI1 uart3/regs/ier_5[3] (to uart_clk_c)
                    --------
                     4.858   (12.4% logic, 87.6% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                    --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart3/regs/SLICE_5649:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R33C61C.CLK uart_clk_c
                    --------
                     2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                    --------
                     1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:


Passed: The following path meets requirements by 3.075ns (weighted slack = 15.375ns)

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             wb_arb/rr[0]  (from clk_125_c +)
   Destination:    FF         Data in       uart3/regs/lcr[4]  (to uart_clk_c +)

   Delay:               4.857ns  (12.4% logic, 87.6% route), 3 logic levels.

 Constraint Details:

      4.857ns physical path delay SLICE_4320 to uart3/regs/SLICE_5656 meets
      8.000ns delay constraint less
     -1.466ns skew and
      1.466ns feedback compensation and
      0.068ns DIN_SET requirement (totaling 7.932ns) by 3.075ns

 Physical Path Details:

      Data path SLICE_4320 to uart3/regs/SLICE_5656:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R22C42C.CLK to     R22C42C.Q0 SLICE_4320 (from clk_125_c)
ROUTE       220     1.433     R22C42C.Q0 to     R23C34C.B0 reveal_ist_135
CTOF_DEL    ---     0.164     R23C34C.B0 to     R23C34C.F0 SLICE_5247
ROUTE        25     2.821     R23C34C.F0 to     R34C63C.B0 I_1011.t1
```

```
CTOF_DEL    ---     0.164     R34C63C.B0 to     R34C63C.F0 uart3/regs/SLICE_5656
ROUTE         1     0.000     R34C63C.F0 to    R34C63C.DI0 uart3/regs/lcr_4[4] (to uart_clk_c)
                  --------
                    4.857   (12.4% logic, 87.6% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to SLICE_4320:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R22C42C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to uart3/regs/SLICE_5656:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.567 *FF_TX_H_CLK_0 to PLL_R53C5.CLKI clk_125_c
CLKI2OP_DE  ---     0.000 PLL_R53C5.CLKI to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.314 *L_R53C5.CLKOP to    R34C63C.CLK uart_clk_c
                  --------
                    2.881   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

      Destination Clock f/b:

   Name    Fanout   Delay (ns)          Site               Resource
CLKFB2OP_D  ---     0.000 *L_R53C5.CLKFB to *L_R53C5.CLKOP pll_uarts/PLLInst_0
ROUTE       999     1.466 *L_R53C5.CLKOP to *L_R53C5.CLKFB uart_clk_c
                  --------
                    1.466   (0.0% logic, 100.0% route), 1 logic levels.

PLL_R53C5.CLKOP attributes:

Report:   39.801MHz is the maximum frequency for this preference.


================================================================================
Preference: FREQUENCY NET "pcie/pclk" 250.000000 MHz ;
            987 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.823ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_lbk_sm/lbk_sloopback  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_pcs_pipe/pipe_top_0/ffc_fb_loopback  (to pcie/pclk +)

   Delay:               3.109ns  (19.4% logic, 80.6% route), 3 logic levels.

 Constraint Details:

      3.109ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_lbk_sm/SLICE_2062 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4224 meets
      4.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 3.932ns) by 0.823ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_lbk_sm/SLICE_2062 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4224:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R28C20C.CLK to     R28C20C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_lbk_sm/SLICE_2062 (from clk_125_c)
ROUTE         1     0.978     R28C20C.Q0 to     R31C28D.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/phy_sloopback
CTOF_DEL    ---     0.164     R31C28D.C0 to     R31C28D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_pipe/SLICE_9733
ROUTE         2     1.528     R31C28D.F0 to     R49C34C.C0 pcie/tx_detect_rx_lb
CTOF_DEL    ---     0.164     R49C34C.C0 to     R49C34C.F0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_4224
ROUTE         1     0.000     R49C34C.F0 to    R49C34C.DI0 pcie/u1_pcs_pipe/pipe_top_0/un1_ffc_fb_loopback_0_a2 (to pcie/pclk)
                  --------
                    3.109   (19.4% logic, 80.6% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_lbk_sm/SLICE_2062:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R28C20C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4224:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to    R49C34C.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.881ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_pntr[1]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/data_out[3]  (to pcie/pclk +)

   Delay:               3.051ns  (25.1% logic, 74.9% route), 4 logic levels.

 Constraint Details:

      3.051ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306 meets
      4.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 3.932ns) by 0.881ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R43C5C.CLK to      R43C5C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 (from pcie/pclk)
ROUTE        24     0.947      R43C5C.Q1 to      R45C5C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_pntr[1]
CTOF_DEL    ---     0.164      R45C5C.B1 to      R45C5C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3310
ROUTE         3     0.603      R45C5C.F1 to      R45C5D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0ror_0
CTOF_DEL    ---     0.164      R45C5D.B0 to      R45C5D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_8116
ROUTE         9     0.734      R45C5D.F0 to      R47C5A.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1ror
CTOF_DEL    ---     0.164      R47C5A.C1 to      R47C5A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306
ROUTE         1     0.000      R47C5A.F1 to     R47C5A.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_2633_i (to pcie/pclk)
                  --------
                    3.051   (25.1% logic, 74.9% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to     R43C5C.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to     R47C5A.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.881ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_pntr[1]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/data_out[2]  (to pcie/pclk +)

   Delay:               3.051ns  (25.1% logic, 74.9% route), 4 logic levels.

 Constraint Details:

      3.051ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306 meets
      4.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 3.932ns) by 0.881ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R43C5C.CLK to      R43C5C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 (from pcie/pclk)
ROUTE        24     0.947      R43C5C.Q1 to      R45C5C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_pntr[1]
CTOF_DEL    ---     0.164      R45C5C.B1 to      R45C5C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3310
```

```
ROUTE         3     0.603      R45C5C.F1 to      R45C5D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0ror_0
CTOF_DEL    ---     0.164      R45C5D.B0 to      R45C5D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_8116
ROUTE         9     0.734      R45C5D.F0 to      R47C5A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1ror
CTOF_DEL    ---     0.164      R47C5A.C0 to      R47C5A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306
ROUTE         1     0.000      R47C5A.F0 to     R47C5A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_2632_i (to pcie/pclk)
                  --------
                    3.051   (25.1% logic, 74.9% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to     R43C5C.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to     R47C5A.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.895ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_pntr[0]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/data_out[3]  (to pcie/pclk +)

   Delay:               3.037ns  (25.3% logic, 74.7% route), 4 logic levels.

 Constraint Details:

      3.037ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306 meets
      4.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 3.932ns) by 0.895ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R43C5C.CLK to      R43C5C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 (from pcie/pclk)
ROUTE        25     0.933      R43C5C.Q0 to      R45C5C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_pntr[0]
CTOF_DEL    ---     0.164      R45C5C.A1 to      R45C5C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3310
ROUTE         3     0.603      R45C5C.F1 to      R45C5D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0ror_0
CTOF_DEL    ---     0.164      R45C5D.B0 to      R45C5D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_8116
ROUTE         9     0.734      R45C5D.F0 to      R47C5A.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1ror
CTOF_DEL    ---     0.164      R47C5A.C1 to      R47C5A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306
ROUTE         1     0.000      R47C5A.F1 to     R47C5A.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_2633_i (to pcie/pclk)
                  --------
                    3.037   (25.3% logic, 74.7% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to     R43C5C.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to     R47C5A.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.895ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_pntr[0]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/data_out[2]  (to pcie/pclk +)

   Delay:               3.037ns  (25.3% logic, 74.7% route), 4 logic levels.

 Constraint Details:

      3.037ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306 meets
      4.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 3.932ns) by 0.895ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R43C5C.CLK to      R43C5C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 (from pcie/pclk)
ROUTE        25     0.933      R43C5C.Q0 to      R45C5C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_pntr[0]
CTOF_DEL    ---     0.164      R45C5C.A1 to      R45C5C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3310
ROUTE         3     0.603      R45C5C.F1 to      R45C5D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0ror_0
CTOF_DEL    ---     0.164      R45C5D.B0 to      R45C5D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_8116
ROUTE         9     0.734      R45C5D.F0 to      R47C5A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1ror
CTOF_DEL    ---     0.164      R47C5A.C0 to      R47C5A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306
ROUTE         1     0.000      R47C5A.F0 to     R47C5A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_2632_i (to pcie/pclk)
                  --------
                    3.037   (25.3% logic, 74.7% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to     R43C5C.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3306:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to     R47C5A.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.937ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_pcs_pipe/pipe_top_0/RxData_chx_reg[7]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_pcs_pipe/pipe_top_0/RxValid_chx  (to pcie/pclk +)

   Delay:               2.766ns  (27.7% logic, 72.3% route), 4 logic levels.

 Constraint Details:

      2.766ns physical path delay pcie/u1_pcs_pipe/pipe_top_0/SLICE_4241 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_1994 meets
      4.000ns delay constraint less
      0.000ns skew and
      0.297ns CE_SET requirement (totaling 3.703ns) by 0.937ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pipe_top_0/SLICE_4241 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_1994:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R59C39C.CLK to     R59C39C.Q1 pcie/u1_pcs_pipe/pipe_top_0/SLICE_4241 (from pcie/pclk)
ROUTE         2     0.643     R59C39C.Q1 to     R59C38A.A1 pcie/u1_pcs_pipe/pipe_top_0/RxData_chx_reg[7]
CTOF_DEL    ---     0.164     R59C38A.A1 to     R59C38A.F1 pcie/u1_pcs_pipe/pipe_top_0/SLICE_7682
ROUTE         1     0.379     R59C38A.F1 to     R59C38A.B0 pcie/u1_pcs_pipe/pipe_top_0/un1_RxValid_chx5_0_a2_0
CTOF_DEL    ---     0.164     R59C38A.B0 to     R59C38A.F0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_7682
ROUTE         1     0.623     R59C38A.F0 to     R57C38D.D0 pcie/u1_pcs_pipe/pipe_top_0/un1_RxValid_chx5_0_a2_6
CTOF_DEL    ---     0.164     R57C38D.D0 to     R57C38D.F0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_7681
ROUTE         1     0.354     R57C38D.F0 to     R57C38A.CE pcie/u1_pcs_pipe/pipe_top_0/un1_RxValid_chx5_0 (to pcie/pclk)
                  --------
                    2.766   (27.7% logic, 72.3% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4241:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to    R59C39C.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.
```

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_1994:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 192 | 1.415 *FF_TX_F_CLK_0 to | R57C38A.CLK | pcie/pclk |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 0.949ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_lbk_sm/lbk_sloopback (from clk_125_c +)
Destination: FF Data in pcie/u1_pcs_pipe/enable_det_ch0 (to pcie/pclk +)

Delay: 2.983ns (20.2% logic, 79.8% route), 3 logic levels.

Constraint Details:

2.983ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_lbk_sm/SLICE_2062 to pcie/u1_pcs_pipe/SLICE_4223 meets
4.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 3.932ns) by 0.949ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_lbk_sm/SLICE_2062 to pcie/u1_pcs_pipe/SLICE_4223:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 R28C20C.CLK to | R28C20C.Q0 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_lbk_sm/SLICE_2062 (from clk_125_c) |
| ROUTE | 1 | 0.978 R28C20C.Q0 to | R31C28D.C0 | pcie/u1_dut/u1_dut/u1_dut/phy_sloopback |
| CTOF_DEL | --- | 0.164 R31C28D.C0 to | R31C28D.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_pipe/SLICE_9733 |
| ROUTE | 2 | 1.402 R31C28D.F0 to | R48C34A.D0 | pcie/tx_detect_rx_lb |
| CTOF_DEL | --- | 0.164 R48C34A.D0 to | R48C34A.F0 | pcie/u1_pcs_pipe/SLICE_4223 |
| ROUTE | 1 | 0.000 R48C34A.F0 to | R48C34A.DI0 | pcie/u1_pcs_pipe/un1_enable_det_ch0_0_a2 (to pcie/pclk) |
| | | 2.983 (20.2% logic, 79.8% route), 3 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_lbk_sm/SLICE_2062:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R28C20C.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/SLICE_4223:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 192 | 1.415 *FF_TX_F_CLK_0 to | R48C34A.CLK | pcie/pclk |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 0.962ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/data_out[2] (from pcie/pclk +)
Destination: FF Data in pcie/u1_pcs_pipe/pipe_top_0/TxData_chx_s[2] (to pcie/pclk +)

Delay: 2.893ns (9.5% logic, 90.5% route), 1 logic levels.

Constraint Details:

2.893ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/SLICE_2002 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4202 meets
4.000ns delay constraint less
0.000ns skew and
0.145ns M_SET requirement (totaling 3.855ns) by 0.962ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/SLICE_2002 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4202:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 R57C5C.CLK to | R57C5C.Q0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/SLICE_2002 (from pcie/pclk) |
| ROUTE | 1 | 2.618 R57C5C.Q0 to | R61C35C.M0 | pcie/txp_data_ln0[2] (to pcie/pclk) |
| | | 2.893 (9.5% logic, 90.5% route), 1 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_scram/SLICE_2002:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 192 | 1.415 *FF_TX_F_CLK_0 to | R57C5C.CLK | pcie/pclk |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4202:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 192 | 1.415 *FF_TX_F_CLK_0 to | R61C35C.CLK | pcie/pclk |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 1.006ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_pntr[1] (from pcie/pclk +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/data_out[8] (to pcie/pclk +)

Delay: 2.926ns (20.6% logic, 79.4% route), 3 logic levels.

Constraint Details:

2.926ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3309 meets
4.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 3.932ns) by 1.006ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3309:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 R43C5C.CLK to | R43C5C.Q1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 (from pcie/pclk) |
| ROUTE | 24 | 1.029 R43C5C.Q1 to | R43C3A.B0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_pntr[1] |
| CTOF_DEL | --- | 0.164 R43C3A.B0 to | R43C3A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1391 |
| ROUTE | 1 | 1.294 R43C3A.F0 to | R45C5B.B0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0rx[8] |
| CTOF_DEL | --- | 0.164 R45C5B.B0 to | R45C5B.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3309 |
| ROUTE | 1 | 0.000 R45C5B.F0 to | R45C5B.DI0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_2636_i (to pcie/pclk) |
| | | 2.926 (20.6% logic, 79.4% route), 3 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 192 | 1.415 *FF_TX_F_CLK_0 to | R43C5C.CLK | pcie/pclk |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3309:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 192 | 1.415 *FF_TX_F_CLK_0 to | R45C5B.CLK | pcie/pclk |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 1.007ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_pntr[1] (from pcie/pclk +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/data_out[1] (to pcie/pclk +)

Delay: 2.925ns (26.2% logic, 73.8% route), 4 logic levels.

Constraint Details:

2.925ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3305 meets
4.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 3.932ns) by 1.007ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3305:

```
   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R43C5C.CLK to      R43C5C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361 (from pcie/pclk)
ROUTE        24     0.947      R43C5C.Q1 to      R45C5C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rd_pntr[1]
CTOF_DEL    ---     0.164      R45C5C.B1 to      R45C5C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3310
ROUTE         3     0.603      R45C5C.F1 to      R45C5D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0ror_0
CTOF_DEL    ---     0.164      R45C5D.B0 to      R45C5D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_8116
ROUTE         9     0.608      R45C5D.F0 to      R47C5C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1ror
CTOF_DEL    ---     0.164      R47C5C.D1 to      R47C5C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3305
ROUTE         1     0.000      R47C5C.F1 to     R47C5C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_2631_i (to pcie/pclk)
                  --------
                    2.925   (26.2% logic, 73.8% route), 4 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3361:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to     R43C5C.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3305:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     1.415 *FF_TX_F_CLK_0 to     R47C5C.CLK pcie/pclk
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Report:  314.762MHz is the maximum frequency for this preference.


================================================================================
Preference: FREQUENCY NET "pcie/u1_pcs_pipe/ff_rx_fclk_0" 250.000000 MHz ;
            1 item scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed:  The following path meets requirements by 1.574ns
         The internal maximum frequency of the following component is 412.201 MHz

 Logical Details:  Cell type  Pin name       Component name

   Destination:    FSLICE     CLK            pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268

   Delay:               2.426ns -- based on Minimum Pulse Width


Passed: The following path meets requirements by 3.251ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_pcs_pipe/pipe_top_0/sync1_RxPolarity  (from pcie/u1_pcs_pipe/ff_rx_fclk_0 +)
   Destination:    FF         Data in        pcie/u1_pcs_pipe/pipe_top_0/sync2_RxPolarity  (to pcie/u1_pcs_pipe/ff_rx_fclk_0 +)

   Delay:               0.604ns  (45.5% logic, 54.5% route), 1 logic levels.

 Constraint Details:

      0.604ns physical path delay pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268 meets
      4.000ns delay constraint less
      0.000ns skew and
      0.145ns M_SET requirement (totaling 3.855ns) by 3.251ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R59C34B.CLK to     R59C34B.Q0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268 (from pcie/u1_pcs_pipe/ff_rx_fclk_0)
ROUTE         1     0.329     R59C34B.Q0 to     R59C34B.M1 pcie/u1_pcs_pipe/pipe_top_0/sync1_RxPolarity (to pcie/u1_pcs_pipe/ff_rx_fclk_0)
                  --------
                    0.604   (45.5% logic, 54.5% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE         1     3.129 *FF_RX_F_CLK_0 to    R59C34B.CLK pcie/u1_pcs_pipe/ff_rx_fclk_0
                  --------
                    3.129   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE         1     3.129 *FF_RX_F_CLK_0 to    R59C34B.CLK pcie/u1_pcs_pipe/ff_rx_fclk_0
                  --------
                    3.129   (0.0% logic, 100.0% route), 0 logic levels.

Report:  412.201MHz is the maximum frequency for this preference.


================================================================================
Preference: BLOCK PATH FROM PORT "rstn" ;
            119 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: BLOCK PATH TO PORT "OUT*" ;
            0 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: BLOCK PATH FROM PORT "INP*" ;
            16 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: BLOCK PATH FROM PORT "SRAM_A*" ;
            0 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: BLOCK PATH TO PORT "LED*" ;
            8 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: BLOCK PATH FROM CELL "*ctc_reset_chx*" ;
            14 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*cnt_done_nfts_rx*" 2.000000 X ;
            214 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 10.153ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[6]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               5.779ns  (30.2% logic, 69.8% route), 13 logic levels.

 Constraint Details:

      5.779ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 10.153ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R19C7A.CLK to     R19C7A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 (from clk_125_c)
ROUTE         6     1.403      R19C7A.Q0 to     R15C6D.A1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[6]
CTOF_DEL    ---     0.164      R15C6D.A1 to     R15C6D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8099
ROUTE         1     0.588      R15C6D.F1 to     R15C6D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c6_a0_0
CTOF_DEL    ---     0.164      R15C6D.B0 to     R15C6D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8099
ROUTE         1     1.058      R15C6D.F0 to     R16C5B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c6_i
C1TOFCO_DE  ---     0.310      R16C5B.A1 to    R16C5B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1023
ROUTE         1     0.000     R16C5B.FCO to    R16C5C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
```

```
FCITOFCO_D  ---     0.064     R16C5C.FCI to     R16C5C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024
ROUTE         1     0.000     R16C5C.FCO to     R16C6A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.064     R16C6A.FCI to     R16C6A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000     R16C6A.FCO to     R16C6B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.064     R16C6B.FCI to     R16C6B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000     R16C6B.FCO to     R16C6C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.064     R16C6C.FCI to     R16C6C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000     R16C6C.FCO to     R16C7A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.064     R16C7A.FCI to     R16C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000     R16C7A.FCO to     R16C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.064     R16C7B.FCI to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.064     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.220     R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.985      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.164      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    5.779   (30.2% logic, 69.8% route), 13 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C7A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 10.337ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[7]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               5.595ns  (31.2% logic, 68.8% route), 13 logic levels.

 Constraint Details:

      5.595ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 10.337ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R19C7A.CLK to      R19C7A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 (from clk_125_c)
ROUTE         5     1.219      R19C7A.Q1 to      R15C6D.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[7]
CTOF_DEL    ---     0.164      R15C6D.C1 to      R15C6D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8099
ROUTE         1     0.588      R15C6D.F1 to      R15C6D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c6_a0_0
CTOF_DEL    ---     0.164      R15C6D.B0 to      R15C6D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8099
ROUTE         1     1.058      R15C6D.F0 to      R16C5B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c6_i
C1TOFCO_DE  ---     0.310      R16C5B.A1 to     R16C5B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1023
ROUTE         1     0.000     R16C5B.FCO to     R16C5C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
FCITOFCO_D  ---     0.064     R16C5C.FCI to     R16C5C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024
ROUTE         1     0.000     R16C5C.FCO to     R16C6A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.064     R16C6A.FCI to     R16C6A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000     R16C6A.FCO to     R16C6B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.064     R16C6B.FCI to     R16C6B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000     R16C6B.FCO to     R16C6C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.064     R16C6C.FCI to     R16C6C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000     R16C6C.FCO to     R16C7A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.064     R16C7A.FCI to     R16C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000     R16C7A.FCO to     R16C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.064     R16C7B.FCI to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.064     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.220     R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.985      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.164      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    5.595   (31.2% logic, 68.8% route), 13 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C7A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 10.425ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[4]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               5.507ns  (31.7% logic, 68.3% route), 13 logic levels.

 Constraint Details:

      5.507ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 10.425ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R19C6C.CLK to      R19C6C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 (from clk_125_c)
ROUTE         9     1.131      R19C6C.Q0 to      R15C6D.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[4]
CTOF_DEL    ---     0.164      R15C6D.B1 to      R15C6D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8099
ROUTE         1     0.588      R15C6D.F1 to      R15C6D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c6_a0_0
CTOF_DEL    ---     0.164      R15C6D.B0 to      R15C6D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8099
ROUTE         1     1.058      R15C6D.F0 to      R16C5B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c6_i
C1TOFCO_DE  ---     0.310      R16C5B.A1 to     R16C5B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1023
ROUTE         1     0.000     R16C5B.FCO to     R16C5C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
FCITOFCO_D  ---     0.064     R16C5C.FCI to     R16C5C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024
ROUTE         1     0.000     R16C5C.FCO to     R16C6A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.064     R16C6A.FCI to     R16C6A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000     R16C6A.FCO to     R16C6B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.064     R16C6B.FCI to     R16C6B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000     R16C6B.FCO to     R16C6C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.064     R16C6C.FCI to     R16C6C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000     R16C6C.FCO to     R16C7A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.064     R16C7A.FCI to     R16C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000     R16C7A.FCO to     R16C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.064     R16C7B.FCI to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.064     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.220     R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.985      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.164      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    5.507   (31.7% logic, 68.3% route), 13 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C6C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.
```

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R19C9A.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 10.577ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[4] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx (to clk_125_c +)

Delay: 5.355ns (33.5% logic, 66.5% route), 12 logic levels.

Constraint Details:

5.355ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
16.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 15.932ns) by 10.577ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 R19C6C.CLK to | R19C6C.Q0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 (from clk_125_c) |
| ROUTE | 9 | 1.403 R19C6C.Q0 to | R15C5A.A1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[4] |
| CTOF_DEL | --- | 0.164 R15C5A.A1 to | R15C5A.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8097 |
| ROUTE | 2 | 0.370 R15C5A.F1 to | R15C5B.D0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c7_a0_4 |
| CTOF_DEL | --- | 0.164 R15C5B.D0 to | R15C5B.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_9669 |
| ROUTE | 1 | 0.803 R15C5B.F0 to | R16C5C.B0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c7_i |
| C0TOFCO_DE | --- | 0.423 R16C5C.B0 to | R16C5C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024 |
| ROUTE | 1 | 0.000 R16C5C.FCO to | R16C6A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10] |
| FCITOFCO_D | --- | 0.064 R16C6A.FCI to | R16C6A.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025 |
| ROUTE | 1 | 0.000 R16C6A.FCO to | R16C6B.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12] |
| FCITOFCO_D | --- | 0.064 R16C6B.FCI to | R16C6B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026 |
| ROUTE | 1 | 0.000 R16C6B.FCO to | R16C6C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14] |
| FCITOFCO_D | --- | 0.064 R16C6C.FCI to | R16C6C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027 |
| ROUTE | 1 | 0.000 R16C6C.FCO to | R16C7A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16] |
| FCITOFCO_D | --- | 0.064 R16C7A.FCI to | R16C7A.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028 |
| ROUTE | 1 | 0.000 R16C7A.FCO to | R16C7B.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20] |
| FCITOFCO_D | --- | 0.064 R16C7B.FCI to | R16C7B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029 |
| ROUTE | 1 | 0.000 R16C7B.FCO to | R16C7C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24] |
| FCITOFCO_D | --- | 0.064 R16C7C.FCI to | R16C7C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030 |
| ROUTE | 1 | 0.000 R16C7C.FCO to | R16C8A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28] |
| FCITOF1_DE | --- | 0.220 R16C8A.FCI to | R16C8A.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031 |
| ROUTE | 1 | 0.985 R16C8A.F1 to | R19C9A.C0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30] |
| CTOF_DEL | --- | 0.164 R19C9A.C0 to | R19C9A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 |
| ROUTE | 1 | 0.000 R19C9A.F0 to | R19C9A.DI0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c) |
| | | 5.355 (33.5% logic, 66.5% route), 12 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R19C6C.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R19C9A.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 10.646ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[5] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx (to clk_125_c +)

Delay: 5.286ns (33.0% logic, 67.0% route), 13 logic levels.

Constraint Details:

5.286ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
16.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 15.932ns) by 10.646ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 R19C6C.CLK to | R19C6C.Q1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 (from clk_125_c) |
| ROUTE | 8 | 0.910 R19C6C.Q1 to | R15C6D.D1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[5] |
| CTOF_DEL | --- | 0.164 R15C6D.D1 to | R15C6D.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8099 |
| ROUTE | 1 | 0.588 R15C6D.F1 to | R15C6D.B0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c6_a0_0 |
| CTOF_DEL | --- | 0.164 R15C6D.B0 to | R15C6D.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8099 |
| ROUTE | 1 | 1.058 R15C6D.F0 to | R16C5B.A1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c6_i |
| C1TOFCO_DE | --- | 0.310 R16C5B.A1 to | R16C5B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1023 |
| ROUTE | 1 | 0.000 R16C5B.FCO to | R16C5C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8] |
| FCITOFCO_D | --- | 0.064 R16C5C.FCI to | R16C5C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024 |
| ROUTE | 1 | 0.000 R16C5C.FCO to | R16C6A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10] |
| FCITOFCO_D | --- | 0.064 R16C6A.FCI to | R16C6A.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025 |
| ROUTE | 1 | 0.000 R16C6A.FCO to | R16C6B.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12] |
| FCITOFCO_D | --- | 0.064 R16C6B.FCI to | R16C6B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026 |
| ROUTE | 1 | 0.000 R16C6B.FCO to | R16C6C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14] |
| FCITOFCO_D | --- | 0.064 R16C6C.FCI to | R16C6C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027 |
| ROUTE | 1 | 0.000 R16C6C.FCO to | R16C7A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16] |
| FCITOFCO_D | --- | 0.064 R16C7A.FCI to | R16C7A.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028 |
| ROUTE | 1 | 0.000 R16C7A.FCO to | R16C7B.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20] |
| FCITOFCO_D | --- | 0.064 R16C7B.FCI to | R16C7B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029 |
| ROUTE | 1 | 0.000 R16C7B.FCO to | R16C7C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24] |
| FCITOFCO_D | --- | 0.064 R16C7C.FCI to | R16C7C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030 |
| ROUTE | 1 | 0.000 R16C7C.FCO to | R16C8A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28] |
| FCITOF1_DE | --- | 0.220 R16C8A.FCI to | R16C8A.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031 |
| ROUTE | 1 | 0.985 R16C8A.F1 to | R19C9A.C0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30] |
| CTOF_DEL | --- | 0.164 R19C9A.C0 to | R19C9A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 |
| ROUTE | 1 | 0.000 R19C9A.F0 to | R19C9A.DI0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c) |
| | | 5.286 (33.0% logic, 67.0% route), 13 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R19C6C.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R19C9A.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 10.666ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[6] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx (to clk_125_c +)

Delay: 5.266ns (34.1% logic, 65.9% route), 12 logic levels.

Constraint Details:

5.266ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
16.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 15.932ns) by 10.666ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 R19C7A.CLK to | R19C7A.Q0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 (from clk_125_c) |
| ROUTE | 6 | 1.314 R19C7A.Q0 to | R15C5A.B1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[6] |
| CTOF_DEL | --- | 0.164 R15C5A.B1 to | R15C5A.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8097 |

ROUTE         2     0.370      R15C5A.F1 to      R15C5B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c7_a0_4
CTOF_DEL    ---     0.164      R15C5B.D0 to      R15C5B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_9669
ROUTE         1     0.803      R15C5B.F0 to      R16C5C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c7_i
C0TOFCO_DE  ---     0.423      R16C5C.B0 to     R16C5C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024
ROUTE         1     0.000     R16C5C.FCO to     R16C6A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.064     R16C6A.FCI to     R16C6A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000     R16C6A.FCO to     R16C6B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.064     R16C6B.FCI to     R16C6B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000     R16C6B.FCO to     R16C6C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.064     R16C6C.FCI to     R16C6C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000     R16C6C.FCO to     R16C7A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.064     R16C7A.FCI to     R16C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000     R16C7A.FCO to     R16C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.064     R16C7B.FCI to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.064     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.220     R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.985      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.164      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    5.266   (34.1% logic, 65.9% route), 12 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C7A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 10.690ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[7]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               5.242ns  (28.1% logic, 71.9% route), 7 logic levels.

 Constraint Details:

      5.242ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 10.690ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R19C7C.CLK to      R19C7C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 (from clk_125_c)
ROUTE         2     0.885      R19C7C.Q1 to      R18C7A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[7]
CTOF_DEL    ---     0.164      R18C7A.B1 to      R18C7A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8078
ROUTE        22     1.068      R18C7A.F1 to      R16C8D.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_1_0
CTOF_DEL    ---     0.164      R16C8D.C1 to      R16C8D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8341
ROUTE         1     0.830      R16C8D.F1 to      R16C7B.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_df22
C0TOFCO_DE  ---     0.423      R16C7B.A0 to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.064     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.220     R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.985      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.164      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    5.242   (28.1% logic, 71.9% route), 7 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C7C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 10.694ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[9]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               5.238ns  (28.1% logic, 71.9% route), 7 logic levels.

 Constraint Details:

      5.238ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_976 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 10.694ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_976 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R19C7B.CLK to      R19C7B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_976 (from clk_125_c)
ROUTE         1     0.881      R19C7B.Q1 to      R18C7A.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[9]
CTOF_DEL    ---     0.164      R18C7A.D1 to      R18C7A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8078
ROUTE        22     1.068      R18C7A.F1 to      R16C8D.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_1_0
CTOF_DEL    ---     0.164      R16C8D.C1 to      R16C8D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8341
ROUTE         1     0.830      R16C8D.F1 to      R16C7B.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_df22
C0TOFCO_DE  ---     0.423      R16C7B.A0 to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.064     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.220     R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.985      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.164      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    5.238   (28.1% logic, 71.9% route), 7 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_976:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C7B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 10.709ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[5]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               5.223ns  (34.3% logic, 65.7% route), 12 logic levels.

 Constraint Details:

      5.223ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
     16.000ns delay constraint less

      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 10.709ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R19C6C.CLK to      R19C6C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 (from clk_125_c)
ROUTE         8     1.271      R19C6C.Q1 to      R15C5A.C1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[5]
CTOF_DEL    ---     0.164      R15C5A.C1 to      R15C5A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8097
ROUTE         2     0.370      R15C5A.F1 to      R15C5B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c7_a0_4
CTOF_DEL    ---     0.164      R15C5B.D0 to      R15C5B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_9669
ROUTE         1     0.803      R15C5B.F0 to      R16C5C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c7_i
C0TOFCO_DE  ---     0.423      R16C5C.B0 to     R16C5C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024
ROUTE         1     0.000     R16C5C.FCO to     R16C6A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.064     R16C6A.FCI to     R16C6A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000     R16C6A.FCO to     R16C6B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.064     R16C6B.FCI to     R16C6B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000     R16C6B.FCO to     R16C6C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.064     R16C6C.FCI to     R16C6C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000     R16C6C.FCO to     R16C7A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.064     R16C7A.FCI to     R16C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000     R16C7A.FCO to     R16C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.064     R16C7B.FCI to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.064     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.220      R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.985      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.164      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    5.223   (34.3% logic, 65.7% route), 12 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C6C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 10.717ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[7]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               5.215ns  (28.3% logic, 71.7% route), 7 logic levels.

 Constraint Details:

      5.215ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 10.717ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R19C7C.CLK to      R19C7C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 (from clk_125_c)
ROUTE         2     0.885      R19C7C.Q1 to      R18C7A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[7]
CTOF_DEL    ---     0.164      R18C7A.B1 to      R18C7A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8078
ROUTE        22     1.068      R18C7A.F1 to      R16C8D.C0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_1_0
CTOF_DEL    ---     0.164      R16C8D.C0 to      R16C8D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8341
ROUTE         1     0.803      R16C8D.F0 to      R16C7B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_lt22
C0TOFCO_DE  ---     0.423      R16C7B.B0 to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.064     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.220      R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.985      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.164      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    5.215   (28.3% logic, 71.7% route), 7 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C7C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


================================================================================
Preference: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*ltssm_nfts_rx_skp*" 2.000000 X ;
            244 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 9.572ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[7]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               6.360ns  (23.9% logic, 76.1% route), 9 logic levels.

 Constraint Details:

      6.360ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.572ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R19C7C.CLK to      R19C7C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 (from clk_125_c)
ROUTE         2     0.885      R19C7C.Q1 to      R18C7B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[7]
CTOF_DEL    ---     0.164      R18C7B.B1 to      R18C7B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8096
ROUTE         2     0.670      R18C7B.F1 to      R18C8D.A1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c8_a0_0
CTOF_DEL    ---     0.164      R18C8D.A1 to      R18C8D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8081
ROUTE        16     1.351      R18C8D.F1 to      R16C9C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i
CTOF_DEL    ---     0.164      R16C9C.B0 to      R16C9C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8455
ROUTE         1     0.824      R16C9C.F0 to      R15C9A.A1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_df22
C1TOFCO_DE  ---     0.310      R15C9A.A1 to     R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to     R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.064     R15C9B.FCI to     R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to     R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.064     R15C9C.FCI to     R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.149    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     1.112     R15C10A.F0 to      R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.164      R21C9A.A0 to      R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    6.360   (23.9% logic, 76.1% route), 9 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C7C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R21C9A.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 9.577ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[7] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

Delay: 6.355ns (25.7% logic, 74.3% route), 9 logic levels.

Constraint Details:

6.355ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
16.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 15.932ns) by 9.577ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 R19C7C.CLK to | R19C7C.Q1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 (from clk_125_c) |
| ROUTE | 2 | 0.885 R19C7C.Q1 to | R18C7B.B1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[7] |
| CTOF_DEL | --- | 0.164 R18C7B.B1 to | R18C7B.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8096 |
| ROUTE | 2 | 0.670 R18C7B.F1 to | R18C8D.A1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c8_a0_0 |
| CTOF_DEL | --- | 0.164 R18C8D.A1 to | R18C8D.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8081 |
| ROUTE | 16 | 1.227 R18C8D.F1 to | R16C9A.C0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i |
| CTOF_DEL | --- | 0.164 R16C9A.C0 to | R16C9A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8454 |
| ROUTE | 1 | 0.830 R16C9A.F0 to | R15C9A.A0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_df20 |
| C0TOFCO_DE | --- | 0.423 R15C9A.A0 to | R15C9A.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002 |
| ROUTE | 1 | 0.000 R15C9A.FCO to | R15C9B.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22] |
| FCITOFCO_D | --- | 0.064 R15C9B.FCI to | R15C9B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003 |
| ROUTE | 1 | 0.000 R15C9B.FCO to | R15C9C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26] |
| FCITOFCO_D | --- | 0.064 R15C9C.FCI to | R15C9C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004 |
| ROUTE | 1 | 0.000 R15C9C.FCO to | R15C10A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30] |
| FCITOF0_DE | --- | 0.149 R15C10A.FCI to | R15C10A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005 |
| ROUTE | 1 | 1.112 R15C10A.F0 to | R21C9A.A0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30] |
| CTOF_DEL | --- | 0.164 R21C9A.A0 to | R21C9A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 |
| ROUTE | 1 | 0.000 R21C9A.F0 to | R21C9A.DI0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c) |
| | | 6.355 (25.7% logic, 74.3% route), 9 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R19C7C.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R21C9A.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 9.593ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[7] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

Delay: 6.339ns (23.9% logic, 76.1% route), 9 logic levels.

Constraint Details:

6.339ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
16.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 15.932ns) by 9.593ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 R19C7C.CLK to | R19C7C.Q1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 (from clk_125_c) |
| ROUTE | 2 | 0.885 R19C7C.Q1 to | R18C7B.B1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[7] |
| CTOF_DEL | --- | 0.164 R18C7B.B1 to | R18C7B.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8096 |
| ROUTE | 2 | 0.670 R18C7B.F1 to | R18C8D.A1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c8_a0_0 |
| CTOF_DEL | --- | 0.164 R18C8D.A1 to | R18C8D.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8081 |
| ROUTE | 16 | 1.351 R18C8D.F1 to | R16C9C.B1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i |
| CTOF_DEL | --- | 0.164 R16C9C.B1 to | R16C9C.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8455 |
| ROUTE | 1 | 0.803 R16C9C.F1 to | R15C9A.B1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_lt22 |
| C1TOFCO_DE | --- | 0.310 R15C9A.B1 to | R15C9A.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002 |
| ROUTE | 1 | 0.000 R15C9A.FCO to | R15C9B.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22] |
| FCITOFCO_D | --- | 0.064 R15C9B.FCI to | R15C9B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003 |
| ROUTE | 1 | 0.000 R15C9B.FCO to | R15C9C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26] |
| FCITOFCO_D | --- | 0.064 R15C9C.FCI to | R15C9C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004 |
| ROUTE | 1 | 0.000 R15C9C.FCO to | R15C10A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30] |
| FCITOF0_DE | --- | 0.149 R15C10A.FCI to | R15C10A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005 |
| ROUTE | 1 | 1.112 R15C10A.F0 to | R21C9A.A0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30] |
| CTOF_DEL | --- | 0.164 R21C9A.A0 to | R21C9A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 |
| ROUTE | 1 | 0.000 R21C9A.F0 to | R21C9A.DI0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c) |
| | | 6.339 (23.9% logic, 76.1% route), 9 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R19C7C.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R21C9A.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 9.612ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[6] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

Delay: 6.320ns (24.0% logic, 76.0% route), 9 logic levels.

Constraint Details:

6.320ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
16.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 15.932ns) by 9.612ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 R19C7C.CLK to | R19C7C.Q0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 (from clk_125_c) |
| ROUTE | 2 | 0.845 R19C7C.Q0 to | R18C7B.D1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[6] |
| CTOF_DEL | --- | 0.164 R18C7B.D1 to | R18C7B.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8096 |
| ROUTE | 2 | 0.670 R18C7B.F1 to | R18C8D.A1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c8_a0_0 |
| CTOF_DEL | --- | 0.164 R18C8D.A1 to | R18C8D.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8081 |
| ROUTE | 16 | 1.351 R18C8D.F1 to | R16C9C.B0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i |
| CTOF_DEL | --- | 0.164 R16C9C.B0 to | R16C9C.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8455 |
| ROUTE | 1 | 0.824 R16C9C.F0 to | R15C9A.A1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_df22 |
| C1TOFCO_DE | --- | 0.310 R15C9A.A1 to | R15C9A.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002 |
| ROUTE | 1 | 0.000 R15C9A.FCO to | R15C9B.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22] |
| FCITOFCO_D | --- | 0.064 R15C9B.FCI to | R15C9B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003 |
| ROUTE | 1 | 0.000 R15C9B.FCO to | R15C9C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26] |
| FCITOFCO_D | --- | 0.064 R15C9C.FCI to | R15C9C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004 |
| ROUTE | 1 | 0.000 R15C9C.FCO to | R15C10A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30] |
| FCITOF0_DE | --- | 0.149 R15C10A.FCI to | R15C10A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005 |
| ROUTE | 1 | 1.112 R15C10A.F0 to | R21C9A.A0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30] |
| CTOF_DEL | --- | 0.164 R21C9A.A0 to | R21C9A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 |

ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    6.320   (24.0% logic, 76.0% route), 9 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C7C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R21C9A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 9.616ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               6.316ns  (24.0% logic, 76.0% route), 9 logic levels.

 Constraint Details:

      6.316ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.616ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R20C6C.CLK to      R20C6C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983 (from clk_125_c)
ROUTE        11     0.841      R20C6C.Q0 to      R18C7B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[1]
CTOF_DEL    ---     0.164      R18C7B.A1 to      R18C7B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8096
ROUTE         2     0.670      R18C7B.F1 to      R18C8D.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c8_a0_0
CTOF_DEL    ---     0.164      R18C8D.A1 to      R18C8D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8081
ROUTE        16     1.351      R18C8D.F1 to      R16C9C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i
CTOF_DEL    ---     0.164      R16C9C.B0 to      R16C9C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8455
ROUTE         1     0.824      R16C9C.F0 to      R15C9A.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_df22
C1TOFCO_DE  ---     0.310      R15C9A.A1 to     R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to     R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.064     R15C9B.FCI to     R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to     R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.064     R15C9C.FCI to     R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.149    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     1.112     R15C10A.F0 to      R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.164      R21C9A.A0 to      R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    6.316   (24.0% logic, 76.0% route), 9 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R20C6C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R21C9A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 9.617ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[6]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               6.315ns  (25.8% logic, 74.2% route), 9 logic levels.

 Constraint Details:

      6.315ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.617ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275      R19C7C.CLK to      R19C7C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 (from clk_125_c)
ROUTE         2     0.845      R19C7C.Q0 to      R18C7B.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[6]
CTOF_DEL    ---     0.164      R18C7B.D1 to      R18C7B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8096
ROUTE         2     0.670      R18C7B.F1 to      R18C8D.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c8_a0_0
CTOF_DEL    ---     0.164      R18C8D.A1 to      R18C8D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8081
ROUTE        16     1.227      R18C8D.F1 to      R16C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i
CTOF_DEL    ---     0.164      R16C9A.C0 to      R16C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8454
ROUTE         1     0.830      R16C9A.F0 to      R15C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_df20
C0TOFCO_DE  ---     0.423      R15C9A.A0 to     R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to     R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.064     R15C9B.FCI to     R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to     R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.064     R15C9C.FCI to     R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.149    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     1.112     R15C10A.F0 to      R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.164      R21C9A.A0 to      R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    6.315   (25.8% logic, 74.2% route), 9 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C7C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R21C9A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 9.621ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               6.311ns  (25.8% logic, 74.2% route), 9 logic levels.

 Constraint Details:

      6.311ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.621ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R20C6C.CLK to      R20C6C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983 (from clk_125_c)
ROUTE        11     0.841      R20C6C.Q0 to      R18C7B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[1]
CTOF_DEL    ---     0.164      R18C7B.A1 to      R18C7B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8096
ROUTE         2     0.670      R18C7B.F1 to      R18C8D.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c8_a0_0

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CTOF_DEL    ---     0.164      R18C8D.A1 to      R18C8D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8081
ROUTE        16     1.227      R18C8D.F1 to      R16C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i
CTOF_DEL    ---     0.164      R16C9A.C0 to      R16C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8454
ROUTE         1     0.830      R16C9A.F0 to      R15C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_df20
C0TOFCO_DE  ---     0.423      R15C9A.A0 to     R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to     R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.064     R15C9B.FCI to     R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to     R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.064     R15C9C.FCI to     R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.149    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     1.112     R15C10A.F0 to      R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.164      R21C9A.A0 to      R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    6.311   (25.8% logic, 74.2% route), 9 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R20C6C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R21C9A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 9.633ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[6]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               6.299ns  (24.1% logic, 75.9% route), 9 logic levels.

 Constraint Details:

      6.299ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.633ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R19C7C.CLK to      R19C7C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986 (from clk_125_c)
ROUTE         2     0.845      R19C7C.Q0 to      R18C7B.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[6]
CTOF_DEL    ---     0.164      R18C7B.D1 to      R18C7B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8096
ROUTE         2     0.670      R18C7B.F1 to      R18C8D.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c8_a0_0
CTOF_DEL    ---     0.164      R18C8D.A1 to      R18C8D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8081
ROUTE        16     1.351      R18C8D.F1 to      R16C9C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i
CTOF_DEL    ---     0.164      R16C9C.B1 to      R16C9C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8455
ROUTE         1     0.803      R16C9C.F1 to      R15C9A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_lt22
C1TOFCO_DE  ---     0.310      R15C9A.B1 to     R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to     R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.064     R15C9B.FCI to     R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to     R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.064     R15C9C.FCI to     R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.149    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     1.112     R15C10A.F0 to      R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.164      R21C9A.A0 to      R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    6.299   (24.1% logic, 75.9% route), 9 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2986:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C7C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R21C9A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 9.637ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               6.295ns  (24.1% logic, 75.9% route), 9 logic levels.

 Constraint Details:

      6.295ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
     16.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 15.932ns) by 9.637ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R20C6C.CLK to      R20C6C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983 (from clk_125_c)
ROUTE        11     0.841      R20C6C.Q0 to      R18C7B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[1]
CTOF_DEL    ---     0.164      R18C7B.A1 to      R18C7B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8096
ROUTE         2     0.670      R18C7B.F1 to      R18C8D.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c8_a0_0
CTOF_DEL    ---     0.164      R18C8D.A1 to      R18C8D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8081
ROUTE        16     1.351      R18C8D.F1 to      R16C9C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c9_i
CTOF_DEL    ---     0.164      R16C9C.B1 to      R16C9C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8455
ROUTE         1     0.803      R16C9C.F1 to      R15C9A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_lt22
C1TOFCO_DE  ---     0.310      R15C9A.B1 to     R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to     R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.064     R15C9B.FCI to     R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to     R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.064     R15C9C.FCI to     R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.149    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     1.112     R15C10A.F0 to      R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.164      R21C9A.A0 to      R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    6.295   (24.1% logic, 75.9% route), 9 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R20C6C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R21C9A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 9.642ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[6]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               6.290ns  (27.6% logic, 72.4% route), 14 logic levels.

 Constraint Details:

      6.290ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
```

```
    16.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 15.932ns) by 9.642ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R19C7A.CLK to      R19C7A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 (from clk_125_c)
ROUTE         6     1.378      R19C7A.Q0 to      R15C5D.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[6]
CTOF_DEL    ---     0.164      R15C5D.D1 to      R15C5D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8098
ROUTE         1     1.259      R15C5D.F1 to      R15C5D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c6_a0_0
CTOF_DEL    ---     0.164      R15C5D.B0 to      R15C5D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8098
ROUTE         1     0.803      R15C5D.F0 to      R15C7A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un20_ltssm_nfts_rx_skp_c6_i
C1TOFCO_DE  ---     0.310      R15C7A.B1 to     R15C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_996
ROUTE         1     0.000     R15C7A.FCO to     R15C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[7]
FCITOFCO_D  ---     0.064     R15C7B.FCI to     R15C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_997
ROUTE         1     0.000     R15C7B.FCO to     R15C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[9]
FCITOFCO_D  ---     0.064     R15C7C.FCI to     R15C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_998
ROUTE         1     0.000     R15C7C.FCO to     R15C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11]
FCITOFCO_D  ---     0.064     R15C8A.FCI to     R15C8A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_999
ROUTE         1     0.000     R15C8A.FCO to     R15C8B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D  ---     0.064     R15C8B.FCI to     R15C8B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1000
ROUTE         1     0.000     R15C8B.FCO to     R15C8C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D  ---     0.064     R15C8C.FCI to     R15C8C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001
ROUTE         1     0.000     R15C8C.FCO to     R15C9A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D  ---     0.064     R15C9A.FCI to     R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to     R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.064     R15C9B.FCI to     R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to     R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.064     R15C9C.FCI to     R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.149    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     1.112     R15C10A.F0 to      R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.164      R21C9A.A0 to      R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    6.290   (27.6% logic, 72.4% route), 14 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R19C7A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R21C9A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr*" 6.000000 ns ;
            33 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 4.427ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0rff_3  (to clk_125_c +)

   Delay:               1.505ns  (29.2% logic, 70.8% route), 2 logic levels.

 Constraint Details:

      1.505ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.427ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R42C4A.CLK to      R42C4A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        11     1.066      R42C4A.Q1 to      R45C5A.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
CTOF_DEL    ---     0.164      R45C5A.C1 to      R45C5A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363
ROUTE         1     0.000      R45C5A.F1 to     R45C5A.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_32952_0 (to clk_125_c)
                  --------
                    1.505   (29.2% logic, 70.8% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R45C5A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.427ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0rff_2  (to clk_125_c +)

   Delay:               1.505ns  (29.2% logic, 70.8% route), 2 logic levels.

 Constraint Details:

      1.505ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.427ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R42C4A.CLK to      R42C4A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        11     1.066      R42C4A.Q1 to      R45C5A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
CTOF_DEL    ---     0.164      R45C5A.C0 to      R45C5A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363
ROUTE         1     0.000      R45C5A.F0 to     R45C5A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_32955_0 (to clk_125_c)
                  --------
                    1.505   (29.2% logic, 70.8% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R45C5A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.548ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0rff_2  (to clk_125_c +)

   Delay:               1.384ns  (31.7% logic, 68.3% route), 2 logic levels.

 Constraint Details:
```

1.384ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 4.548ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 | R42C4A.CLK to | R42C4A.Q0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c) |
| ROUTE | 12 | 0.945 | R42C4A.Q0 to | R45C5A.B0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0] |
| CTOF_DEL | --- | 0.164 | R45C5A.B0 to | R45C5A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363 |
| ROUTE | 1 | 0.000 | R45C5A.F0 to | R45C5A.DI0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_32955_0 (to clk_125_c) |
| | | 1.384 | (31.7% logic, 68.3% route), 2 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R42C4A.CLK | clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R45C5A.CLK | clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 4.648ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0rff_1 (to clk_125_c +)

Delay: 1.284ns (34.2% logic, 65.8% route), 2 logic levels.

Constraint Details:

1.284ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 4.648ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 | R42C4A.CLK to | R42C4A.Q0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c) |
| ROUTE | 12 | 0.845 | R42C4A.Q0 to | R45C4C.C1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0] |
| CTOF_DEL | --- | 0.164 | R45C4C.C1 to | R45C4C.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362 |
| ROUTE | 1 | 0.000 | R45C4C.F1 to | R45C4C.DI1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_32954_0 (to clk_125_c) |
| | | 1.284 | (34.2% logic, 65.8% route), 2 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R42C4A.CLK | clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R45C4C.CLK | clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 4.648ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0rff_0 (to clk_125_c +)

Delay: 1.284ns (34.2% logic, 65.8% route), 2 logic levels.

Constraint Details:

1.284ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 4.648ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 | R42C4A.CLK to | R42C4A.Q0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c) |
| ROUTE | 12 | 0.845 | R42C4A.Q0 to | R45C4C.C0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0] |
| CTOF_DEL | --- | 0.164 | R45C4C.C0 to | R45C4C.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362 |
| ROUTE | 1 | 0.000 | R45C4C.F0 to | R45C4C.DI0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_32953_0 (to clk_125_c) |
| | | 1.284 | (34.2% logic, 65.8% route), 2 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R42C4A.CLK | clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R45C4C.CLK | clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 4.785ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0rff_3 (to clk_125_c +)

Delay: 1.147ns (38.3% logic, 61.7% route), 2 logic levels.

Constraint Details:

1.147ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 4.785ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 | R42C4A.CLK to | R42C4A.Q0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c) |
| ROUTE | 12 | 0.708 | R42C4A.Q0 to | R45C5A.D1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0] |
| CTOF_DEL | --- | 0.164 | R45C5A.D1 to | R45C5A.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363 |
| ROUTE | 1 | 0.000 | R45C5A.F1 to | R45C5A.DI1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_32952_0 (to clk_125_c) |
| | | 1.147 | (38.3% logic, 61.7% route), 2 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R42C4A.CLK | clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3363:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|

ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R45C5A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.788ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0rff_0  (to clk_125_c +)

   Delay:               1.144ns  (38.4% logic, 61.6% route), 2 logic levels.

 Constraint Details:

     1.144ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.788ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275      R42C4A.CLK to      R42C4A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        11     0.705       R42C4A.Q1 to      R45C4C.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
CTOF_DEL    ---     0.164       R45C4C.D0 to      R45C4C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362
ROUTE         1     0.000       R45C4C.F0 to     R45C4C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_32953_0 (to clk_125_c)
                  --------
                    1.144   (38.4% logic, 61.6% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R45C4C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.788ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0rff_1  (to clk_125_c +)

   Delay:               1.144ns  (38.4% logic, 61.6% route), 2 logic levels.

 Constraint Details:

     1.144ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.788ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275      R42C4A.CLK to      R42C4A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        11     0.705       R42C4A.Q1 to      R45C4C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
CTOF_DEL    ---     0.164       R45C4C.D1 to      R45C4C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362
ROUTE         1     0.000       R45C4C.F1 to     R45C4C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/N_32954_0 (to clk_125_c)
                  --------
                    1.144   (38.4% logic, 61.6% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3362:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R45C4C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.830ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1

   Delay:               1.429ns  (19.2% logic, 80.8% route), 2 logic levels.

 Constraint Details:

     1.429ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1397 meets
     6.000ns delay constraint less
     0.000ns skew and
    -0.259ns WAD_SET requirement (totaling 6.259ns) by 4.830ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1397:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275      R42C4A.CLK to      R42C4A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        12     1.154       R42C4A.Q0 to      R48C5C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL    ---     0.000      R48C5C.A0 to   R48C5C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1395
ROUTE         2     0.000   R48C5C.WADO0 to    R48C5B.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
                  --------
                    1.429   (19.2% logic, 80.8% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1397:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R48C5C.CLK clk_125_c
ZERO_DEL    ---     0.000     R48C5C.CLK to    R48C5C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1395
ROUTE         2     0.000    R48C5C.WCKO to     R48C5B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
                  --------
                    1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 4.830ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0

   Delay:               1.429ns  (19.2% logic, 80.8% route), 2 logic levels.

 Constraint Details:

     1.429ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1396 meets
     6.000ns delay constraint less
     0.000ns skew and
    -0.259ns WAD_SET requirement (totaling 6.259ns) by 4.830ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1396:

```
   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R42C4A.CLK to      R42C4A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        12     1.154      R42C4A.Q0 to      R48C5C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL    ---     0.000      R48C5C.A0 to   R48C5C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1395
ROUTE         2     0.000   R48C5C.WADO0 to    R48C5A.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
                  --------
                    1.429   (19.2% logic, 80.8% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1396:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R48C5C.CLK clk_125_c
ZERO_DEL    ---     0.000     R48C5C.CLK to    R48C5C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1395
ROUTE         2     0.000    R48C5C.WCKO to     R48C5A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
                  --------
                    1.415   (0.0% logic, 100.0% route), 1 logic levels.

Report:  635.728MHz is the maximum frequency for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr*" 6.000000 ns ;
            147 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 2.256ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[0]  (to clk_125_c +)

   Delay:               3.676ns  (16.4% logic, 83.6% route), 3 logic levels.

 Constraint Details:

      3.676ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2775 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 2.256ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2775:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R36C8C.CLK to      R36C8C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c)
ROUTE        29     1.923      R36C8C.Q1 to     R39C18A.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL    ---     0.164     R39C18A.B0 to     R39C18A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1379
ROUTE         1     1.150     R39C18A.F0 to     R39C13C.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1rx[0]
CTOF_DEL    ---     0.164     R39C13C.C0 to     R39C13C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2775
ROUTE         1     0.000     R39C13C.F0 to    R39C13C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[0] (to clk_125_c)
                  --------
                    3.676   (16.4% logic, 83.6% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2775:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R39C13C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 2.387ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[9]  (to clk_125_c +)

   Delay:               3.545ns  (17.0% logic, 83.0% route), 3 logic levels.

 Constraint Details:

      3.545ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2784 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 2.387ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2784:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275      R36C8C.CLK to      R36C8C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c)
ROUTE        29     1.669      R36C8C.Q1 to     R39C11A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL    ---     0.164     R39C11A.B1 to     R39C11A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_1/SLICE_1373
ROUTE         1     1.273     R39C11A.F1 to     R36C12C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1rx[9]
CTOF_DEL    ---     0.164     R36C12C.B0 to     R36C12C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2784
ROUTE         1     0.000     R36C12C.F0 to    R36C12C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[9] (to clk_125_c)
                  --------
                    3.545   (17.0% logic, 83.0% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2784:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R36C12C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 2.483ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[5]  (to clk_125_c +)

   Delay:               3.449ns  (17.5% logic, 82.5% route), 3 logic levels.

 Constraint Details:

      3.449ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2777 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 2.483ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2777:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275      R36C8C.CLK to      R36C8C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c)
ROUTE        29     1.829      R36C8C.Q1 to     R39C14A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL    ---     0.164     R39C14A.B1 to     R39C14A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/SLICE_1376
ROUTE         1     1.017     R39C14A.F1 to     R38C13B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1rx[5]
CTOF_DEL    ---     0.164     R38C13B.A1 to     R38C13B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2777
ROUTE         1     0.000     R38C13B.F1 to    R38C13B.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[5] (to clk_125_c)
                  --------
                    3.449   (17.5% logic, 82.5% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
```

```
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2777:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R38C13B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 2.535ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[2]  (to clk_125_c +)

   Delay:               3.397ns  (17.8% logic, 82.2% route), 3 logic levels.

 Constraint Details:

      3.397ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2776 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 2.535ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2776:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R36C8C.CLK to      R36C8C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c)
ROUTE        29     1.923      R36C8C.Q1 to     R39C18B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL    ---     0.164     R39C18B.B0 to     R39C18B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1380
ROUTE         1     0.871     R39C18B.F0 to     R39C13A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1rx[2]
CTOF_DEL    ---     0.164     R39C13A.A0 to     R39C13A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2776
ROUTE         1     0.000     R39C13A.F0 to    R39C13A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[2] (to clk_125_c)
                  --------
                    3.397   (17.8% logic, 82.2% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2776:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R39C13A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 2.544ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[0]  (to clk_125_c +)

   Delay:               3.388ns  (17.8% logic, 82.2% route), 3 logic levels.

 Constraint Details:

      3.388ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2775 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 2.544ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2775:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R36C8C.CLK to      R36C8C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c)
ROUTE        30     1.635      R36C8C.Q0 to     R39C18A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL    ---     0.164     R39C18A.A0 to     R39C18A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1379
ROUTE         1     1.150     R39C18A.F0 to     R39C13C.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1rx[0]
CTOF_DEL    ---     0.164     R39C13C.C0 to     R39C13C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2775
ROUTE         1     0.000     R39C13C.F0 to    R39C13C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[0] (to clk_125_c)
                  --------
                    3.388   (17.8% logic, 82.2% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2775:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R39C13C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 2.575ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[10]  (to clk_125_c +)

   Delay:               3.357ns  (18.0% logic, 82.0% route), 3 logic levels.

 Constraint Details:

      3.357ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 2.575ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R36C8C.CLK to      R36C8C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c)
ROUTE        29     1.669      R36C8C.Q1 to     R39C11B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL    ---     0.164     R39C11B.B0 to     R39C11B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_1/SLICE_1374
ROUTE         1     1.085     R39C11B.F0 to     R34C11C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1rx[10]
CTOF_DEL    ---     0.164     R34C11C.B0 to     R34C11C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817
ROUTE         1     0.000     R34C11C.F0 to    R34C11C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[10] (to clk_125_c)
                  --------
                    3.357   (18.0% logic, 82.0% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R34C11C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 2.592ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[6]  (to clk_125_c +)

   Delay:               3.340ns  (18.1% logic, 81.9% route), 3 logic levels.

 Constraint Details:
```

3.340ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2782 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 2.592ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2782:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 | R36C8C.CLK to | R36C8C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c) |
| ROUTE | 29 | 1.679 | R36C8C.Q1 to | R39C17B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1] |
| CTOF_DEL | --- | 0.164 | R39C17B.B0 to | R39C17B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1366 |
| ROUTE | 1 | 1.058 | R39C17B.F0 to | R37C16A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0rx[6] |
| CTOF_DEL | --- | 0.164 | R37C16A.A0 to | R37C16A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2782 |
| ROUTE | 1 | 0.000 | R37C16A.F0 to | R37C16A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[6] (to clk_125_c) |
| | | 3.340 | (18.1% logic, 81.9% route), 3 logic levels. | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R36C8C.CLK clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2782:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R37C16A.CLK clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | |

Passed: The following path meets requirements by 2.605ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

| | | | |
|---|---|---|---|
| Source: | FF | Q | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0] (from clk_125_c +) |
| Destination: | FF | Data in | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[2] (to clk_125_c +) |

Delay: 3.327ns (18.1% logic, 81.9% route), 3 logic levels.

Constraint Details:

3.327ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2780 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 2.605ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2780:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 | R36C8C.CLK to | R36C8C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c) |
| ROUTE | 30 | 1.894 | R36C8C.Q0 to | R34C18B.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0] |
| CTOF_DEL | --- | 0.164 | R34C18B.A0 to | R34C18B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram/SLICE_1369 |
| ROUTE | 1 | 0.830 | R34C18B.F0 to | R34C16C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0rx[2] |
| CTOF_DEL | --- | 0.164 | R34C16C.A0 to | R34C16C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2780 |
| ROUTE | 1 | 0.000 | R34C16C.F0 to | R34C16C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[2] (to clk_125_c) |
| | | 3.327 | (18.1% logic, 81.9% route), 3 logic levels. | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R36C8C.CLK clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2780:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R34C16C.CLK clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | |

Passed: The following path meets requirements by 2.680ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

| | | | |
|---|---|---|---|
| Source: | FF | Q | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1] (from clk_125_c +) |
| Destination: | FF | Data in | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[8] (to clk_125_c +) |

Delay: 3.252ns (18.5% logic, 81.5% route), 3 logic levels.

Constraint Details:

3.252ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2785 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 2.680ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2785:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 | R36C8C.CLK to | R36C8C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c) |
| ROUTE | 29 | 1.669 | R36C8C.Q1 to | R39C11A.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1] |
| CTOF_DEL | --- | 0.164 | R39C11A.B0 to | R39C11A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_1/SLICE_1373 |
| ROUTE | 1 | 0.980 | R39C11A.F0 to | R36C11A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1rx[8] |
| CTOF_DEL | --- | 0.164 | R36C11A.C0 to | R36C11A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2785 |
| ROUTE | 1 | 0.000 | R36C11A.F0 to | R36C11A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[8] (to clk_125_c) |
| | | 3.252 | (18.5% logic, 81.5% route), 3 logic levels. | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R36C8C.CLK clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2785:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R36C11A.CLK clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | |

Passed: The following path meets requirements by 2.686ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

| | | | |
|---|---|---|---|
| Source: | FF | Q | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0] (from clk_125_c +) |
| Destination: | FF | Data in | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[3] (to clk_125_c +) |

Delay: 3.246ns (18.6% logic, 81.4% route), 3 logic levels.

Constraint Details:

3.246ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2780 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 2.686ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2780:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 | R36C8C.CLK to | R36C8C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c) |
| ROUTE | 30 | 1.894 | R36C8C.Q0 to | R34C18B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0] |
| CTOF_DEL | --- | 0.164 | R34C18B.A1 to | R34C18B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram/SLICE_1369 |
| ROUTE | 1 | 0.749 | R34C18B.F1 to | R34C16C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0rx[3] |
| CTOF_DEL | --- | 0.164 | R34C16C.C1 to | R34C16C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2780 |
| ROUTE | 1 | 0.000 | R34C16C.F1 to | R34C16C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[3] (to clk_125_c) |
| | | 3.246 | (18.6% logic, 81.4% route), 3 logic levels. | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2780:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R34C16C.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

Report:  267.094MHz is the maximum frequency for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr*" 6.000000 ns ;
            14 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 4.647ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_eidle_tx  (to clk_125_c +)

   Delay:               1.285ns  (34.2% logic, 65.8% route), 2 logic levels.

 Constraint Details:

      1.285ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.647ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R31C21A.CLK to     R31C21A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 (from clk_125_c)
ROUTE         5     0.846     R31C21A.Q0 to     R30C21A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]
CTOF_DEL    ---     0.164     R30C21A.A0 to     R30C21A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0
ROUTE         1     0.000     R30C21A.F0 to    R30C21A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/ltssm_eidle_tx (to clk_125_c)
                    --------
                      1.285   (34.2% logic, 65.8% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R31C21A.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C21A.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.785ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_eidle_tx  (to clk_125_c +)

   Delay:               1.147ns  (38.3% logic, 61.7% route), 2 logic levels.

 Constraint Details:

      1.147ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.785ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R31C21B.CLK to     R31C21B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 (from clk_125_c)
ROUTE         3     0.708     R31C21B.Q1 to     R30C21A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]
CTOF_DEL    ---     0.164     R30C21A.C0 to     R30C21A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0
ROUTE         1     0.000     R30C21A.F0 to    R30C21A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/ltssm_eidle_tx (to clk_125_c)
                    --------
                      1.147   (38.3% logic, 61.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R31C21B.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C21A.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.862ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]  (to clk_125_c +)

   Delay:               1.070ns  (41.0% logic, 59.0% route), 2 logic levels.

 Constraint Details:

      1.070ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.862ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R31C21A.CLK to     R31C21A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 (from clk_125_c)
ROUTE         5     0.631     R31C21A.Q0 to     R31C21C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]
CTOF_DEL    ---     0.164     R31C21C.A0 to     R31C21C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233
ROUTE         1     0.000     R31C21C.F0 to    R31C21C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n3 (to clk_125_c)
                    --------
                      1.070   (41.0% logic, 59.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R31C21A.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R31C21C.CLK clk_125_c
                    --------
                      1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.881ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]  (to clk_125_c +)

   Delay:               1.051ns  (41.8% logic, 58.2% route), 2 logic levels.
```

Constraint Details:

     1.051ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.881ns

Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R31C21B.CLK to     R31C21B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 (from clk_125_c)
ROUTE         4     0.612     R31C21B.Q0 to     R31C21B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]
CTOF_DEL    ---     0.164     R31C21B.A1 to     R31C21B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232
ROUTE         1     0.000     R31C21B.F1 to    R31C21B.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n2 (to clk_125_c)
                  --------
                    1.051   (41.8% logic, 58.2% route), 2 logic levels.

Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R31C21B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R31C21B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.889ns

Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_eidle_tx  (to clk_125_c +)

   Delay:               1.043ns  (42.1% logic, 57.9% route), 2 logic levels.

Constraint Details:

     1.043ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.889ns

Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R31C21B.CLK to     R31C21B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 (from clk_125_c)
ROUTE         4     0.604     R31C21B.Q0 to     R30C21A.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]
CTOF_DEL    ---     0.164     R30C21A.B0 to     R30C21A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0
ROUTE         1     0.000     R30C21A.F0 to    R30C21A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/ltssm_eidle_tx (to clk_125_c)
                  --------
                    1.043   (42.1% logic, 57.9% route), 2 logic levels.

Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R31C21B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C21A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.889ns

Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]  (to clk_125_c +)

   Delay:               1.043ns  (42.1% logic, 57.9% route), 2 logic levels.

Constraint Details:

     1.043ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.889ns

Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R31C21B.CLK to     R31C21B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 (from clk_125_c)
ROUTE         4     0.604     R31C21B.Q0 to     R31C21C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]
CTOF_DEL    ---     0.164     R31C21C.B0 to     R31C21C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233
ROUTE         1     0.000     R31C21C.F0 to    R31C21C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n3 (to clk_125_c)
                  --------
                    1.043   (42.1% logic, 57.9% route), 2 logic levels.

Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R31C21B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R31C21C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.989ns

Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]  (to clk_125_c +)

   Delay:               0.943ns  (46.6% logic, 53.4% route), 2 logic levels.

Constraint Details:

     0.943ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.989ns

Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R31C21B.CLK to     R31C21B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 (from clk_125_c)
ROUTE         4     0.504     R31C21B.Q0 to     R31C21B.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]
CTOF_DEL    ---     0.164     R31C21B.C0 to     R31C21B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232
ROUTE         1     0.000     R31C21B.F0 to    R31C21B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n1 (to clk_125_c)
                  --------
                    0.943   (46.6% logic, 53.4% route), 2 logic levels.

Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R31C21B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R31C21B.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 5.103ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2] (to clk_125_c +)

Delay: 0.829ns (53.0% logic, 47.0% route), 2 logic levels.

Constraint Details:

0.829ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 5.103ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 R31C21A.CLK to | R31C21A.Q0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 (from clk_125_c) |
| ROUTE | 5 | 0.390 R31C21A.Q0 to | R31C21B.D1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0] |
| CTOF_DEL | --- | 0.164 R31C21B.D1 to | R31C21B.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 |
| ROUTE | 1 | 0.000 R31C21B.F1 to | R31C21B.DI1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n2 (to clk_125_c) |
| | | 0.829 (53.0% logic, 47.0% route), 2 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R31C21A.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R31C21B.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 5.103ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2] (to clk_125_c +)

Delay: 0.829ns (53.0% logic, 47.0% route), 2 logic levels.

Constraint Details:

0.829ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 5.103ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 R31C21B.CLK to | R31C21B.Q1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 (from clk_125_c) |
| ROUTE | 3 | 0.390 R31C21B.Q1 to | R31C21B.B1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2] |
| CTOF_DEL | --- | 0.164 R31C21B.B1 to | R31C21B.F1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 |
| ROUTE | 1 | 0.000 R31C21B.F1 to | R31C21B.DI1 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n2 (to clk_125_c) |
| | | 0.829 (53.0% logic, 47.0% route), 2 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R31C21B.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R31C21B.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 5.103ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1] (to clk_125_c +)

Delay: 0.829ns (53.0% logic, 47.0% route), 2 logic levels.

Constraint Details:

0.829ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 meets
6.000ns delay constraint less
0.000ns skew and
0.068ns DIN_SET requirement (totaling 5.932ns) by 5.103ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 R31C21A.CLK to | R31C21A.Q0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 (from clk_125_c) |
| ROUTE | 5 | 0.390 R31C21A.Q0 to | R31C21B.D0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0] |
| CTOF_DEL | --- | 0.164 R31C21B.D0 to | R31C21B.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 |
| ROUTE | 1 | 0.000 R31C21B.F0 to | R31C21B.DI0 | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n1 (to clk_125_c) |
| | | 0.829 (53.0% logic, 47.0% route), 2 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R31C21A.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 *FF_TX_H_CLK_0 to | R31C21B.CLK | clk_125_c |
| | | 1.415 (0.0% logic, 100.0% route), 0 logic levels. | | |

Report: 739.098MHz is the maximum frequency for this preference.

================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr*" 6.000000 ns ;
18 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------

Passed: The following path meets requirements by 4.343ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en (to clk_125_c +)

Delay: 1.589ns (37.9% logic, 62.1% route), 3 logic levels.

Constraint Details:

1.589ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230 meets
6.000ns delay constraint less

      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.343ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R30C22A.CLK to     R30C22A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 (from clk_125_c)
ROUTE         3     0.607     R30C22A.Q1 to     R30C22B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]
CTOF_DEL    ---     0.164     R30C22B.A1 to     R30C22B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230
ROUTE         1     0.379     R30C22B.F1 to     R30C22B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en4_NE_i
CTOF_DEL    ---     0.164     R30C22B.B0 to     R30C22B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230
ROUTE         1     0.000     R30C22B.F0 to    R30C22B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/N_33094_0 (to clk_125_c)
                  --------
                    1.589   (37.9% logic, 62.1% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.350ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en  (to clk_125_c +)

   Delay:               1.582ns  (38.1% logic, 61.9% route), 3 logic levels.

 Constraint Details:

      1.582ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.350ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R30C22A.CLK to     R30C22A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 (from clk_125_c)
ROUTE         4     0.600     R30C22A.Q0 to     R30C22B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]
CTOF_DEL    ---     0.164     R30C22B.B1 to     R30C22B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230
ROUTE         1     0.379     R30C22B.F1 to     R30C22B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en4_NE_i
CTOF_DEL    ---     0.164     R30C22B.B0 to     R30C22B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230
ROUTE         1     0.000     R30C22B.F0 to    R30C22B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/N_33094_0 (to clk_125_c)
                  --------
                    1.582   (38.1% logic, 61.9% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.451ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en  (to clk_125_c +)

   Delay:               1.481ns  (40.7% logic, 59.3% route), 3 logic levels.

 Constraint Details:

      1.481ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.451ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R30C22C.CLK to     R30C22C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 (from clk_125_c)
ROUTE         5     0.499     R30C22C.Q1 to     R30C22B.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]
CTOF_DEL    ---     0.164     R30C22B.C1 to     R30C22B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230
ROUTE         1     0.379     R30C22B.F1 to     R30C22B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en4_NE_i
CTOF_DEL    ---     0.164     R30C22B.B0 to     R30C22B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230
ROUTE         1     0.000     R30C22B.F0 to    R30C22B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/N_33094_0 (to clk_125_c)
                  --------
                    1.481   (40.7% logic, 59.3% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.565ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en  (to clk_125_c +)

   Delay:               1.367ns  (44.1% logic, 55.9% route), 3 logic levels.

 Constraint Details:

      1.367ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230 meets
      6.000ns delay constraint less
      0.000ns skew and
      0.068ns DIN_SET requirement (totaling 5.932ns) by 4.565ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R30C22C.CLK to     R30C22C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 (from clk_125_c)
ROUTE         6     0.385     R30C22C.Q0 to     R30C22B.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]
CTOF_DEL    ---     0.164     R30C22B.D1 to     R30C22B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230
ROUTE         1     0.379     R30C22B.F1 to     R30C22B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_en4_NE_i
CTOF_DEL    ---     0.164     R30C22B.B0 to     R30C22B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230
ROUTE         1     0.000     R30C22B.F0 to    R30C22B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/N_33094_0 (to clk_125_c)
                  --------
                    1.367   (44.1% logic, 55.9% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c

                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3230:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.844ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]  (to clk_125_c +)

   Delay:               1.088ns  (40.3% logic, 59.7% route), 2 logic levels.

 Constraint Details:

     1.088ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.844ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R30C22C.CLK to     R30C22C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 (from clk_125_c)
ROUTE         6     0.649     R30C22C.Q0 to     R30C22C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]
CTOF_DEL    ---     0.164     R30C22C.A1 to     R30C22C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258
ROUTE         1     0.000     R30C22C.F1 to    R30C22C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[1] (to clk_125_c)
                  --------
                    1.088   (40.3% logic, 59.7% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.866ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]  (to clk_125_c +)

   Delay:               1.066ns  (41.2% logic, 58.8% route), 2 logic levels.

 Constraint Details:

     1.066ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.866ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R30C22A.CLK to     R30C22A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 (from clk_125_c)
ROUTE         4     0.627     R30C22A.Q0 to     R30C22A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]
CTOF_DEL    ---     0.164     R30C22A.A0 to     R30C22A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259
ROUTE         1     0.000     R30C22A.F0 to    R30C22A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[2] (to clk_125_c)
                  --------
                    1.066   (41.2% logic, 58.8% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.866ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]  (to clk_125_c +)

   Delay:               1.066ns  (41.2% logic, 58.8% route), 2 logic levels.

 Constraint Details:

     1.066ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.866ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R30C22A.CLK to     R30C22A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 (from clk_125_c)
ROUTE         4     0.627     R30C22A.Q0 to     R30C22A.A1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]
CTOF_DEL    ---     0.164     R30C22A.A1 to     R30C22A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259
ROUTE         1     0.000     R30C22A.F1 to    R30C22A.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[3] (to clk_125_c)
                  --------
                    1.066   (41.2% logic, 58.8% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 4.871ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]  (to clk_125_c +)

   Delay:               1.061ns  (41.4% logic, 58.6% route), 2 logic levels.

 Constraint Details:

     1.061ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.871ns

 Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

```
   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R30C22C.CLK to     R30C22C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 (from clk_125_c)
ROUTE         5     0.622     R30C22C.Q1 to     R30C22C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]
CTOF_DEL    ---     0.164     R30C22C.B1 to     R30C22C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258
ROUTE         1     0.000     R30C22C.F1 to    R30C22C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[1] (to clk_125_c)
                  --------
                    1.061   (41.4% logic, 58.6% route), 2 logic levels.
```

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.
```

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.
```

Passed: The following path meets requirements by 4.894ns

Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

```
   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]  (to clk_125_c +)

   Delay:               1.038ns  (42.3% logic, 57.7% route), 2 logic levels.
```

Constraint Details:

```
     1.038ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.894ns
```

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

```
   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R30C22C.CLK to     R30C22C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 (from clk_125_c)
ROUTE         5     0.599     R30C22C.Q1 to     R30C22A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]
CTOF_DEL    ---     0.164     R30C22A.B1 to     R30C22A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259
ROUTE         1     0.000     R30C22A.F1 to    R30C22A.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[3] (to clk_125_c)
                  --------
                    1.038   (42.3% logic, 57.7% route), 2 logic levels.
```

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.
```

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.
```

Passed: The following path meets requirements by 4.971ns

Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

```
   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]  (to clk_125_c +)

   Delay:               0.961ns  (45.7% logic, 54.3% route), 2 logic levels.
```

Constraint Details:

```
     0.961ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 meets
     6.000ns delay constraint less
     0.000ns skew and
     0.068ns DIN_SET requirement (totaling 5.932ns) by 4.971ns
```

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

```
   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275    R30C22C.CLK to     R30C22C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 (from clk_125_c)
ROUTE         6     0.522     R30C22C.Q0 to     R30C22A.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]
CTOF_DEL    ---     0.164     R30C22A.C1 to     R30C22A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259
ROUTE         1     0.000     R30C22A.F1 to    R30C22A.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[3] (to clk_125_c)
                  --------
                    0.961   (45.7% logic, 54.3% route), 2 logic levels.
```

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.
```

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.
```

Report:  603.500MHz is the maximum frequency for this preference.

```
================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data*" 6.000000 ns ;
            16 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------
```

Passed: The following path meets requirements by 3.795ns

Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

```
   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[13]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM0

   Delay:               2.361ns  (18.6% logic, 81.4% route), 3 logic levels.
```

Constraint Details:

```
     2.361ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2795 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1385 meets
     6.000ns delay constraint less
     0.000ns skew and
    -0.156ns WD_SET requirement (totaling 6.156ns) by 3.795ns
```

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2795 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1385:

```
   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275      R50C5C.CLK to      R50C5C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2795 (from clk_125_c)
ROUTE         1     0.657      R50C5C.Q1 to      R43C5D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[13]
CTOF_DEL    ---     0.164      R43C5D.D0 to      R43C5D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9725
ROUTE         1     1.265      R43C5D.F0 to      R43C6C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[13]
ZERO_DEL    ---     0.000      R43C6C.B1 to    R43C6C.WDO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1384
ROUTE         1     0.000    R43C6C.WDO1 to     R43C6A.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT)
                  --------
                    2.361   (18.6% logic, 81.4% route), 3 logic levels.
```

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2795:

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R50C5C.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.
```

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1385:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R43C6C.CLK clk_125_c |
| ZERO_DEL | --- | 0.000 | R43C6C.CLK to | R43C6C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1384 |
| ROUTE | 2 | 0.000 | R43C6C.WCKO to | R43C6A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT |
| | | 1.415 | (0.0% logic, 100.0% route), 1 logic levels. | |

Passed: The following path meets requirements by 3.875ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

| | | | |
|---|---|---|---|
| Source: | FF | Q | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[3] (from clk_125_c +) |
| Destination: | FF | Data in | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +) |
| | FF | | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1 |

Delay: 2.281ns (19.2% logic, 80.8% route), 3 logic levels.

Constraint Details:

2.281ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2790 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1397 meets
6.000ns delay constraint less
0.000ns skew and
-0.156ns WD_SET requirement (totaling 6.156ns) by 3.875ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2790 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1397:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 | R50C5B.CLK to | R50C5B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2790 (from clk_125_c) |
| ROUTE | 1 | 1.078 | R50C5B.Q1 to | R48C4D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[3] |
| CTOF_DEL | --- | 0.164 | R48C4D.B0 to | R48C4D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9715 |
| ROUTE | 1 | 0.764 | R48C4D.F0 to | R48C5C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[3] |
| ZERO_DEL | --- | 0.000 | R48C5C.D1 to | R48C5C.WDO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1395 |
| ROUTE | 1 | 0.000 | R48C5C.WDO3 to | R48C5B.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT) |
| | | 2.281 | (19.2% logic, 80.8% route), 3 logic levels. | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2790:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R50C5B.CLK clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1397:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R48C5C.CLK clk_125_c |
| ZERO_DEL | --- | 0.000 | R48C5C.CLK to | R48C5C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1395 |
| ROUTE | 2 | 0.000 | R48C5C.WCKO to | R48C5B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT |
| | | 1.415 | (0.0% logic, 100.0% route), 1 logic levels. | |

Passed: The following path meets requirements by 3.890ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

| | | | |
|---|---|---|---|
| Source: | FF | Q | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[6] (from clk_125_c +) |
| Destination: | FF | Data in | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT +) |
| | FF | | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1 |

Delay: 2.266ns (19.4% logic, 80.6% route), 3 logic levels.

Constraint Details:

2.266ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2792 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1394 meets
6.000ns delay constraint less
0.000ns skew and
-0.156ns WD_SET requirement (totaling 6.156ns) by 3.890ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2792 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1394:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 | R49C7B.CLK to | R49C7B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2792 (from clk_125_c) |
| ROUTE | 1 | 1.086 | R49C7B.Q0 to | R45C7C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[6] |
| CTOF_DEL | --- | 0.164 | R45C7C.B0 to | R45C7C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9718 |
| ROUTE | 1 | 0.741 | R45C7C.F0 to | R43C7C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[6] |
| ZERO_DEL | --- | 0.000 | R43C7C.C1 to | R43C7C.WDO2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1392 |
| ROUTE | 1 | 0.000 | R43C7C.WDO2 to | R43C7B.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT) |
| | | 2.266 | (19.4% logic, 80.6% route), 3 logic levels. | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2792:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R49C7B.CLK clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1394:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R43C7C.CLK clk_125_c |
| ZERO_DEL | --- | 0.000 | R43C7C.CLK to | R43C7C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1392 |
| ROUTE | 2 | 0.000 | R43C7C.WCKO to | R43C7B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT |
| | | 1.415 | (0.0% logic, 100.0% route), 1 logic levels. | |

Passed: The following path meets requirements by 3.987ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

| | | | |
|---|---|---|---|
| Source: | FF | Q | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[12] (from clk_125_c +) |
| Destination: | FF | Data in | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM0 (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT +) |
| | FF | | pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM0 |

Delay: 2.169ns (20.2% logic, 79.8% route), 3 logic levels.

Constraint Details:

2.169ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2795 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1385 meets
6.000ns delay constraint less
0.000ns skew and
-0.156ns WD_SET requirement (totaling 6.156ns) by 3.987ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2795 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1385:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.275 | R50C5C.CLK to | R50C5C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2795 (from clk_125_c) |
| ROUTE | 1 | 0.805 | R50C5C.Q0 to | R46C5D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[12] |
| CTOF_DEL | --- | 0.164 | R46C5D.D0 to | R46C5D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9724 |
| ROUTE | 1 | 0.925 | R46C5D.F0 to | R43C6C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[12] |
| ZERO_DEL | --- | 0.000 | R43C6C.A1 to | R43C6C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1384 |
| ROUTE | 1 | 0.000 | R43C6C.WDO0 to | R43C6A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT) |
| | | 2.169 | (20.2% logic, 79.8% route), 3 logic levels. | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2795:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R50C5C.CLK clk_125_c |
| | | 1.415 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1385:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 1.415 | *FF_TX_H_CLK_0 to | R43C6C.CLK clk_125_c |
| ZERO_DEL | --- | 0.000 | R43C6C.CLK to | R43C6C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1384 |
| ROUTE | 2 | 0.000 | R43C6C.WCKO to | R43C6A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT |
| | | 1.415 | (0.0% logic, 100.0% route), 1 logic levels. | |

Passed: The following path meets requirements by 4.139ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

```
   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[9]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0

   Delay:               2.017ns  (21.8% logic, 78.2% route), 3 logic levels.

 Constraint Details:

      2.017ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2793 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1388 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.156ns WD_SET requirement (totaling 6.156ns) by 4.139ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2793 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1388:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R49C7C.CLK to      R49C7C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2793 (from clk_125_c)
ROUTE         1     0.588      R49C7C.Q1 to      R49C7D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[9]
CTOF_DEL    ---     0.164      R49C7D.B0 to      R49C7D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9721
ROUTE         1     0.990      R49C7D.F0 to      R48C6C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[9]
ZERO_DEL    ---     0.000     R48C6C.B1 to    R48C6C.WDO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1387
ROUTE         1     0.000    R48C6C.WDO1 to     R48C6A.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT)
                   --------
                     2.017   (21.8% logic, 78.2% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2793:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R49C7C.CLK clk_125_c
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1388:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R48C6C.CLK clk_125_c
ZERO_DEL    ---     0.000     R48C6C.CLK to    R48C6C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1387
ROUTE         2     0.000    R48C6C.WCKO to     R48C6A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT
                   --------
                     1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 4.144ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[14]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM1

   Delay:               2.012ns  (21.8% logic, 78.2% route), 3 logic levels.

 Constraint Details:

      2.012ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2796 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1386 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.156ns WD_SET requirement (totaling 6.156ns) by 4.144ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2796 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1386:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275      R50C7A.CLK to      R50C7A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2796 (from clk_125_c)
ROUTE         1     0.588      R50C7A.Q0 to      R49C7A.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[14]
CTOF_DEL    ---     0.164      R49C7A.B0 to      R49C7A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9726
ROUTE         1     0.985      R49C7A.F0 to      R43C6C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[14]
ZERO_DEL    ---     0.000      R43C6C.C1 to    R43C6C.WDO2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1384
ROUTE         1     0.000    R43C6C.WDO2 to     R43C6B.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT)
                   --------
                     2.012   (21.8% logic, 78.2% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2796:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R50C7A.CLK clk_125_c
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1386:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R43C6C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C6C.CLK to    R43C6C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1384
ROUTE         2     0.000    R43C6C.WCKO to     R43C6B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT
                   --------
                     1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 4.184ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[2]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1

   Delay:               1.972ns  (22.3% logic, 77.7% route), 3 logic levels.

 Constraint Details:

      1.972ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2790 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1397 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.156ns WD_SET requirement (totaling 6.156ns) by 4.184ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2790 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1397:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275      R50C5B.CLK to      R50C5B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2790 (from clk_125_c)
ROUTE         1     0.830      R50C5B.Q0 to      R49C4A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[2]
CTOF_DEL    ---     0.164      R49C4A.A0 to      R49C4A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9714
ROUTE         1     0.703      R49C4A.F0 to      R48C5C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[2]
ZERO_DEL    ---     0.000      R48C5C.C1 to    R48C5C.WDO2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1395
ROUTE         1     0.000    R48C5C.WDO2 to     R48C5B.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
                   --------
                     1.972   (22.3% logic, 77.7% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2790:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R50C5B.CLK clk_125_c
                   --------
                     1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1397:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R48C5C.CLK clk_125_c
ZERO_DEL    ---     0.000     R48C5C.CLK to    R48C5C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1395
ROUTE         2     0.000    R48C5C.WCKO to     R48C5B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
                   --------
                     1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 4.213ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[15]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM1

   Delay:               1.943ns  (22.6% logic, 77.4% route), 3 logic levels.

 Constraint Details:

      1.943ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2796 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1386 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.156ns WD_SET requirement (totaling 6.156ns) by 4.213ns
```

```
 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2796 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1386:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R50C7A.CLK to      R50C7A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2796 (from clk_125_c)
ROUTE         1     0.852      R50C7A.Q1 to      R45C7D.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[15]
CTOF_DEL    ---     0.164      R45C7D.C0 to      R45C7D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9727
ROUTE         1     0.652      R45C7D.F0 to      R43C6C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[15]
ZERO_DEL    ---     0.000      R43C6C.D1 to    R43C6C.WDO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1384
ROUTE         1     0.000    R43C6C.WDO3 to     R43C6B.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT)
                  --------
                    1.943   (22.6% logic, 77.4% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2796:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R50C7A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1386:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R43C6C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C6C.CLK to    R43C6C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1384
ROUTE         2     0.000    R43C6C.WCKO to     R43C6B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT
                  --------
                    1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 4.239ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[4]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM0

   Delay:               1.917ns  (22.9% logic, 77.1% route), 3 logic levels.

 Constraint Details:

      1.917ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2791 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1393 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.156ns WD_SET requirement (totaling 6.156ns) by 4.239ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2791 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1393:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R50C6A.CLK to      R50C6A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2791 (from clk_125_c)
ROUTE         1     0.863      R50C6A.Q0 to      R43C7D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[4]
CTOF_DEL    ---     0.164      R43C7D.D0 to      R43C7D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9716
ROUTE         1     0.615      R43C7D.F0 to      R43C7C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[4]
ZERO_DEL    ---     0.000      R43C7C.A1 to    R43C7C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1392
ROUTE         1     0.000    R43C7C.WDO0 to     R43C7A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT)
                  --------
                    1.917   (22.9% logic, 77.1% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2791:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R50C6A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1393:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R43C7C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C7C.CLK to    R43C7C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1392
ROUTE         2     0.000    R43C7C.WCKO to     R43C7A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT
                  --------
                    1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 4.270ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[7]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1

   Delay:               1.886ns  (23.3% logic, 76.7% route), 3 logic levels.

 Constraint Details:

      1.886ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2792 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1394 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.156ns WD_SET requirement (totaling 6.156ns) by 4.270ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2792 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1394:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275      R49C7B.CLK to      R49C7B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2792 (from clk_125_c)
ROUTE         1     0.588       R49C7B.Q1 to      R48C7B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[7]
CTOF_DEL    ---     0.164      R48C7B.B0 to      R48C7B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9719
ROUTE         1     0.859      R48C7B.F0 to      R43C7C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[7]
ZERO_DEL    ---     0.000      R43C7C.D1 to    R43C7C.WDO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1392
ROUTE         1     0.000    R43C7C.WDO3 to     R43C7B.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT)
                  --------
                    1.886   (23.3% logic, 76.7% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2792:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R49C7B.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1394:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R43C7C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C7C.CLK to    R43C7C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1392
ROUTE         2     0.000    R43C7C.WCKO to     R43C7B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT
                  --------
                    1.415   (0.0% logic, 100.0% route), 1 logic levels.

Report:  453.515MHz is the maximum frequency for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl*" 6.000000 ns ;
            2 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 3.891ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM0

   Delay:               2.265ns  (19.4% logic, 80.6% route), 3 logic levels.

 Constraint Details:

      2.265ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1382 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.156ns WD_SET requirement (totaling 6.156ns) by 3.891ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1382:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275      R49C5A.CLK to      R49C5A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798 (from clk_125_c)
```

```
ROUTE         1     0.898      R49C5A.Q1 to      R46C4B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/frm_kcntl_16[1]
CTOF_DEL    ---     0.164      R46C4B.B0 to      R46C4B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9711
ROUTE         1     0.928      R46C4B.F0 to      R43C4C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/frm_kcntl_16_m[1]
ZERO_DEL    ---     0.000      R43C4C.A1 to    R43C4C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1381
ROUTE         1     0.000    R43C4C.WDO0 to     R43C4A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT)
                  --------
                    2.265   (19.4% logic, 80.6% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R49C5A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1382:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R43C4C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C4C.CLK to    R43C4C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1381
ROUTE         2     0.000    R43C4C.WCKO to     R43C4A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT
                  --------
                    1.415   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 4.430ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/RAM0

   Delay:               1.726ns  (25.4% logic, 74.6% route), 3 logic levels.

 Constraint Details:

      1.726ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1391 meets
      6.000ns delay constraint less
      0.000ns skew and
     -0.156ns WD_SET requirement (totaling 6.156ns) by 4.430ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1391:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.275     R49C5A.CLK to      R49C5A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798 (from clk_125_c)
ROUTE         1     0.672      R49C5A.Q0 to      R43C4D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_kcntl_16[0]
CTOF_DEL    ---     0.164      R43C4D.D0 to      R43C4D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9710
ROUTE         1     0.615      R43C4D.F0 to      R43C3C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_kcntl_16_m[0]
ZERO_DEL    ---     0.000      R43C3C.A1 to    R43C3C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1390
ROUTE         1     0.000    R43C3C.WDO0 to     R43C3A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT)
                  --------
                    1.726   (25.4% logic, 74.6% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R49C5A.CLK clk_125_c
                  --------
                    1.415   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1391:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     1.415 *FF_TX_H_CLK_0 to     R43C3C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C3C.CLK to    R43C3C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1390
ROUTE         2     0.000    R43C3C.WCKO to     R43C3A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT
                  --------
                    1.415   (0.0% logic, 100.0% route), 1 logic levels.

Report:  474.158MHz is the maximum frequency for this preference.
```

## Report Summary

```
----------
--------------------------------------------------------------------------------
Preference                              |   Constraint|       Actual|Levels
--------------------------------------------------------------------------------
                                        |             |             |
FREQUENCY NET "clk_125_c" 125.000000    |             |             |
MHz ;                                   |  125.000 MHz|  132.031 MHz|  17
                                        |             |             |
FREQUENCY NET "can_clk_c" 25.000000 MHz |             |             |
;                                       |   25.000 MHz|   30.534 MHz|   4
                                        |             |             |
FREQUENCY NET "uart_clk_c" 25.000000    |             |             |
MHz ;                                   |   25.000 MHz|   39.801 MHz|   2
                                        |             |             |
FREQUENCY NET "pcie/pclk" 250.000000    |             |             |
MHz ;                                   |  250.000 MHz|  314.762 MHz|   3
                                        |             |             |
FREQUENCY NET                           |             |             |
"pcie/u1_pcs_pipe/ff_rx_fclk_0"         |             |             |
250.000000 MHz ;                        |  250.000 MHz|  412.201 MHz|   1
                                        |             |             |
MULTICYCLE FROM CELL                    |             |             |
"*nfts_rx_skp_cnt*" TO CELL             |             |             |
"*cnt_done_nfts_rx*" 2.000000 X ;       |    16.000 ns|     5.847 ns|  13
                                        |             |             |
MULTICYCLE FROM CELL                    |             |             |
"*nfts_rx_skp_cnt*" TO CELL             |             |             |
"*ltssm_nfts_rx_skp*" 2.000000 X ;      |    16.000 ns|     6.428 ns|   9
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr|             |             |
*" 6.000000 ns ;                        |  166.667 MHz|  635.728 MHz|   2
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr|             |             |
*" 6.000000 ns ;                        |  166.667 MHz|  267.094 MHz|   3
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr|             |             |
*" 6.000000 ns ;                        |  166.667 MHz|  739.098 MHz|   2
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr|             |             |
*" 6.000000 ns ;                        |  166.667 MHz|  603.500 MHz|   3
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_da|             |             |
ta*" 6.000000 ns ;                      |  166.667 MHz|  453.515 MHz|   3
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kc|             |             |
ntl*" 6.000000 ns ;                     |  166.667 MHz|  474.158 MHz|   3
                                        |             |             |
--------------------------------------------------------------------------------


All preferences were met.
```

## Clock Domains Analysis

```
----------------------

Found 8 clocks:

Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0   Loads: 3230
   Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr*" 6.000000 ns ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data*" 6.000000 ns ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl*" 6.000000 ns ;
   Covered under: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*cnt_done_nfts_rx*" 2.000000 X ;
   Covered under: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*ltssm_nfts_rx_skp*" 2.000000 X ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr*" 6.000000 ns ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr*" 6.000000 ns ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr*" 6.000000 ns ;

   Data transfers from:
   Clock Domain: can_clk_c   Source: pll_can/PLLInst_0.CLKOP
      Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ;   Transfers: 10

   Clock Domain: uart_clk_c   Source: pll_uarts/PLLInst_0.CLKOP
      Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ;   Transfers: 63

   Clock Domain: pcie/pclk   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_F_CLK_0
      Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ;   Transfers: 37
```

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: can_clk_c   Source: pll_can/PLLInst_0.CLKOP   Loads: 399
   Covered under: FREQUENCY NET "can_clk_c" 25.000000 MHz ;

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
      Covered under: FREQUENCY NET "can_clk_c" 25.000000 MHz ;   Transfers: 20

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: uart_clk_c   Source: pll_uarts/PLLInst_0.CLKOP   Loads: 1176
   Covered under: FREQUENCY NET "uart_clk_c" 25.000000 MHz ;

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
      Covered under: FREQUENCY NET "uart_clk_c" 25.000000 MHz ;   Transfers: 22

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: pcie/pclk   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_F_CLK_0   Loads: 192
   Covered under: FREQUENCY NET "pcie/pclk" 250.000000 MHz ;
   Blocked under: BLOCK PATH FROM CELL "*ctc_reset_chx*" ;

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
      Covered under: FREQUENCY NET "pcie/pclk" 250.000000 MHz ;   Transfers: 41

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: pcie/u1_pcs_pipe/ff_rx_fclk_0   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_RX_F_CLK_0   Loads: 1
   Covered under: FREQUENCY NET "pcie/u1_pcs_pipe/ff_rx_fclk_0" 250.000000 MHz ;

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
      Not reported because source and destination domains are unrelated.

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK   Loads: 653
   No transfer within this clock domain is found

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0

   Clock Domain: pcie/pclk   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_F_CLK_0

Clock Domain: ep5cht/rdcnt_inferred_clock_9   Source: ep5cht/SLICE_1098.Q0   Loads: 23
   No transfer within this clock domain is found

Clock Domain: ep5cht/lclk   Source: ep5cht/losc/SLICE_8253.F0   Loads: 10
   No transfer within this clock domain is found

## Timing summary (Setup):

---

Timing errors: 0  Score: 0
Cumulative negative slack: 0

Constraints cover 202945 paths, 114 nets, and 65996 connections (94.9% coverage)

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## Lattice TRACE Report - Hold, Version Diamond Version 2.0.0.154

Thu Jun 26 08:10:26 2014



## Report Information

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Command line:    trce -v 10 -gt -sethld -sp 7 -sphld m -o top_impl1.twr top_impl1.ncd top_impl1.prf
Design file:     top_impl1.ncd
Preference file: top_impl1.prf
Device,speed:    LFE3-35EA,m
Report level:    verbose report, limited to 10 items per preference
---

## Preference Summary

- FREQUENCY NET "clk_125_c" 125.000000 MHz (0 errors)
            4096 items scored, 0 timing errors detected.

- FREQUENCY NET "can_clk_c" 25.000000 MHz (0 errors)
            4096 items scored, 0 timing errors detected.

- FREQUENCY NET "uart_clk_c" 25.000000 MHz (0 errors)
            4096 items scored, 0 timing errors detected.

- FREQUENCY NET "pcie/pclk" 250.000000 MHz (0 errors)
            987 items scored, 0 timing errors detected.

- FREQUENCY NET "pcie/u1_pcs_pipe/ff_rx_fclk_0" 250.000000 MHz (0 errors)
            1 item scored, 0 timing errors detected.

- BLOCK PATH FROM PORT "rstn" (0 errors)
            119 items scored, 0 timing errors detected.

- BLOCK PATH TO PORT "OUT*" (0 errors)
            0 items scored, 0 timing errors detected.

- BLOCK PATH FROM PORT "INP*" (0 errors)
            16 items scored, 0 timing errors detected.

- BLOCK PATH FROM PORT "SRAM_A*" (0 errors)
            0 items scored, 0 timing errors detected.

- BLOCK PATH TO PORT "LED*" (0 errors)
            8 items scored, 0 timing errors detected.

- BLOCK PATH FROM CELL "*ctc_reset_chx*" (0 errors)
            14 items scored, 0 timing errors detected.

- MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*cnt_done_nfts_rx*" 2.000000 X (0 errors)
            214 items scored, 0 timing errors detected.

- MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*ltssm_nfts_rx_skp*" 2.000000 X (0 errors)
            244 items scored, 0 timing errors detected.

- MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr*" 6.000000 ns (0 errors)
            33 items scored, 0 timing errors detected.

- MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr*" 6.000000 ns (0 errors)
            147 items scored, 0 timing errors detected.

- MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr*" 6.000000 ns (0 errors)
            14 items scored, 0 timing errors detected.

- MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr*" 6.000000 ns (0 errors)
            18 items scored, 0 timing errors detected.

- MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data*" 6.000000 ns (0 errors)
            16 items scored, 0 timing errors detected.

- MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl*" 6.000000 ns (0 errors)
            2 items scored, 0 timing errors detected.

42 potential circuit loops found in timing analysis.
BLOCK ASYNCPATHS
BLOCK RESETPATHS
BLOCK JTAG PATHS
---

================================================================================
Preference: FREQUENCY NET "clk_125_c" 125.000000 MHz ;
            4096 items scored, 0 timing errors detected.
---

Passed: The following path meets requirements by 0.053ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/tlp_size[9]  (from clk_125_c +)
   Destination:    PDPW16KC   Port          pcie/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/u1_atbl_mem/pmi_ram_dpEbnonessen208146208146_0_0_0(ASIC)  (to clk_125_c +)

   Delay:               0.219ns  (42.5% logic, 57.5% route), 1 logic levels.

 Constraint Details:

      0.219ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/SLICE_803 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/u1_atbl_mem/pmi_ram_dpEbnonessen208146208146_0_0_0 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.053ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/SLICE_803 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/u1_atbl_mem/pmi_ram_dpEbnonessen208146208146_0_0_0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R52C18C.CLK to     R52C18C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/SLICE_803 (from clk_125_c)
ROUTE         3     0.126     R52C18C.Q0 to *R_R53C17.DI19 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/tlp_size[9] (to clk_125_c)
                  --------
                    0.219   (42.5% logic, 57.5% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/SLICE_803:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R52C18C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dll/u1_txtp/u1_txtp_rtry/u1_atbl_mem/pmi_ram_dpEbnonessen208146208146_0_0_0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to *R_R53C17.CLKW clk_125_c
                  --------
                    0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.055ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[337]  (from clk_125_c +)
   Destination:    PDPW16KC   Port          top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_9_3(ASIC)  (to clk_125_c +)

   Delay:               0.221ns  (42.1% logic, 57.9% route), 1 logic levels.

 Constraint Details:

      0.221ns physical path delay top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4836 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_9_3 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.055ns

 Physical Path Details:

      Data path top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4836 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_9_3:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R9C43B.CLK to      R9C43B.Q0 top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4836 (from clk_125_c)
ROUTE         1     0.128      R9C43B.Q0 to EBR_R8C41.DI13 top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[337] (to clk_125_c)
                  --------
                    0.221   (42.1% logic, 57.9% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4836:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R9C43B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_9_3:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to EBR_R8C41.CLKW clk_125_c
                  --------
                    0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.055ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[433]  (from clk_125_c +)
   Destination:    PDPW16KC   Port          top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_12_0(ASIC)  (to clk_125_c +)

   Delay:               0.221ns  (42.1% logic, 57.9% route), 1 logic levels.

 Constraint Details:

      0.221ns physical path delay top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4884 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_12_0 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.055ns

 Physical Path Details:

      Data path top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4884 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_12_0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R18C54A.CLK to     R18C54A.Q0 top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4884 (from clk_125_c)
ROUTE         1     0.128     R18C54A.Q0 to EBR_R17C53.DI1 top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[433] (to clk_125_c)
                  --------
                    0.221   (42.1% logic, 57.9% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4884:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R18C54A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_12_0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to *R_R17C53.CLKW clk_125_c
                  --------
                    0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.055ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[341]  (from clk_125_c +)
   Destination:    PDPW16KC   Port          top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_9_3(ASIC)  (to clk_125_c +)

   Delay:               0.221ns  (42.1% logic, 57.9% route), 1 logic levels.

 Constraint Details:

      0.221ns physical path delay top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4838 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_9_3 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.055ns

 Physical Path Details:

      Data path top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4838 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_9_3:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R9C41A.CLK to      R9C41A.Q0 top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4838 (from clk_125_c)
ROUTE         1     0.128      R9C41A.Q0 to EBR_R8C41.DI17 top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[341] (to clk_125_c)
                  --------
                    0.221   (42.1% logic, 57.9% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4838:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R9C41A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_9_3:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to EBR_R8C41.CLKW clk_125_c
                  --------
                    0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.070ns

```
 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[34]  (from clk_125_c +)
   Destination:    PDPW16KC   Port           top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_0_12(ASIC)  (to clk_125_c +)

   Delay:               0.236ns  (39.4% logic, 60.6% route), 1 logic levels.

 Constraint Details:

      0.236ns physical path delay top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4719 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_0_12 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.070ns

 Physical Path Details:

      Data path top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4719 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_0_12:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R36C32A.CLK to     R36C32A.Q1 top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4719 (from clk_125_c)
ROUTE         1     0.143     R36C32A.Q1 to *R_R35C32.DI34 top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[34] (to clk_125_c)
                   --------
                     0.236   (39.4% logic, 60.6% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4719:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R36C32A.CLK clk_125_c
                   --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_0_12:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to *R_R35C32.CLKW clk_125_c
                   --------
                     0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.070ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[434]  (from clk_125_c +)
   Destination:    PDPW16KC   Port           top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_12_0(ASIC)  (to clk_125_c +)

   Delay:               0.236ns  (39.4% logic, 60.6% route), 1 logic levels.

 Constraint Details:

      0.236ns physical path delay top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4884 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_12_0 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.070ns

 Physical Path Details:

      Data path top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4884 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_12_0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R18C54A.CLK to     R18C54A.Q1 top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4884 (from clk_125_c)
ROUTE         1     0.143     R18C54A.Q1 to EBR_R17C53.DI2 top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[434] (to clk_125_c)
                   --------
                     0.236   (39.4% logic, 60.6% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4884:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R18C54A.CLK clk_125_c
                   --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_12_0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to *R_R17C53.CLKW clk_125_c
                   --------
                     0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.070ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[95]  (from clk_125_c +)
   Destination:    PDPW16KC   Port           top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_2_10(ASIC)  (to clk_125_c +)

   Delay:               0.236ns  (39.4% logic, 60.6% route), 1 logic levels.

 Constraint Details:

      0.236ns physical path delay top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4746 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_2_10 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.070ns

 Physical Path Details:

      Data path top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4746 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_2_10:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R18C39C.CLK to     R18C39C.Q0 top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4746 (from clk_125_c)
ROUTE         1     0.143     R18C39C.Q0 to *R_R17C38.DI23 top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[95] (to clk_125_c)
                   --------
                     0.236   (39.4% logic, 60.6% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4746:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R18C39C.CLK clk_125_c
                   --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_2_10:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to *R_R17C38.CLKW clk_125_c
                   --------
                     0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.106ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[29]  (from clk_125_c +)
   Destination:    PDPW16KC   Port           top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_0_12(ASIC)  (to clk_125_c +)

   Delay:               0.272ns  (34.2% logic, 65.8% route), 1 logic levels.

 Constraint Details:

      0.272ns physical path delay top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4717 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_0_12 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.106ns

 Physical Path Details:

      Data path top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4717 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_0_12:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R33C33C.CLK to     R33C33C.Q0 top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4717 (from clk_125_c)
ROUTE         1     0.179     R33C33C.Q0 to *R_R35C32.DI29 top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[29] (to clk_125_c)
                   --------
                     0.272   (34.2% logic, 65.8% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4717:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R33C33C.CLK clk_125_c
                   --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_0_12:
```

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to *R_R35C32.CLKW clk_125_c
                    --------
                     0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.106ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[74]  (from clk_125_c +)
   Destination:    PDPW16KC   Port           top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_2_10(ASIC)  (to clk_125_c +)

   Delay:               0.272ns  (34.2% logic, 65.8% route), 1 logic levels.

 Constraint Details:

      0.272ns physical path delay top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4739 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_2_10 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.106ns

 Physical Path Details:

      Data path top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4739 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_2_10:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R19C39B.CLK to     R19C39B.Q1 top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4739 (from clk_125_c)
ROUTE         1     0.179     R19C39B.Q1 to EBR_R17C38.DI2 top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[74] (to clk_125_c)
                    --------
                     0.272   (34.2% logic, 65.8% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4739:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R19C39B.CLK clk_125_c
                    --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_2_10:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to *R_R17C38.CLKW clk_125_c
                    --------
                     0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.106ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[290]  (from clk_125_c +)
   Destination:    PDPW16KC   Port           top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_8_4(ASIC)  (to clk_125_c +)

   Delay:               0.272ns  (34.2% logic, 65.8% route), 1 logic levels.

 Constraint Details:

      0.272ns physical path delay top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4812 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_8_4 meets
      0.107ns DATA_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.166ns) by 0.106ns

 Physical Path Details:

      Data path top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4812 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_8_4:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R16C43B.CLK to     R16C43B.Q0 top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4812 (from clk_125_c)
ROUTE         1     0.179     R16C43B.Q0 to EBR_R17C44.DI2 top_reveal_coretop_instance/top_la0_inst_0/tm_u/trace_din_d[290] (to clk_125_c)
                    --------
                     0.272   (34.2% logic, 65.8% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/SLICE_4812:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R16C43B.CLK clk_125_c
                    --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to top_reveal_coretop_instance/top_la0_inst_0/tm_u/genblk4.tr_mem/pmi_ram_dpEbnonesadr45995124599512_0_8_4:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.586 *FF_TX_H_CLK_0 to *R_R17C44.CLKW clk_125_c
                    --------
                     0.586   (0.0% logic, 100.0% route), 0 logic levels.


================================================================================
Preference: FREQUENCY NET "can_clk_c" 25.000000 MHz ;
            4096 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.151ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              can/i_can_bsp/i_can_fifo/wr_info_pointer[3]  (from can_clk_c +)
   Destination:    FF         Data in        can/i_can_bsp/i_can_fifo/length_fifo_ram_0/RAM1  (to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WCK_INT +)
                   FF                        can/i_can_bsp/i_can_fifo/length_fifo_ram_0/RAM1

   Delay:               0.255ns  (36.5% logic, 63.5% route), 2 logic levels.

 Constraint Details:

      0.255ns physical path delay can/i_can_bsp/i_can_fifo/SLICE_1617 to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1162 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.151ns

 Physical Path Details:

      Data path can/i_can_bsp/i_can_fifo/SLICE_1617 to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1162:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R36C53A.CLK to     R36C53A.Q1 can/i_can_bsp/i_can_fifo/SLICE_1617 (from can_clk_c)
ROUTE        10     0.162     R36C53A.Q1 to     R34C53C.D0 can/i_can_bsp/i_can_fifo/wr_info_pointer[3]
ZERO_DEL    ---     0.000     R34C53C.D0 to  R34C53C.WADO3 can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1160
ROUTE         2     0.000  R34C53C.WADO3 to   R34C53B.WAD3 can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WAD3_INT (to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WCK_INT)
                    --------
                     0.255   (36.5% logic, 63.5% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/SLICE_1617:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       399     0.488 *_R53C70.CLKOP to    R36C53A.CLK can_clk_c
                    --------
                     0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1162:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       399     0.488 *_R53C70.CLKOP to    R34C53C.CLK can_clk_c
ZERO_DEL    ---     0.000    R34C53C.CLK to   R34C53C.WCKO can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1160
ROUTE         2     0.000   R34C53C.WCKO to    R34C53B.WCK can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WCK_INT
                    --------
                     0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.151ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              can/i_can_bsp/i_can_fifo/wr_info_pointer[3]  (from can_clk_c +)
   Destination:    FF         Data in        can/i_can_bsp/i_can_fifo/length_fifo_ram_0/RAM0  (to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WCK_INT +)
                   FF                        can/i_can_bsp/i_can_fifo/length_fifo_ram_0/RAM0

   Delay:               0.255ns  (36.5% logic, 63.5% route), 2 logic levels.

 Constraint Details:

      0.255ns physical path delay can/i_can_bsp/i_can_fifo/SLICE_1617 to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1161 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.151ns

 Physical Path Details:
```

Data path can/i_can_bsp/i_can_fifo/SLICE_1617 to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1161:

```
   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R36C53A.CLK to     R36C53A.Q1 can/i_can_bsp/i_can_fifo/SLICE_1617 (from can_clk_c)
ROUTE        10     0.162     R36C53A.Q1 to     R34C53C.D0 can/i_can_bsp/i_can_fifo/wr_info_pointer[3]
ZERO_DEL    ---     0.000     R34C53C.D0 to  R34C53C.WADO3 can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1160
ROUTE         2     0.000  R34C53C.WADO3 to   R34C53A.WAD3 can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WAD3_INT (to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WCK_INT)
                  --------
                    0.255   (36.5% logic, 63.5% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/SLICE_1617:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       399     0.488 *_R53C70.CLKOP to    R36C53A.CLK can_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1161:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       399     0.488 *_R53C70.CLKOP to    R34C53C.CLK can_clk_c
ZERO_DEL    ---     0.000    R34C53C.CLK to   R34C53C.WCKO can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1160
ROUTE         2     0.000   R34C53C.WCKO to    R34C53A.WCK can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.186ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             can/i_can_bsp/i_can_fifo/wr_pointer[3]  (from can_clk_c +)
   Destination:    FF         Data in       can/i_can_bsp/i_can_fifo/fifo_ram_4/RAM0  (to can/i_can_bsp/i_can_fifo/fifo_ram_4/WCK_INT +)
                   FF                       can/i_can_bsp/i_can_fifo/fifo_ram_4/RAM0

   Delay:               0.290ns  (32.1% logic, 67.9% route), 2 logic levels.

 Constraint Details:

      0.290ns physical path delay can/i_can_bsp/i_can_fifo/SLICE_7 to can/i_can_bsp/i_can_fifo/fifo_ram_4/SLICE_1137 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.186ns

 Physical Path Details:

      Data path can/i_can_bsp/i_can_fifo/SLICE_7 to can/i_can_bsp/i_can_fifo/fifo_ram_4/SLICE_1137:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R25C51C.CLK to     R25C51C.Q0 can/i_can_bsp/i_can_fifo/SLICE_7 (from can_clk_c)
ROUTE         9     0.197     R25C51C.Q0 to     R25C45C.D0 can/i_can_bsp/i_can_fifo/wr_pointer[3]
ZERO_DEL    ---     0.000     R25C45C.D0 to  R25C45C.WADO3 can/i_can_bsp/i_can_fifo/fifo_ram_4/SLICE_1136
ROUTE         2     0.000  R25C45C.WADO3 to   R25C45A.WAD3 can/i_can_bsp/i_can_fifo/fifo_ram_4/WAD3_INT (to can/i_can_bsp/i_can_fifo/fifo_ram_4/WCK_INT)
                  --------
                    0.290   (32.1% logic, 67.9% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/SLICE_7:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       399     0.488 *_R53C70.CLKOP to    R25C51C.CLK can_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/fifo_ram_4/SLICE_1137:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       399     0.488 *_R53C70.CLKOP to    R25C45C.CLK can_clk_c
ZERO_DEL    ---     0.000    R25C45C.CLK to   R25C45C.WCKO can/i_can_bsp/i_can_fifo/fifo_ram_4/SLICE_1136
ROUTE         2     0.000   R25C45C.WCKO to    R25C45A.WCK can/i_can_bsp/i_can_fifo/fifo_ram_4/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.186ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             can/i_can_bsp/i_can_fifo/wr_pointer[3]  (from can_clk_c +)
   Destination:    FF         Data in       can/i_can_bsp/i_can_fifo/fifo_ram_4/RAM1  (to can/i_can_bsp/i_can_fifo/fifo_ram_4/WCK_INT +)
                   FF                       can/i_can_bsp/i_can_fifo/fifo_ram_4/RAM1

   Delay:               0.290ns  (32.1% logic, 67.9% route), 2 logic levels.

 Constraint Details:

      0.290ns physical path delay can/i_can_bsp/i_can_fifo/SLICE_7 to can/i_can_bsp/i_can_fifo/fifo_ram_4/SLICE_1138 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.186ns

 Physical Path Details:

      Data path can/i_can_bsp/i_can_fifo/SLICE_7 to can/i_can_bsp/i_can_fifo/fifo_ram_4/SLICE_1138:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R25C51C.CLK to     R25C51C.Q0 can/i_can_bsp/i_can_fifo/SLICE_7 (from can_clk_c)
ROUTE         9     0.197     R25C51C.Q0 to     R25C45C.D0 can/i_can_bsp/i_can_fifo/wr_pointer[3]
ZERO_DEL    ---     0.000     R25C45C.D0 to  R25C45C.WADO3 can/i_can_bsp/i_can_fifo/fifo_ram_4/SLICE_1136
ROUTE         2     0.000  R25C45C.WADO3 to   R25C45B.WAD3 can/i_can_bsp/i_can_fifo/fifo_ram_4/WAD3_INT (to can/i_can_bsp/i_can_fifo/fifo_ram_4/WCK_INT)
                  --------
                    0.290   (32.1% logic, 67.9% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/SLICE_7:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       399     0.488 *_R53C70.CLKOP to    R25C51C.CLK can_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/fifo_ram_4/SLICE_1138:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       399     0.488 *_R53C70.CLKOP to    R25C45C.CLK can_clk_c
ZERO_DEL    ---     0.000    R25C45C.CLK to   R25C45C.WCKO can/i_can_bsp/i_can_fifo/fifo_ram_4/SLICE_1136
ROUTE         2     0.000   R25C45C.WCKO to    R25C45B.WCK can/i_can_bsp/i_can_fifo/fifo_ram_4/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.188ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             can/i_can_bsp/i_can_fifo/wr_info_pointer[2]  (from can_clk_c +)
   Destination:    FF         Data in       can/i_can_bsp/i_can_fifo/length_fifo_ram_0/RAM0  (to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WCK_INT +)
                   FF                       can/i_can_bsp/i_can_fifo/length_fifo_ram_0/RAM0

   Delay:               0.292ns  (31.8% logic, 68.2% route), 2 logic levels.

 Constraint Details:

      0.292ns physical path delay can/i_can_bsp/i_can_fifo/SLICE_1617 to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1161 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.188ns

 Physical Path Details:

      Data path can/i_can_bsp/i_can_fifo/SLICE_1617 to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1161:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R36C53A.CLK to     R36C53A.Q0 can/i_can_bsp/i_can_fifo/SLICE_1617 (from can_clk_c)
ROUTE        10     0.199     R36C53A.Q0 to     R34C53C.C0 can/i_can_bsp/i_can_fifo/wr_info_pointer[2]
ZERO_DEL    ---     0.000     R34C53C.C0 to  R34C53C.WADO2 can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1160
ROUTE         2     0.000  R34C53C.WADO2 to   R34C53A.WAD2 can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WAD2_INT (to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WCK_INT)
                  --------
                    0.292   (31.8% logic, 68.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/SLICE_1617:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       399     0.488 *_R53C70.CLKOP to    R36C53A.CLK can_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.
```

Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1161:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 399 | 0.488 | *_R53C70.CLKOP to | R34C53C.CLK can_clk_c |
| ZERO_DEL | --- | 0.000 | R34C53C.CLK to | R34C53C.WCKO can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1160 |
| ROUTE | 2 | 0.000 | R34C53C.WCKO to | R34C53A.WCK can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WCK_INT |
| | | 0.488 | (0.0% logic, 100.0% route), 1 logic levels. | |

Passed: The following path meets requirements by 0.188ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

| | | | |
|---|---|---|---|
| Source: | FF | Q | can/i_can_bsp/i_can_fifo/wr_info_pointer[2] (from can_clk_c +) |
| Destination: | FF | Data in | can/i_can_bsp/i_can_fifo/length_fifo_ram_0/RAM1 (to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WCK_INT +) |
| | FF | | can/i_can_bsp/i_can_fifo/length_fifo_ram_0/RAM1 |

Delay: 0.292ns (31.8% logic, 68.2% route), 2 logic levels.

Constraint Details:

0.292ns physical path delay can/i_can_bsp/i_can_fifo/SLICE_1617 to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1162 meets
0.104ns WAD_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling 0.104ns) by 0.188ns

Physical Path Details:

Data path can/i_can_bsp/i_can_fifo/SLICE_1617 to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1162:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.093 | R36C53A.CLK to | R36C53A.Q0 can/i_can_bsp/i_can_fifo/SLICE_1617 (from can_clk_c) |
| ROUTE | 10 | 0.199 | R36C53A.Q0 to | R34C53C.C0 can/i_can_bsp/i_can_fifo/wr_info_pointer[2] |
| ZERO_DEL | --- | 0.000 | R34C53C.C0 to | R34C53C.WADO2 can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1160 |
| ROUTE | 2 | 0.000 | R34C53C.WADO2 to | R34C53B.WAD2 can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WAD2_INT (to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WCK_INT) |
| | | 0.292 | (31.8% logic, 68.2% route), 2 logic levels. | |

Clock Skew Details:

Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/SLICE_1617:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 399 | 0.488 | *_R53C70.CLKOP to | R36C53A.CLK can_clk_c |
| | | 0.488 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1162:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 399 | 0.488 | *_R53C70.CLKOP to | R34C53C.CLK can_clk_c |
| ZERO_DEL | --- | 0.000 | R34C53C.CLK to | R34C53C.WCKO can/i_can_bsp/i_can_fifo/length_fifo_ram_0/SLICE_1160 |
| ROUTE | 2 | 0.000 | R34C53C.WCKO to | R34C53B.WCK can/i_can_bsp/i_can_fifo/length_fifo_ram_0/WCK_INT |
| | | 0.488 | (0.0% logic, 100.0% route), 1 logic levels. | |

Passed: The following path meets requirements by 0.200ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

| | | | |
|---|---|---|---|
| Source: | FF | Q | can/i_can_btl/tx_point (from can_clk_c +) |
| Destination: | FF | Data in | can/i_can_btl/tx_point (to can_clk_c +) |

Delay: 0.189ns (78.8% logic, 21.2% route), 2 logic levels.

Constraint Details:

0.189ns physical path delay can/i_can_btl/SLICE_1835 to can/i_can_btl/SLICE_1835 meets
-0.011ns DIN_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.011ns) by 0.200ns

Physical Path Details:

Data path can/i_can_btl/SLICE_1835 to can/i_can_btl/SLICE_1835:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.093 | R14C57B.CLK to | R14C57B.Q0 can/i_can_btl/SLICE_1835 (from can_clk_c) |
| ROUTE | 23 | 0.040 | R14C57B.Q0 to | R14C57B.D0 can/tx_point |
| CTOF_DEL | --- | 0.056 | R14C57B.D0 to | R14C57B.F0 can/i_can_btl/SLICE_1835 |
| ROUTE | 1 | 0.000 | R14C57B.F0 to | R14C57B.DI0 can/i_can_btl/tx_point_2 (to can_clk_c) |
| | | 0.189 | (78.8% logic, 21.2% route), 2 logic levels. | |

Clock Skew Details:

Source Clock Path pll_can/PLLInst_0 to can/i_can_btl/SLICE_1835:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 399 | 0.488 | *_R53C70.CLKOP to | R14C57B.CLK can_clk_c |
| | | 0.488 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pll_can/PLLInst_0 to can/i_can_btl/SLICE_1835:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 399 | 0.488 | *_R53C70.CLKOP to | R14C57B.CLK can_clk_c |
| | | 0.488 | (0.0% logic, 100.0% route), 0 logic levels. | |

Passed: The following path meets requirements by 0.200ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

| | | | |
|---|---|---|---|
| Source: | FF | Q | can/i_can_bsp/error_cnt2_fast[2] (from can_clk_c +) |
| Destination: | FF | Data in | can/i_can_bsp/error_cnt2_fast[2] (to can_clk_c +) |

Delay: 0.189ns (78.8% logic, 21.2% route), 2 logic levels.

Constraint Details:

0.189ns physical path delay can/i_can_bsp/SLICE_1600 to can/i_can_bsp/SLICE_1600 meets
-0.011ns DIN_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.011ns) by 0.200ns

Physical Path Details:

Data path can/i_can_bsp/SLICE_1600 to can/i_can_bsp/SLICE_1600:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.093 | R13C63B.CLK to | R13C63B.Q0 can/i_can_bsp/SLICE_1600 (from can_clk_c) |
| ROUTE | 2 | 0.040 | R13C63B.Q0 to | R13C63B.D0 can/i_can_bsp/error_cnt2_fast[2] |
| CTOF_DEL | --- | 0.056 | R13C63B.D0 to | R13C63B.F0 can/i_can_bsp/SLICE_1600 |
| ROUTE | 1 | 0.000 | R13C63B.F0 to | R13C63B.DI0 can/i_can_bsp/error_cnt2_3_fast[2] (to can_clk_c) |
| | | 0.189 | (78.8% logic, 21.2% route), 2 logic levels. | |

Clock Skew Details:

Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/SLICE_1600:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 399 | 0.488 | *_R53C70.CLKOP to | R13C63B.CLK can_clk_c |
| | | 0.488 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/SLICE_1600:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 399 | 0.488 | *_R53C70.CLKOP to | R13C63B.CLK can_clk_c |
| | | 0.488 | (0.0% logic, 100.0% route), 0 logic levels. | |

Passed: The following path meets requirements by 0.200ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

| | | | |
|---|---|---|---|
| Source: | FF | Q | can/i_can_bsp/delayed_dominant_cnt[0] (from can_clk_c +) |
| Destination: | FF | Data in | can/i_can_bsp/delayed_dominant_cnt[0] (to can_clk_c +) |

Delay: 0.189ns (78.8% logic, 21.2% route), 2 logic levels.

Constraint Details:

0.189ns physical path delay can/i_can_bsp/SLICE_1586 to can/i_can_bsp/SLICE_1586 meets
-0.011ns DIN_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.011ns) by 0.200ns

```
 Physical Path Details:

      Data path can/i_can_bsp/SLICE_1586 to can/i_can_bsp/SLICE_1586:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R9C65A.CLK to      R9C65A.Q0 can/i_can_bsp/SLICE_1586 (from can_clk_c)
ROUTE         4     0.040      R9C65A.Q0 to      R9C65A.D0 can/i_can_bsp/delayed_dominant_cnt[0]
CTOF_DEL    ---     0.056      R9C65A.D0 to      R9C65A.F0 can/i_can_bsp/SLICE_1586
ROUTE         1     0.000      R9C65A.F0 to     R9C65A.DI0 can/i_can_bsp/delayed_dominant_cnt_3[0] (to can_clk_c)
                  --------
                    0.189   (78.8% logic, 21.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_can/PLLInst_0 to can/i_can_bsp/SLICE_1586:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       399     0.488 *_R53C70.CLKOP to     R9C65A.CLK can_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_can/PLLInst_0 to can/i_can_bsp/SLICE_1586:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       399     0.488 *_R53C70.CLKOP to     R9C65A.CLK can_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.200ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             can/i_can_btl/tx_point_fast  (from can_clk_c +)
   Destination:    FF         Data in       can/i_can_btl/tx_point_fast  (to can_clk_c +)

   Delay:               0.189ns  (78.8% logic, 21.2% route), 2 logic levels.

 Constraint Details:

      0.189ns physical path delay can/i_can_btl/SLICE_1836 to can/i_can_btl/SLICE_1836 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.200ns

 Physical Path Details:

      Data path can/i_can_btl/SLICE_1836 to can/i_can_btl/SLICE_1836:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R14C57A.CLK to     R14C57A.Q0 can/i_can_btl/SLICE_1836 (from can_clk_c)
ROUTE         4     0.040     R14C57A.Q0 to     R14C57A.D0 can/tx_point_fast
CTOF_DEL    ---     0.056     R14C57A.D0 to     R14C57A.F0 can/i_can_btl/SLICE_1836
ROUTE         1     0.000     R14C57A.F0 to    R14C57A.DI0 can/i_can_btl/tx_point_2_fast (to can_clk_c)
                  --------
                    0.189   (78.8% logic, 21.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_can/PLLInst_0 to can/i_can_btl/SLICE_1836:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       399     0.488 *_R53C70.CLKOP to    R14C57A.CLK can_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_can/PLLInst_0 to can/i_can_btl/SLICE_1836:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       399     0.488 *_R53C70.CLKOP to    R14C57A.CLK can_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.


================================================================================
Preference: FREQUENCY NET "uart_clk_c" 25.000000 MHz ;
            4096 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.075ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             uart2/regs/transmitter/fifo_tx/top[3]  (from uart_clk_c +)
   Destination:    FF         Data in       uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM1  (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT +)
                   FF                       uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM1

   Delay:               0.179ns  (52.0% logic, 48.0% route), 2 logic levels.

 Constraint Details:

      0.179ns physical path delay uart2/regs/transmitter/fifo_tx/SLICE_5567 to uart2/regs/transmitter/SLICE_1233 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.075ns

 Physical Path Details:

      Data path uart2/regs/transmitter/fifo_tx/SLICE_5567 to uart2/regs/transmitter/SLICE_1233:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R24C67A.CLK to     R24C67A.Q1 uart2/regs/transmitter/fifo_tx/SLICE_5567 (from uart_clk_c)
ROUTE         3     0.086     R24C67A.Q1 to     R25C67C.D0 uart2/regs/transmitter/fifo_tx/top[3]
ZERO_DEL    ---     0.000     R25C67C.D0 to  R25C67C.WADO3 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1231
ROUTE         2     0.000  R25C67C.WADO3 to   R25C67B.WAD3 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WAD3_INT (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT)
                  --------
                    0.179   (52.0% logic, 48.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/SLICE_5567:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R24C67A.CLK uart_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/SLICE_1233:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R25C67C.CLK uart_clk_c
ZERO_DEL    ---     0.000    R25C67C.CLK to   R25C67C.WCKO uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1231
ROUTE         2     0.000   R25C67C.WCKO to    R25C67B.WCK uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.075ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             uart2/regs/transmitter/fifo_tx/top[3]  (from uart_clk_c +)
   Destination:    FF         Data in       uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM0  (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT +)
                   FF                       uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM0

   Delay:               0.179ns  (52.0% logic, 48.0% route), 2 logic levels.

 Constraint Details:

      0.179ns physical path delay uart2/regs/transmitter/fifo_tx/SLICE_5567 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1232 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.075ns

 Physical Path Details:

      Data path uart2/regs/transmitter/fifo_tx/SLICE_5567 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1232:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R24C67A.CLK to     R24C67A.Q1 uart2/regs/transmitter/fifo_tx/SLICE_5567 (from uart_clk_c)
ROUTE         3     0.086     R24C67A.Q1 to     R25C67C.D0 uart2/regs/transmitter/fifo_tx/top[3]
ZERO_DEL    ---     0.000     R25C67C.D0 to  R25C67C.WADO3 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1231
ROUTE         2     0.000  R25C67C.WADO3 to   R25C67A.WAD3 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WAD3_INT (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT)
                  --------
                    0.179   (52.0% logic, 48.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/SLICE_5567:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R24C67A.CLK uart_clk_c
                  --------
```

                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R25C67C.CLK uart_clk_c
ZERO_DEL    ---     0.000    R25C67C.CLK to   R25C67C.WCKO uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1231
ROUTE         2     0.000   R25C67C.WCKO to    R25C67A.WCK uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.096ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             uart2/regs/transmitter/fifo_tx/top[2]  (from uart_clk_c +)
   Destination:    FF         Data in       uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM0  (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT +)
                   FF                       uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM0

   Delay:               0.200ns  (46.5% logic, 53.5% route), 2 logic levels.

 Constraint Details:

     0.200ns physical path delay uart2/regs/transmitter/fifo_tx/SLICE_5567 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1232 meets
     0.104ns WAD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.104ns) by 0.096ns

 Physical Path Details:

     Data path uart2/regs/transmitter/fifo_tx/SLICE_5567 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1232:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R24C67A.CLK to     R24C67A.Q0 uart2/regs/transmitter/fifo_tx/SLICE_5567 (from uart_clk_c)
ROUTE         4     0.107     R24C67A.Q0 to     R25C67C.C0 uart2/regs/transmitter/fifo_tx/top[2]
ZERO_DEL    ---     0.000     R25C67C.C0 to  R25C67C.WADO2 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1231
ROUTE         2     0.000  R25C67C.WADO2 to   R25C67A.WAD2 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WAD2_INT (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT)
                  --------
                    0.200   (46.5% logic, 53.5% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/SLICE_5567:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R24C67A.CLK uart_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R25C67C.CLK uart_clk_c
ZERO_DEL    ---     0.000    R25C67C.CLK to   R25C67C.WCKO uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1231
ROUTE         2     0.000   R25C67C.WCKO to    R25C67A.WCK uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.096ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             uart2/regs/transmitter/fifo_tx/top[2]  (from uart_clk_c +)
   Destination:    FF         Data in       uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM1  (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT +)
                   FF                       uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM1

   Delay:               0.200ns  (46.5% logic, 53.5% route), 2 logic levels.

 Constraint Details:

     0.200ns physical path delay uart2/regs/transmitter/fifo_tx/SLICE_5567 to uart2/regs/transmitter/SLICE_1233 meets
     0.104ns WAD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.104ns) by 0.096ns

 Physical Path Details:

     Data path uart2/regs/transmitter/fifo_tx/SLICE_5567 to uart2/regs/transmitter/SLICE_1233:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R24C67A.CLK to     R24C67A.Q0 uart2/regs/transmitter/fifo_tx/SLICE_5567 (from uart_clk_c)
ROUTE         4     0.107     R24C67A.Q0 to     R25C67C.C0 uart2/regs/transmitter/fifo_tx/top[2]
ZERO_DEL    ---     0.000     R25C67C.C0 to  R25C67C.WADO2 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1231
ROUTE         2     0.000  R25C67C.WADO2 to   R25C67B.WAD2 uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WAD2_INT (to uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT)
                  --------
                    0.200   (46.5% logic, 53.5% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/fifo_tx/SLICE_5567:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R24C67A.CLK uart_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pll_uarts/PLLInst_0 to uart2/regs/transmitter/SLICE_1233:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R25C67C.CLK uart_clk_c
ZERO_DEL    ---     0.000    R25C67C.CLK to   R25C67C.WCKO uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1231
ROUTE         2     0.000   R25C67C.WCKO to    R25C67B.WCK uart2/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.103ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             uart5/regs/transmitter/fifo_tx/top[2]  (from uart_clk_c +)
   Destination:    FF         Data in       uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM0  (to uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT +)
                   FF                       uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM0

   Delay:               0.207ns  (44.9% logic, 55.1% route), 2 logic levels.

 Constraint Details:

     0.207ns physical path delay uart5/regs/transmitter/fifo_tx/SLICE_6107 to uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1196 meets
     0.104ns WAD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.104ns) by 0.103ns

 Physical Path Details:

     Data path uart5/regs/transmitter/fifo_tx/SLICE_6107 to uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1196:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R39C59C.CLK to     R39C59C.Q0 uart5/regs/transmitter/fifo_tx/SLICE_6107 (from uart_clk_c)
ROUTE         4     0.114     R39C59C.Q0 to     R39C60C.C0 uart5/regs/transmitter/fifo_tx/top[2]
ZERO_DEL    ---     0.000     R39C60C.C0 to  R39C60C.WADO2 uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1195
ROUTE         2     0.000  R39C60C.WADO2 to   R39C60A.WAD2 uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WAD2_INT (to uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT)
                  --------
                    0.207   (44.9% logic, 55.1% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pll_uarts/PLLInst_0 to uart5/regs/transmitter/fifo_tx/SLICE_6107:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R39C59C.CLK uart_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pll_uarts/PLLInst_0 to uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1196:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R39C60C.CLK uart_clk_c
ZERO_DEL    ---     0.000    R39C60C.CLK to   R39C60C.WCKO uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1195
ROUTE         2     0.000   R39C60C.WCKO to    R39C60A.WCK uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.103ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             uart5/regs/transmitter/fifo_tx/top[2]  (from uart_clk_c +)
   Destination:    FF         Data in       uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM1  (to uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT +)
                   FF                       uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM1

   Delay:               0.207ns  (44.9% logic, 55.1% route), 2 logic levels.

 Constraint Details:

      0.207ns physical path delay uart5/regs/transmitter/fifo_tx/SLICE_6107 to uart5/regs/transmitter/SLICE_1197 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.103ns

 Physical Path Details:

      Data path uart5/regs/transmitter/fifo_tx/SLICE_6107 to uart5/regs/transmitter/SLICE_1197:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R39C59C.CLK to     R39C59C.Q0 uart5/regs/transmitter/fifo_tx/SLICE_6107 (from uart_clk_c)
ROUTE         4     0.114     R39C59C.Q0 to     R39C60C.C0 uart5/regs/transmitter/fifo_tx/top[2]
ZERO_DEL    ---     0.000     R39C60C.C0 to  R39C60C.WADO2 uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1195
ROUTE         2     0.000  R39C60C.WADO2 to   R39C60B.WAD2 uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WAD2_INT (to uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT)
                  --------
                    0.207   (44.9% logic, 55.1% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_uarts/PLLInst_0 to uart5/regs/transmitter/fifo_tx/SLICE_6107:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R39C59C.CLK uart_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_uarts/PLLInst_0 to uart5/regs/transmitter/SLICE_1197:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R39C60C.CLK uart_clk_c
ZERO_DEL    ---     0.000    R39C60C.CLK to   R39C60C.WCKO uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1195
ROUTE         2     0.000   R39C60C.WCKO to    R39C60B.WCK uart5/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.126ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             uart1/regs/transmitter/fifo_tx/top[2]  (from uart_clk_c +)
   Destination:    FF         Data in       uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM0  (to uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT +)
                   FF                       uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM0

   Delay:               0.230ns  (40.4% logic, 59.6% route), 2 logic levels.

 Constraint Details:

      0.230ns physical path delay uart1/regs/transmitter/fifo_tx/SLICE_5388 to uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1244 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.126ns

 Physical Path Details:

      Data path uart1/regs/transmitter/fifo_tx/SLICE_5388 to uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1244:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R22C30B.CLK to     R22C30B.Q0 uart1/regs/transmitter/fifo_tx/SLICE_5388 (from uart_clk_c)
ROUTE         4     0.137     R22C30B.Q0 to     R21C30C.C0 uart1/regs/transmitter/fifo_tx/top[2]
ZERO_DEL    ---     0.000     R21C30C.C0 to  R21C30C.WADO2 uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1243
ROUTE         2     0.000  R21C30C.WADO2 to   R21C30A.WAD2 uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WAD2_INT (to uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT)
                  --------
                    0.230   (40.4% logic, 59.6% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_uarts/PLLInst_0 to uart1/regs/transmitter/fifo_tx/SLICE_5388:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R22C30B.CLK uart_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_uarts/PLLInst_0 to uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1244:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R21C30C.CLK uart_clk_c
ZERO_DEL    ---     0.000    R21C30C.CLK to   R21C30C.WCKO uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1243
ROUTE         2     0.000   R21C30C.WCKO to    R21C30A.WCK uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.126ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             uart1/regs/transmitter/fifo_tx/top[2]  (from uart_clk_c +)
   Destination:    FF         Data in       uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM1  (to uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT +)
                   FF                       uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/RAM1

   Delay:               0.230ns  (40.4% logic, 59.6% route), 2 logic levels.

 Constraint Details:

      0.230ns physical path delay uart1/regs/transmitter/fifo_tx/SLICE_5388 to uart1/regs/transmitter/SLICE_1245 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.126ns

 Physical Path Details:

      Data path uart1/regs/transmitter/fifo_tx/SLICE_5388 to uart1/regs/transmitter/SLICE_1245:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R22C30B.CLK to     R22C30B.Q0 uart1/regs/transmitter/fifo_tx/SLICE_5388 (from uart_clk_c)
ROUTE         4     0.137     R22C30B.Q0 to     R21C30C.C0 uart1/regs/transmitter/fifo_tx/top[2]
ZERO_DEL    ---     0.000     R21C30C.C0 to  R21C30C.WADO2 uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1243
ROUTE         2     0.000  R21C30C.WADO2 to   R21C30B.WAD2 uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WAD2_INT (to uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT)
                  --------
                    0.230   (40.4% logic, 59.6% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_uarts/PLLInst_0 to uart1/regs/transmitter/fifo_tx/SLICE_5388:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R22C30B.CLK uart_clk_c
                  --------
                    0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_uarts/PLLInst_0 to uart1/regs/transmitter/SLICE_1245:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R21C30C.CLK uart_clk_c
ZERO_DEL    ---     0.000    R21C30C.CLK to   R21C30C.WCKO uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/SLICE_1243
ROUTE         2     0.000   R21C30C.WCKO to    R21C30B.WCK uart1/regs/transmitter/fifo_tx/tfifo/ram_ram_0/WCK_INT
                  --------
                    0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.126ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             uart6/regs/transmitter/fifo_tx/top[2]  (from uart_clk_c +)
   Destination:    FF         Data in       uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/RAM1  (to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT +)
                   FF                       uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/RAM1

   Delay:               0.230ns  (40.4% logic, 59.6% route), 2 logic levels.

 Constraint Details:

      0.230ns physical path delay uart6/regs/transmitter/fifo_tx/SLICE_6288 to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1188 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.126ns

 Physical Path Details:

      Data path uart6/regs/transmitter/fifo_tx/SLICE_6288 to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1188:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R33C41B.CLK to     R33C41B.Q0 uart6/regs/transmitter/fifo_tx/SLICE_6288 (from uart_clk_c)
ROUTE         4     0.137     R33C41B.Q0 to     R34C41C.C0 uart6/regs/transmitter/fifo_tx/top[2]
ZERO_DEL    ---     0.000     R34C41C.C0 to  R34C41C.WADO2 uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1186
ROUTE         2     0.000  R34C41C.WADO2 to   R34C41B.WAD2 uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/WAD2_INT (to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT)
                  --------
                    0.230   (40.4% logic, 59.6% route), 2 logic levels.

```
 Clock Skew Details:

      Source Clock Path pll_uarts/PLLInst_0 to uart6/regs/transmitter/fifo_tx/SLICE_6288:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R33C41B.CLK uart_clk_c
                    --------
                      0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_uarts/PLLInst_0 to uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1188:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R34C41C.CLK uart_clk_c
ZERO_DEL    ---     0.000    R34C41C.CLK to   R34C41C.WCKO uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1186
ROUTE         2     0.000   R34C41C.WCKO to    R34C41B.WCK uart6/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT
                    --------
                      0.488   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.126ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              uart4/regs/transmitter/fifo_tx/top[2]  (from uart_clk_c +)
   Destination:    FF         Data in        uart4/regs/transmitter/fifo_tx/tfifo/ram_ram/RAM1  (to uart4/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT +)
                   FF                        uart4/regs/transmitter/fifo_tx/tfifo/ram_ram/RAM1

   Delay:               0.230ns  (40.4% logic, 59.6% route), 2 logic levels.

 Constraint Details:

      0.230ns physical path delay uart4/regs/transmitter/fifo_tx/SLICE_5925 to uart4/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1212 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.126ns

 Physical Path Details:

      Data path uart4/regs/transmitter/fifo_tx/SLICE_5925 to uart4/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1212:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R22C68A.CLK to     R22C68A.Q0 uart4/regs/transmitter/fifo_tx/SLICE_5925 (from uart_clk_c)
ROUTE         4     0.137     R22C68A.Q0 to     R21C68C.C0 uart4/regs/transmitter/fifo_tx/top[2]
ZERO_DEL    ---     0.000     R21C68C.C0 to  R21C68C.WADO2 uart4/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1210
ROUTE         2     0.000  R21C68C.WADO2 to   R21C68B.WAD2 uart4/regs/transmitter/fifo_tx/tfifo/ram_ram/WAD2_INT (to uart4/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT)
                    --------
                      0.230   (40.4% logic, 59.6% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pll_uarts/PLLInst_0 to uart4/regs/transmitter/fifo_tx/SLICE_5925:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R22C68A.CLK uart_clk_c
                    --------
                      0.488   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pll_uarts/PLLInst_0 to uart4/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1212:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.488 *L_R53C5.CLKOP to    R21C68C.CLK uart_clk_c
ZERO_DEL    ---     0.000    R21C68C.CLK to   R21C68C.WCKO uart4/regs/transmitter/fifo_tx/tfifo/ram_ram/SLICE_1210
ROUTE         2     0.000   R21C68C.WCKO to    R21C68B.WCK uart4/regs/transmitter/fifo_tx/tfifo/ram_ram/WCK_INT
                    --------
                      0.488   (0.0% logic, 100.0% route), 1 logic levels.


================================================================================
Preference: FREQUENCY NET "pcie/pclk" 250.000000 MHz ;
            987 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.136ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/data_out[6]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/RAM1

   Delay:               0.198ns  (47.0% logic, 53.0% route), 2 logic levels.

 Constraint Details:

      0.198ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/SLICE_1377 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.136ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/SLICE_1377:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R39C15C.CLK to     R39C15C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302 (from pcie/pclk)
ROUTE         2     0.105     R39C15C.Q0 to     R39C14C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/rxrc_data[6]
ZERO_DEL    ---     0.000     R39C14C.C1 to   R39C14C.WDO2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/SLICE_1375
ROUTE         1     0.000   R39C14C.WDO2 to    R39C14B.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/WD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/WCK_INT)
                    --------
                      0.198   (47.0% logic, 53.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R39C15C.CLK pcie/pclk
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/SLICE_1377:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R39C14C.CLK pcie/pclk
ZERO_DEL    ---     0.000    R39C14C.CLK to   R39C14C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/SLICE_1375
ROUTE         2     0.000   R39C14C.WCKO to    R39C14B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/WCK_INT
                    --------
                      0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.147ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_pcs_pipe/pipe_top_0/TxData_chx_s[2]  (from pcie/pclk +)
   Destination:    PCSD       Port           pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0(ASIC)  (to pcie/pclk +)

   Delay:               0.493ns  (18.9% logic, 81.1% route), 1 logic levels.

 Constraint Details:

      0.493ns physical path delay pcie/u1_pcs_pipe/pipe_top_0/SLICE_4202 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 meets
      0.287ns FFTXD_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.346ns) by 0.147ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pipe_top_0/SLICE_4202 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R61C35C.CLK to     R61C35C.Q0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_4202 (from pcie/pclk)
ROUTE         1     0.400     R61C35C.Q0 to *A.FF_TX_D_0_2 pcie/u1_pcs_pipe/TxData_0_out[2] (to pcie/pclk)
                    --------
                      0.493   (18.9% logic, 81.1% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4202:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R61C35C.CLK pcie/pclk
                    --------
                      0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.586 *FF_TX_F_CLK_0 to *.FF_TXI_CLK_0 pcie/pclk
                    --------
                      0.586   (0.0% logic, 100.0% route), 0 logic levels.
```

Passed: The following path meets requirements by 0.155ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_pcs_pipe/pipe_top_0/TxDataK_chx_s  (from pcie/pclk +)
   Destination:    PCSD       Port           pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0(ASIC)  (to pcie/pclk +)

   Delay:               0.501ns  (18.6% logic, 81.4% route), 1 logic levels.

 Constraint Details:

      0.501ns physical path delay pcie/u1_pcs_pipe/pipe_top_0/SLICE_4200 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 meets
      0.287ns FFTXD_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.346ns) by 0.155ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pipe_top_0/SLICE_4200 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R57C38C.CLK to     R57C38C.Q0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_4200 (from pcie/pclk)
ROUTE         1     0.408     R57C38C.Q0 to *A.FF_TX_D_0_8 pcie/u1_pcs_pipe/TxDataK_0_out (to pcie/pclk)
                  --------
                    0.501   (18.6% logic, 81.4% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4200:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R57C38C.CLK pcie/pclk
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.586 *FF_TX_F_CLK_0 to *.FF_TXI_CLK_0 pcie/pclk
                  --------
                    0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.167ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/data_out[6]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/WCK_INT +)
                  FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/RAM1

   Delay:               0.229ns  (40.6% logic, 59.4% route), 2 logic levels.

 Constraint Details:

      0.229ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1366 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.167ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1366:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R39C15C.CLK to     R39C15C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302 (from pcie/pclk)
ROUTE         2     0.136     R39C15C.Q0 to     R39C17C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/rxrc_data[6]
ZERO_DEL    ---     0.000     R39C17C.C1 to   R39C17C.WDO2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1364
ROUTE         1     0.000   R39C17C.WDO2 to    R39C17B.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/WD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/WCK_INT)
                  --------
                    0.229   (40.6% logic, 59.4% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R39C15C.CLK pcie/pclk
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1366:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R39C17C.CLK pcie/pclk
ZERO_DEL    ---     0.000    R39C17C.CLK to   R39C17C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1364
ROUTE         2     0.000   R39C17C.WCKO to    R39C17B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.173ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/data_out[7]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/WCK_INT +)
                  FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/RAM1

   Delay:               0.235ns  (39.6% logic, 60.4% route), 2 logic levels.

 Constraint Details:

      0.235ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/SLICE_1377 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.173ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/SLICE_1377:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R39C15C.CLK to     R39C15C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302 (from pcie/pclk)
ROUTE         2     0.142     R39C15C.Q1 to     R39C14C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/rxrc_data[7]
ZERO_DEL    ---     0.000     R39C14C.D1 to   R39C14C.WDO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/SLICE_1375
ROUTE         1     0.000   R39C14C.WDO3 to    R39C14B.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/WD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/WCK_INT)
                  --------
                    0.235   (39.6% logic, 60.4% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R39C15C.CLK pcie/pclk
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/SLICE_1377:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R39C14C.CLK pcie/pclk
ZERO_DEL    ---     0.000    R39C14C.CLK to   R39C14C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/SLICE_1375
ROUTE         2     0.000   R39C14C.WCKO to    R39C14B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram_0/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.173ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/data_out[7]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/WCK_INT +)
                  FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/RAM1

   Delay:               0.235ns  (39.6% logic, 60.4% route), 2 logic levels.

 Constraint Details:

      0.235ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1366 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.173ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1366:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R39C15C.CLK to     R39C15C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302 (from pcie/pclk)
ROUTE         2     0.142     R39C15C.Q1 to     R39C17C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/rxrc_data[7]

ZERO_DEL    ---     0.000     R39C17C.D1 to    R39C17C.WDO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1364
ROUTE         1     0.000   R39C17C.WDO3 to    R39C17B.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/WD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/WCK_INT)
                  --------
                    0.235   (39.6% logic, 60.4% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3302:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R39C15C.CLK pcie/pclk
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1366:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R39C17C.CLK pcie/pclk
ZERO_DEL    ---     0.000    R39C17C.CLK to   R39C17C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1364
ROUTE         2     0.000   R39C17C.WCKO to    R39C17B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.180ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/data_out[3]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/RAM1

   Delay:               0.242ns  (38.4% logic, 61.6% route), 2 logic levels.

 Constraint Details:

      0.242ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3300 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1380 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.180ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3300 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1380:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R39C16A.CLK to     R39C16A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3300 (from pcie/pclk)
ROUTE         2     0.149     R39C16A.Q1 to     R39C18C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/rxrc_data[3]
ZERO_DEL    ---     0.000     R39C18C.D1 to   R39C18C.WDO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1378
ROUTE         1     0.000   R39C18C.WDO3 to    R39C18B.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/WD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/WCK_INT)
                  --------
                    0.242   (38.4% logic, 61.6% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3300:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R39C16A.CLK pcie/pclk
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1380:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R39C18C.CLK pcie/pclk
ZERO_DEL    ---     0.000    R39C18C.CLK to   R39C18C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/SLICE_1378
ROUTE         2     0.000   R39C18C.WCKO to    R39C18B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1_ram/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.188ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_pcs_pipe/pipe_top_0/TxData_chx_s[0]  (from pcie/pclk +)
   Destination:    PCSD       Port           pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0(ASIC)  (to pcie/pclk +)

   Delay:               0.534ns  (17.4% logic, 82.6% route), 1 logic levels.

 Constraint Details:

      0.534ns physical path delay pcie/u1_pcs_pipe/pipe_top_0/SLICE_4201 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 meets
      0.287ns FFTXD_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.346ns) by 0.188ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pipe_top_0/SLICE_4201 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R58C38B.CLK to     R58C38B.Q0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_4201 (from pcie/pclk)
ROUTE         1     0.441     R58C38B.Q0 to *A.FF_TX_D_0_0 pcie/u1_pcs_pipe/TxData_0_out[0] (to pcie/pclk)
                  --------
                    0.534   (17.4% logic, 82.6% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4201:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R58C38B.CLK pcie/pclk
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.586 *FF_TX_F_CLK_0 to *.FF_TXI_CLK_0 pcie/pclk
                  --------
                    0.586   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.189ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/data_out[4]  (from pcie/pclk +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/RAM0

   Delay:               0.251ns  (37.1% logic, 62.9% route), 2 logic levels.

 Constraint Details:

      0.251ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3301 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1365 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.189ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3301 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1365:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R39C16C.CLK to     R39C16C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3301 (from pcie/pclk)
ROUTE         2     0.158     R39C16C.Q0 to     R39C17C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/rxrc_data[4]
ZERO_DEL    ---     0.000     R39C17C.A1 to   R39C17C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1364
ROUTE         1     0.000   R39C17C.WDO0 to    R39C17A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/WCK_INT)
                  --------
                    0.251   (37.1% logic, 62.9% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_descram/SLICE_3301:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R39C16C.CLK pcie/pclk
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1365:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R39C17C.CLK pcie/pclk
ZERO_DEL    ---     0.000    R39C17C.CLK to   R39C17C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/SLICE_1364
ROUTE         2     0.000   R39C17C.WCKO to    R39C17A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0_ram_0/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.201ns

```
 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_pcs_pipe/pipe_top_0/TxData_chx_s[1]  (from pcie/pclk +)
   Destination:    PCSD       Port           pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0(ASIC)  (to pcie/pclk +)

   Delay:               0.547ns  (17.0% logic, 83.0% route), 1 logic levels.

 Constraint Details:

      0.547ns physical path delay pcie/u1_pcs_pipe/pipe_top_0/SLICE_4201 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 meets
      0.287ns FFTXD_HLD and
      0.000ns delay constraint less
     -0.059ns skew requirement (totaling 0.346ns) by 0.201ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pipe_top_0/SLICE_4201 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R58C38B.CLK to     R58C38B.Q1 pcie/u1_pcs_pipe/pipe_top_0/SLICE_4201 (from pcie/pclk)
ROUTE         1     0.454     R58C38B.Q1 to *A.FF_TX_D_0_1 pcie/u1_pcs_pipe/TxData_0_out[1] (to pcie/pclk)
                  --------
                    0.547   (17.0% logic, 83.0% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4201:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.527 *FF_TX_F_CLK_0 to    R58C38B.CLK pcie/pclk
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       192     0.586 *FF_TX_F_CLK_0 to *.FF_TXI_CLK_0 pcie/pclk
                  --------
                    0.586   (0.0% logic, 100.0% route), 0 logic levels.


================================================================================
Preference: FREQUENCY NET "pcie/u1_pcs_pipe/ff_rx_fclk_0" 250.000000 MHz ;
            1 item scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.227ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_pcs_pipe/pipe_top_0/sync1_RxPolarity  (from pcie/u1_pcs_pipe/ff_rx_fclk_0 +)
   Destination:    FF         Data in        pcie/u1_pcs_pipe/pipe_top_0/sync2_RxPolarity  (to pcie/u1_pcs_pipe/ff_rx_fclk_0 +)

   Delay:               0.179ns  (52.0% logic, 48.0% route), 1 logic levels.

 Constraint Details:

      0.179ns physical path delay pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268 meets
     -0.048ns M_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.048ns) by 0.227ns

 Physical Path Details:

      Data path pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R59C34B.CLK to     R59C34B.Q0 pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268 (from pcie/u1_pcs_pipe/ff_rx_fclk_0)
ROUTE         1     0.086     R59C34B.Q0 to     R59C34B.M1 pcie/u1_pcs_pipe/pipe_top_0/sync1_RxPolarity (to pcie/u1_pcs_pipe/ff_rx_fclk_0)
                  --------
                    0.179   (52.0% logic, 48.0% route), 1 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE         1     1.216 *FF_RX_F_CLK_0 to    R59C34B.CLK pcie/u1_pcs_pipe/ff_rx_fclk_0
                  --------
                    1.216   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_pcs_pipe/pipe_top_0/SLICE_4268:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE         1     1.216 *FF_RX_F_CLK_0 to    R59C34B.CLK pcie/u1_pcs_pipe/ff_rx_fclk_0
                  --------
                    1.216   (0.0% logic, 100.0% route), 0 logic levels.


================================================================================
Preference: BLOCK PATH FROM PORT "rstn" ;
            119 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: BLOCK PATH TO PORT "OUT*" ;
            0 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: BLOCK PATH FROM PORT "INP*" ;
            16 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: BLOCK PATH FROM PORT "SRAM_A*" ;
            0 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: BLOCK PATH TO PORT "LED*" ;
            8 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: BLOCK PATH FROM CELL "*ctc_reset_chx*" ;
            14 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


================================================================================
Preference: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*cnt_done_nfts_rx*" 2.000000 X ;
            214 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 1.035ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.024ns  (43.5% logic, 56.5% route), 10 logic levels.

 Constraint Details:

      1.024ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.035ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R18C6B.CLK to      R18C6B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 (from clk_125_c)
ROUTE         9     0.292      R18C6B.Q1 to      R16C5C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]
C0TOFCO_DE  ---     0.094      R16C5C.A0 to     R16C5C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024
ROUTE         1     0.000     R16C5C.FCO to     R16C6A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.022     R16C6A.FCI to     R16C6A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000     R16C6A.FCO to     R16C6B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.022     R16C6B.FCI to     R16C6B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000     R16C6B.FCO to     R16C6C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022     R16C6C.FCI to     R16C6C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000     R16C6C.FCO to     R16C7A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
```

```
FCITOFCO_D  ---     0.022     R16C7A.FCI to     R16C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000     R16C7A.FCO to     R16C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022     R16C7B.FCI to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070     R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.287      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.024   (43.5% logic, 56.5% route), 10 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R18C6B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.048ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[8]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.037ns  (44.9% logic, 55.1% route), 11 logic levels.

 Constraint Details:

      1.037ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_976 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.048ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_976 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R19C7B.CLK to      R19C7B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_976 (from clk_125_c)
ROUTE         3     0.284      R19C7B.Q0 to      R16C5B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[8]
C1TOFCO_DE  ---     0.093      R16C5B.B1 to     R16C5B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1023
ROUTE         1     0.000     R16C5B.FCO to     R16C5C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
FCITOFCO_D  ---     0.022     R16C5C.FCI to     R16C5C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024
ROUTE         1     0.000     R16C5C.FCO to     R16C6A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.022     R16C6A.FCI to     R16C6A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000     R16C6A.FCO to     R16C6B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.022     R16C6B.FCI to     R16C6B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000     R16C6B.FCO to     R16C6C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022     R16C6C.FCI to     R16C6C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000     R16C6C.FCO to     R16C7A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022     R16C7A.FCI to     R16C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000     R16C7A.FCO to     R16C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022     R16C7B.FCI to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070     R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.287      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.037   (44.9% logic, 55.1% route), 11 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_976:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C7B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.130ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[4]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.119ns  (45.6% logic, 54.4% route), 13 logic levels.

 Constraint Details:

      1.119ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.130ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R19C6C.CLK to      R19C6C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 (from clk_125_c)
ROUTE         9     0.322      R19C6C.Q0 to      R16C4C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[4]
C1TOFCO_DE  ---     0.093      R16C4C.A1 to     R16C4C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1021
ROUTE         1     0.000     R16C4C.FCO to     R16C5A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[4]
FCITOFCO_D  ---     0.022     R16C5A.FCI to     R16C5A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1022
ROUTE         1     0.000     R16C5A.FCO to     R16C5B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[6]
FCITOFCO_D  ---     0.022     R16C5B.FCI to     R16C5B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1023
ROUTE         1     0.000     R16C5B.FCO to     R16C5C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
FCITOFCO_D  ---     0.022     R16C5C.FCI to     R16C5C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024
ROUTE         1     0.000     R16C5C.FCO to     R16C6A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.022     R16C6A.FCI to     R16C6A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000     R16C6A.FCO to     R16C6B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.022     R16C6B.FCI to     R16C6B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000     R16C6B.FCO to     R16C6C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022     R16C6C.FCI to     R16C6C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000     R16C6C.FCO to     R16C7A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022     R16C7A.FCI to     R16C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000     R16C7A.FCO to     R16C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022     R16C7B.FCI to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070     R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.287      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.119   (45.6% logic, 54.4% route), 13 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C6C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.130ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)
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```
   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.119ns  (39.9% logic, 60.1% route), 7 logic levels.

 Constraint Details:

     1.119ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2985 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 1.130ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2985 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R18C6C.CLK to      R18C6C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2985 (from clk_125_c)
ROUTE         1     0.075      R18C6C.Q1 to      R18C7C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]
CTOF_DEL    ---     0.056      R18C7C.D1 to      R18C7C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8079
ROUTE        24     0.201      R18C7C.F1 to      R16C7D.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL    ---     0.056      R16C7D.C1 to      R16C7D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8340
ROUTE         1     0.110      R16C7D.F1 to      R16C7B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_df24
C1TOFCO_DE  ---     0.093      R16C7B.A1 to      R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022      R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000      R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070      R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.287       R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.119   (39.9% logic, 60.1% route), 7 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2985:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R18C6C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.135ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[5]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.124ns  (43.5% logic, 56.5% route), 12 logic levels.

 Constraint Details:

     1.124ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 1.135ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R19C6C.CLK to      R19C6C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974 (from clk_125_c)
ROUTE         8     0.348      R19C6C.Q1 to      R16C5A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[5]
C0TOFCO_DE  ---     0.094      R16C5A.A0 to     R16C5A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1022
ROUTE         1     0.000     R16C5A.FCO to     R16C5B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[6]
FCITOFCO_D  ---     0.022      R16C5B.FCI to     R16C5B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1023
ROUTE         1     0.000     R16C5B.FCO to     R16C5C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
FCITOFCO_D  ---     0.022      R16C5C.FCI to     R16C5C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024
ROUTE         1     0.000     R16C5C.FCO to     R16C6A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.022      R16C6A.FCI to     R16C6A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000     R16C6A.FCO to     R16C6B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.022      R16C6B.FCI to     R16C6B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000     R16C6B.FCO to     R16C6C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022      R16C6C.FCI to     R16C6C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000     R16C6C.FCO to     R16C7A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022      R16C7A.FCI to     R16C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000     R16C7A.FCO to     R16C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022      R16C7B.FCI to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022      R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000      R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070      R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.287       R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.124   (43.5% logic, 56.5% route), 12 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_974:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C6C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.142ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.131ns  (37.6% logic, 62.4% route), 6 logic levels.

 Constraint Details:

     1.131ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2985 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 1.142ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2985 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R18C6C.CLK to      R18C6C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2985 (from clk_125_c)
ROUTE         1     0.075      R18C6C.Q1 to      R18C7C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[5]
CTOF_DEL    ---     0.056      R18C7C.D1 to      R18C7C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8079
ROUTE        24     0.118      R18C7C.F1 to      R18C7D.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_5
CTOF_DEL    ---     0.056      R18C7D.A1 to      R18C7D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8339
ROUTE         1     0.226      R18C7D.F1 to      R16C7C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_df26
C0TOFCO_DE  ---     0.094      R16C7C.A0 to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070      R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.287       R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.131   (37.6% logic, 62.4% route), 6 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2985:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R18C6C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
```

```
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.147ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[8]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.136ns  (40.1% logic, 59.9% route), 9 logic levels.

 Constraint Details:

      1.136ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8078 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.147ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8078 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R18C7A.CLK to      R18C7A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8078 (from clk_125_c)
ROUTE         2     0.126      R18C7A.Q0 to      R18C7A.C1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[8]
CTOF_DEL    ---     0.056      R18C7A.C1 to      R18C7A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8078
ROUTE        22     0.267      R18C7A.F1 to      R16C6B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_1_0
C1TOFCO_DE  ---     0.093      R16C6B.B1 to     R16C6B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000     R16C6B.FCO to     R16C6C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022     R16C6C.FCI to     R16C6C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000     R16C6C.FCO to     R16C7A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022     R16C7A.FCI to     R16C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000     R16C7A.FCO to     R16C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022     R16C7B.FCI to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070      R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.287      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.136   (40.1% logic, 59.9% route), 9 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8078:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R18C7A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.148ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[8]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.137ns  (40.2% logic, 59.8% route), 9 logic levels.

 Constraint Details:

      1.137ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8078 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.148ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8078 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R18C7A.CLK to      R18C7A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8078 (from clk_125_c)
ROUTE         2     0.126      R18C7A.Q0 to      R18C7A.C1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt_fast[8]
CTOF_DEL    ---     0.056      R18C7A.C1 to      R18C7A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8078
ROUTE        22     0.267      R18C7A.F1 to      R16C6B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un7_cnt_done_nfts_rx_1_c8_a0_1_0
C0TOFCO_DE  ---     0.094      R16C6B.B0 to     R16C6B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000     R16C6B.FCO to     R16C6C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022     R16C6C.FCI to     R16C6C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000     R16C6C.FCO to     R16C7A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022     R16C7A.FCI to     R16C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000     R16C7A.FCO to     R16C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022     R16C7B.FCI to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070      R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.287      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.137   (40.2% logic, 59.8% route), 9 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_8078:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R18C7A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.152ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[7]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.141ns  (40.9% logic, 59.1% route), 11 logic levels.

 Constraint Details:

      1.141ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.152ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R19C7A.CLK to      R19C7A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 (from clk_125_c)
ROUTE         5     0.387      R19C7A.Q1 to      R16C5B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[7]
C0TOFCO_DE  ---     0.094      R16C5B.B0 to     R16C5B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1023
ROUTE         1     0.000     R16C5B.FCO to     R16C5C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
FCITOFCO_D  ---     0.022     R16C5C.FCI to     R16C5C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024
ROUTE         1     0.000     R16C5C.FCO to     R16C6A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.022     R16C6A.FCI to     R16C6A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000     R16C6A.FCO to     R16C6B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.022     R16C6B.FCI to     R16C6B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000     R16C6B.FCO to     R16C6C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022     R16C6C.FCI to     R16C6C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000     R16C6C.FCO to     R16C7A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022     R16C7A.FCI to     R16C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000     R16C7A.FCO to     R16C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022     R16C7B.FCI to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070      R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.287      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
```

```
CTOF_DEL    ---     0.056      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.141   (40.9% logic, 59.1% route), 11 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C7A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.152ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[3]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx  (to clk_125_c +)

   Delay:               1.141ns  (44.8% logic, 55.2% route), 13 logic levels.

 Constraint Details:

      1.141ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.152ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R18C6B.CLK to      R18C6B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 (from clk_125_c)
ROUTE        10     0.343      R18C6B.Q0 to      R16C4C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[3]
C0TOFCO_DE  ---     0.094      R16C4C.B0 to     R16C4C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1021
ROUTE         1     0.000     R16C4C.FCO to     R16C5A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[4]
FCITOFCO_D  ---     0.022     R16C5A.FCI to     R16C5A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1022
ROUTE         1     0.000     R16C5A.FCO to     R16C5B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[6]
FCITOFCO_D  ---     0.022     R16C5B.FCI to     R16C5B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1023
ROUTE         1     0.000     R16C5B.FCO to     R16C5C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[8]
FCITOFCO_D  ---     0.022     R16C5C.FCI to     R16C5C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1024
ROUTE         1     0.000     R16C5C.FCO to     R16C6A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[10]
FCITOFCO_D  ---     0.022     R16C6A.FCI to     R16C6A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1025
ROUTE         1     0.000     R16C6A.FCO to     R16C6B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[12]
FCITOFCO_D  ---     0.022     R16C6B.FCI to     R16C6B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1026
ROUTE         1     0.000     R16C6B.FCO to     R16C6C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[14]
FCITOFCO_D  ---     0.022     R16C6C.FCI to     R16C6C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1027
ROUTE         1     0.000     R16C6C.FCO to     R16C7A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[16]
FCITOFCO_D  ---     0.022     R16C7A.FCI to     R16C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1028
ROUTE         1     0.000     R16C7A.FCO to     R16C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[20]
FCITOFCO_D  ---     0.022     R16C7B.FCI to     R16C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1029
ROUTE         1     0.000     R16C7B.FCO to     R16C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[24]
FCITOFCO_D  ---     0.022     R16C7C.FCI to     R16C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1030
ROUTE         1     0.000     R16C7C.FCO to     R16C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry[28]
FCITOF1_DE  ---     0.070     R16C8A.FCI to      R16C8A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1031
ROUTE         1     0.287      R16C8A.F1 to      R19C9A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un10_cnt_done_nfts_rx_cry_i[30]
CTOF_DEL    ---     0.056      R19C9A.C0 to      R19C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874
ROUTE         1     0.000      R19C9A.F0 to     R19C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/cnt_done_nfts_rx_5_i_i (to clk_125_c)
                  --------
                    1.141   (44.8% logic, 55.2% route), 13 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R18C6B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2874:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


================================================================================
Preference: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*ltssm_nfts_rx_skp*" 2.000000 X ;
            244 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 1.108ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[8]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               1.097ns  (40.5% logic, 59.5% route), 11 logic levels.

 Constraint Details:

      1.097ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_976 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.108ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_976 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R19C7B.CLK to      R19C7B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_976 (from clk_125_c)
ROUTE         3     0.322      R19C7B.Q0 to      R15C7B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[8]
C0TOFCO_DE  ---     0.094      R15C7B.B0 to     R15C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_997
ROUTE         1     0.000     R15C7B.FCO to     R15C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[9]
FCITOFCO_D  ---     0.022     R15C7C.FCI to     R15C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_998
ROUTE         1     0.000     R15C7C.FCO to     R15C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11]
FCITOFCO_D  ---     0.022     R15C8A.FCI to     R15C8A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_999
ROUTE         1     0.000     R15C8A.FCO to     R15C8B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D  ---     0.022     R15C8B.FCI to     R15C8B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1000
ROUTE         1     0.000     R15C8B.FCO to     R15C8C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D  ---     0.022     R15C8C.FCI to     R15C8C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001
ROUTE         1     0.000     R15C8C.FCO to     R15C9A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D  ---     0.022     R15C9A.FCI to     R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to     R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.022     R15C9B.FCI to     R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to     R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.022     R15C9C.FCI to     R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.047    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     0.331     R15C10A.F0 to      R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.056      R21C9A.A0 to      R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    1.097   (40.5% logic, 59.5% route), 11 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_976:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C7B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R21C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.112ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)
```

```
   Delay:               1.101ns  (34.2% logic, 65.8% route), 8 logic levels.

 Constraint Details:

      1.101ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.112ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R18C6B.CLK to      R18C6B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 (from clk_125_c)
ROUTE         9     0.393      R18C6B.Q1 to      R15C8B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]
C1TOFCO_DE  ---     0.093      R15C8B.B1 to     R15C8B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1000
ROUTE         1     0.000     R15C8B.FCO to     R15C8C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D  ---     0.022     R15C8C.FCI to     R15C8C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001
ROUTE         1     0.000     R15C8C.FCO to     R15C9A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D  ---     0.022     R15C9A.FCI to     R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to     R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.022     R15C9B.FCI to     R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to     R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.022     R15C9C.FCI to     R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.047    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     0.331     R15C10A.F0 to      R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.056      R21C9A.A0 to      R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    1.101   (34.2% logic, 65.8% route), 8 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R18C6B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R21C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.113ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               1.102ns  (34.3% logic, 65.7% route), 8 logic levels.

 Constraint Details:

      1.102ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.113ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R18C6B.CLK to      R18C6B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 (from clk_125_c)
ROUTE         9     0.393      R18C6B.Q1 to      R15C8B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]
C0TOFCO_DE  ---     0.094      R15C8B.B0 to     R15C8B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1000
ROUTE         1     0.000     R15C8B.FCO to     R15C8C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D  ---     0.022     R15C8C.FCI to     R15C8C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001
ROUTE         1     0.000     R15C8C.FCO to     R15C9A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D  ---     0.022     R15C9A.FCI to     R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to     R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.022     R15C9B.FCI to     R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to     R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.022     R15C9C.FCI to     R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.047    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     0.331     R15C10A.F0 to      R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.056      R21C9A.A0 to      R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    1.102   (34.3% logic, 65.7% route), 8 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R18C6B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R21C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.126ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[6]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               1.115ns  (41.8% logic, 58.2% route), 12 logic levels.

 Constraint Details:

      1.115ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.126ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R19C7A.CLK to      R19C7A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975 (from clk_125_c)
ROUTE         6     0.318      R19C7A.Q0 to      R15C7A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[6]
C0TOFCO_DE  ---     0.094      R15C7A.A0 to     R15C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_996
ROUTE         1     0.000     R15C7A.FCO to     R15C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[7]
FCITOFCO_D  ---     0.022     R15C7B.FCI to     R15C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_997
ROUTE         1     0.000     R15C7B.FCO to     R15C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[9]
FCITOFCO_D  ---     0.022     R15C7C.FCI to     R15C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_998
ROUTE         1     0.000     R15C7C.FCO to     R15C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11]
FCITOFCO_D  ---     0.022     R15C8A.FCI to     R15C8A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_999
ROUTE         1     0.000     R15C8A.FCO to     R15C8B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D  ---     0.022     R15C8B.FCI to     R15C8B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1000
ROUTE         1     0.000     R15C8B.FCO to     R15C8C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D  ---     0.022     R15C8C.FCI to     R15C8C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001
ROUTE         1     0.000     R15C8C.FCO to     R15C9A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D  ---     0.022     R15C9A.FCI to     R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to     R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.022     R15C9B.FCI to     R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to     R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.022     R15C9C.FCI to     R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.047    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     0.331     R15C10A.F0 to      R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.056      R21C9A.A0 to      R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    1.115   (41.8% logic, 58.2% route), 12 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_975:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R19C7A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.
```

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 0.527 *FF_TX_H_CLK_0 to | R21C9A.CLK | clk_125_c |
| | | 0.527 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 1.134ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

Delay: 1.123ns (35.5% logic, 64.5% route), 9 logic levels.

Constraint Details:

1.123ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
-0.011ns DIN_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.011ns) by 1.134ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.093 R18C6B.CLK to | R18C6B.Q1 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 (from clk_125_c) |
| ROUTE | 9 | 0.393 R18C6B.Q1 to | R15C8A.B1 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9] |
| C1TOFCO_DE | --- | 0.093 R15C8A.B1 to | R15C8A.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_999 |
| ROUTE | 1 | 0.000 R15C8A.FCO to | R15C8B.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13] |
| FCITOFCO_D | --- | 0.022 R15C8B.FCI to | R15C8B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1000 |
| ROUTE | 1 | 0.000 R15C8B.FCO to | R15C8C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15] |
| FCITOFCO_D | --- | 0.022 R15C8C.FCI to | R15C8C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001 |
| ROUTE | 1 | 0.000 R15C8C.FCO to | R15C9A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18] |
| FCITOFCO_D | --- | 0.022 R15C9A.FCI to | R15C9A.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002 |
| ROUTE | 1 | 0.000 R15C9A.FCO to | R15C9B.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22] |
| FCITOFCO_D | --- | 0.022 R15C9B.FCI to | R15C9B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003 |
| ROUTE | 1 | 0.000 R15C9B.FCO to | R15C9C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26] |
| FCITOFCO_D | --- | 0.022 R15C9C.FCI to | R15C9C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004 |
| ROUTE | 1 | 0.000 R15C9C.FCO to | R15C10A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30] |
| FCITOF0_DE | --- | 0.047 R15C10A.FCI to | R15C10A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005 |
| ROUTE | 1 | 0.331 R15C10A.F0 to | R21C9A.A0 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30] |
| CTOF_DEL | --- | 0.056 R21C9A.A0 to | R21C9A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 |
| ROUTE | 1 | 0.000 R21C9A.F0 to | R21C9A.DI0 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c) |
| | | 1.123 (35.5% logic, 64.5% route), 9 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 0.527 *FF_TX_H_CLK_0 to | R18C6B.CLK | clk_125_c |
| | | 0.527 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 0.527 *FF_TX_H_CLK_0 to | R21C9A.CLK | clk_125_c |
| | | 0.527 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 1.134ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[3] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

Delay: 1.123ns (45.3% logic, 54.7% route), 14 logic levels.

Constraint Details:

1.123ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
-0.011ns DIN_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.011ns) by 1.134ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.093 R18C6B.CLK to | R18C6B.Q0 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 (from clk_125_c) |
| ROUTE | 10 | 0.283 R18C6B.Q0 to | R15C6B.B1 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[3] |
| C1TOFCO_DE | --- | 0.093 R15C6B.B1 to | R15C6B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_994 |
| ROUTE | 1 | 0.000 R15C6B.FCO to | R15C6C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[3] |
| FCITOFCO_D | --- | 0.022 R15C6C.FCI to | R15C6C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_995 |
| ROUTE | 1 | 0.000 R15C6C.FCO to | R15C7A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[5] |
| FCITOFCO_D | --- | 0.022 R15C7A.FCI to | R15C7A.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_996 |
| ROUTE | 1 | 0.000 R15C7A.FCO to | R15C7B.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[7] |
| FCITOFCO_D | --- | 0.022 R15C7B.FCI to | R15C7B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_997 |
| ROUTE | 1 | 0.000 R15C7B.FCO to | R15C7C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[9] |
| FCITOFCO_D | --- | 0.022 R15C7C.FCI to | R15C7C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_998 |
| ROUTE | 1 | 0.000 R15C7C.FCO to | R15C8A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11] |
| FCITOFCO_D | --- | 0.022 R15C8A.FCI to | R15C8A.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_999 |
| ROUTE | 1 | 0.000 R15C8A.FCO to | R15C8B.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13] |
| FCITOFCO_D | --- | 0.022 R15C8B.FCI to | R15C8B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1000 |
| ROUTE | 1 | 0.000 R15C8B.FCO to | R15C8C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15] |
| FCITOFCO_D | --- | 0.022 R15C8C.FCI to | R15C8C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001 |
| ROUTE | 1 | 0.000 R15C8C.FCO to | R15C9A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18] |
| FCITOFCO_D | --- | 0.022 R15C9A.FCI to | R15C9A.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002 |
| ROUTE | 1 | 0.000 R15C9A.FCO to | R15C9B.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22] |
| FCITOFCO_D | --- | 0.022 R15C9B.FCI to | R15C9B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003 |
| ROUTE | 1 | 0.000 R15C9B.FCO to | R15C9C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26] |
| FCITOFCO_D | --- | 0.022 R15C9C.FCI to | R15C9C.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004 |
| ROUTE | 1 | 0.000 R15C9C.FCO to | R15C10A.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30] |
| FCITOF0_DE | --- | 0.047 R15C10A.FCI to | R15C10A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005 |
| ROUTE | 1 | 0.331 R15C10A.F0 to | R21C9A.A0 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30] |
| CTOF_DEL | --- | 0.056 R21C9A.A0 to | R21C9A.F0 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 |
| ROUTE | 1 | 0.000 R21C9A.F0 to | R21C9A.DI0 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c) |
| | | 1.123 (45.3% logic, 54.7% route), 14 logic levels. | | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 0.527 *FF_TX_H_CLK_0 to | R18C6B.CLK | clk_125_c |
| | | 0.527 (0.0% logic, 100.0% route), 0 logic levels. | | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 0.527 *FF_TX_H_CLK_0 to | R21C9A.CLK | clk_125_c |
| | | 0.527 (0.0% logic, 100.0% route), 0 logic levels. | | |

Passed: The following path meets requirements by 1.135ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp (to clk_125_c +)

Delay: 1.124ns (35.6% logic, 64.4% route), 9 logic levels.

Constraint Details:

1.124ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
-0.011ns DIN_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.011ns) by 1.135ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.093 R18C6B.CLK to | R18C6B.Q1 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 (from clk_125_c) |
| ROUTE | 9 | 0.393 R18C6B.Q1 to | R15C8A.B0 | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9] |
| C0TOFCO_DE | --- | 0.094 R15C8A.B0 to | R15C8A.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_999 |
| ROUTE | 1 | 0.000 R15C8A.FCO to | R15C8B.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13] |
| FCITOFCO_D | --- | 0.022 R15C8B.FCI to | R15C8B.FCO | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1000 |
| ROUTE | 1 | 0.000 R15C8B.FCO to | R15C8C.FCI | pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15] |

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FCITOFCO_D  ---     0.022     R15C8C.FCI to     R15C8C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001
ROUTE         1     0.000     R15C8C.FCO to     R15C9A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D  ---     0.022     R15C9A.FCI to     R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to     R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.022     R15C9B.FCI to     R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to     R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.022     R15C9C.FCI to     R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.047    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     0.331     R15C10A.F0 to       R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.056      R21C9A.A0 to       R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    1.124   (35.6% logic, 64.4% route), 9 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R18C6B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R21C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.139ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[2]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               1.128ns  (45.2% logic, 54.8% route), 14 logic levels.

 Constraint Details:

      1.128ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.139ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R20C6C.CLK to      R20C6C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983 (from clk_125_c)
ROUTE        16     0.287      R20C6C.Q1 to      R15C6B.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[2]
C0TOFCO_DE  ---     0.094      R15C6B.A0 to     R15C6B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_994
ROUTE         1     0.000     R15C6B.FCO to     R15C6C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[3]
FCITOFCO_D  ---     0.022     R15C6C.FCI to     R15C6C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_995
ROUTE         1     0.000     R15C6C.FCO to     R15C7A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[5]
FCITOFCO_D  ---     0.022     R15C7A.FCI to     R15C7A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_996
ROUTE         1     0.000     R15C7A.FCO to     R15C7B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[7]
FCITOFCO_D  ---     0.022     R15C7B.FCI to     R15C7B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_997
ROUTE         1     0.000     R15C7B.FCO to     R15C7C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[9]
FCITOFCO_D  ---     0.022     R15C7C.FCI to     R15C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_998
ROUTE         1     0.000     R15C7C.FCO to     R15C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11]
FCITOFCO_D  ---     0.022     R15C8A.FCI to     R15C8A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_999
ROUTE         1     0.000     R15C8A.FCO to     R15C8B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D  ---     0.022     R15C8B.FCI to     R15C8B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1000
ROUTE         1     0.000     R15C8B.FCO to     R15C8C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D  ---     0.022     R15C8C.FCI to     R15C8C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001
ROUTE         1     0.000     R15C8C.FCO to     R15C9A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D  ---     0.022     R15C9A.FCI to     R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to     R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.022     R15C9B.FCI to     R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to     R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.022     R15C9C.FCI to     R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.047    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     0.331     R15C10A.F0 to       R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.056      R21C9A.A0 to       R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    1.128   (45.2% logic, 54.8% route), 14 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2983:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R20C6C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R21C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.144ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               1.133ns  (37.2% logic, 62.8% route), 10 logic levels.

 Constraint Details:

      1.133ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 1.144ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R18C6B.CLK to      R18C6B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 (from clk_125_c)
ROUTE         9     0.381      R18C6B.Q1 to      R15C7C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]
C1TOFCO_DE  ---     0.093      R15C7C.B1 to     R15C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_998
ROUTE         1     0.000     R15C7C.FCO to     R15C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11]
FCITOFCO_D  ---     0.022     R15C8A.FCI to     R15C8A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_999
ROUTE         1     0.000     R15C8A.FCO to     R15C8B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D  ---     0.022     R15C8B.FCI to     R15C8B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1000
ROUTE         1     0.000     R15C8B.FCO to     R15C8C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D  ---     0.022     R15C8C.FCI to     R15C8C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001
ROUTE         1     0.000     R15C8C.FCO to     R15C9A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D  ---     0.022     R15C9A.FCI to     R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to     R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.022     R15C9B.FCI to     R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to     R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.022     R15C9C.FCI to     R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.047    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     0.331     R15C10A.F0 to       R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.056      R21C9A.A0 to       R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    1.133   (37.2% logic, 62.8% route), 10 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R18C6B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R21C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 1.145ns
```

```
 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp  (to clk_125_c +)

   Delay:               1.134ns  (37.2% logic, 62.8% route), 10 logic levels.

 Constraint Details:

     1.134ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 1.145ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R18C6B.CLK to      R18C6B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984 (from clk_125_c)
ROUTE         9     0.381      R18C6B.Q1 to      R15C7C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/nfts_rx_skp_cnt[9]
C0TOFCO_DE  ---     0.094      R15C7C.B0 to      R15C7C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_998
ROUTE         1     0.000     R15C7C.FCO to      R15C8A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[11]
FCITOFCO_D  ---     0.022      R15C8A.FCI to      R15C8A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_999
ROUTE         1     0.000     R15C8A.FCO to      R15C8B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[13]
FCITOFCO_D  ---     0.022      R15C8B.FCI to      R15C8B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1000
ROUTE         1     0.000     R15C8B.FCO to      R15C8C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[15]
FCITOFCO_D  ---     0.022      R15C8C.FCI to      R15C8C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1001
ROUTE         1     0.000     R15C8C.FCO to      R15C9A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[18]
FCITOFCO_D  ---     0.022      R15C9A.FCI to      R15C9A.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1002
ROUTE         1     0.000     R15C9A.FCO to      R15C9B.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[22]
FCITOFCO_D  ---     0.022      R15C9B.FCI to      R15C9B.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1003
ROUTE         1     0.000     R15C9B.FCO to      R15C9C.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[26]
FCITOFCO_D  ---     0.022      R15C9C.FCI to      R15C9C.FCO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1004
ROUTE         1     0.000     R15C9C.FCO to    R15C10A.FCI pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry_cry[30]
FCITOF0_DE  ---     0.047    R15C10A.FCI to     R15C10A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_1005
ROUTE         1     0.331     R15C10A.F0 to      R21C9A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/un22_ltssm_nfts_rx_skp_cry[30]
CTOF_DEL    ---     0.056      R21C9A.A0 to      R21C9A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967
ROUTE         1     0.000      R21C9A.F0 to     R21C9A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/ltssm_nfts_rx_skp_RNO (to clk_125_c)
                  --------
                    1.134   (37.2% logic, 62.8% route), 10 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2984:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R18C6B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/SLICE_2967:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R21C9A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr*" 6.000000 ns ;
            33 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.143ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT +)

   Delay:               0.247ns  (37.7% logic, 62.3% route), 2 logic levels.

 Constraint Details:

     0.247ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1383 meets
     0.104ns WAD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.104ns) by 0.143ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1383:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R42C4A.CLK to      R42C4A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        12     0.154      R42C4A.Q0 to      R43C4C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL    ---     0.000      R43C4C.A0 to   R43C4C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1381
ROUTE         2     0.000   R43C4C.WADO0 to    R43C4B.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT)
                  --------
                    0.247   (37.7% logic, 62.3% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1383:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R43C4C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C4C.CLK to    R43C4C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1381
ROUTE         2     0.000    R43C4C.WCKO to     R43C4B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.143ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM0

   Delay:               0.247ns  (37.7% logic, 62.3% route), 2 logic levels.

 Constraint Details:

     0.247ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1382 meets
     0.104ns WAD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.104ns) by 0.143ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1382:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R42C4A.CLK to      R42C4A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        12     0.154      R42C4A.Q0 to      R43C4C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL    ---     0.000      R43C4C.A0 to   R43C4C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1381
ROUTE         2     0.000   R43C4C.WADO0 to    R43C4A.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT)
                  --------
                    0.247   (37.7% logic, 62.3% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1382:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R43C4C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C4C.CLK to    R43C4C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1381
ROUTE         2     0.000    R43C4C.WCKO to     R43C4A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.203ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)
```

```
   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (to clk_125_c +)

   Delay:               0.192ns  (77.6% logic, 22.4% route), 2 logic levels.

 Constraint Details:

      0.192ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.203ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R42C4A.CLK to      R42C4A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        12     0.043      R42C4A.Q0 to      R42C4A.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
CTOF_DEL    ---     0.056      R42C4A.D0 to      R42C4A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364
ROUTE         1     0.000      R42C4A.F0 to     R42C4A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr_3[0] (to clk_125_c)
                  --------
                    0.192   (77.6% logic, 22.4% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.206ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/RAM0

   Delay:               0.310ns  (30.0% logic, 70.0% route), 2 logic levels.

 Constraint Details:

      0.310ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1391 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.206ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1391:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R42C4A.CLK to      R42C4A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        12     0.217      R42C4A.Q0 to      R43C3C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL    ---     0.000      R43C3C.A0 to   R43C3C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1390
ROUTE         1     0.000   R43C3C.WADO0 to    R43C3A.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT)
                  --------
                    0.310   (30.0% logic, 70.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1391:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R43C3C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C3C.CLK to    R43C3C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1390
ROUTE         2     0.000    R43C3C.WCKO to     R43C3A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.243ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM0

   Delay:               0.347ns  (26.8% logic, 73.2% route), 2 logic levels.

 Constraint Details:

      0.347ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1385 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.243ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1385:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R42C4A.CLK to      R42C4A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        11     0.254      R42C4A.Q1 to      R43C6C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
ZERO_DEL    ---     0.000      R43C6C.B0 to   R43C6C.WADO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1384
ROUTE         2     0.000   R43C6C.WADO1 to    R43C6A.WAD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WAD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT)
                  --------
                    0.347   (26.8% logic, 73.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1385:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R43C6C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C6C.CLK to    R43C6C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1384
ROUTE         2     0.000    R43C6C.WCKO to     R43C6A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.243ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM1

   Delay:               0.347ns  (26.8% logic, 73.2% route), 2 logic levels.

 Constraint Details:

      0.347ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1386 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.243ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1386:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R42C4A.CLK to      R42C4A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        11     0.254      R42C4A.Q1 to      R43C6C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
ZERO_DEL    ---     0.000      R43C6C.B0 to   R43C6C.WADO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1384
ROUTE         2     0.000   R43C6C.WADO1 to    R43C6B.WAD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WAD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT)
                  --------
```

                    0.347   (26.8% logic, 73.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                    -------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1386:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R43C6C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C6C.CLK to    R43C6C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1384
ROUTE         2     0.000    R43C6C.WCKO to     R43C6B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT
                    -------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.261ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM0

   Delay:              0.365ns  (25.5% logic, 74.5% route), 2 logic levels.

 Constraint Details:

      0.365ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1382 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.261ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1382:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R42C4A.CLK to      R42C4A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        11     0.272      R42C4A.Q1 to      R43C4C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
ZERO_DEL    ---     0.000      R43C4C.B0 to   R43C4C.WADO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1381
ROUTE         2     0.000   R43C4C.WADO1 to    R43C4A.WAD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WAD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT)
                    -------
                    0.365   (25.5% logic, 74.5% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                    -------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1382:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R43C4C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C4C.CLK to    R43C4C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1381
ROUTE         2     0.000    R43C4C.WCKO to     R43C4A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT
                    -------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.261ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT +)

   Delay:              0.365ns  (25.5% logic, 74.5% route), 2 logic levels.

 Constraint Details:

      0.365ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1383 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.261ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1383:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R42C4A.CLK to      R42C4A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        11     0.272      R42C4A.Q1 to      R43C4C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
ZERO_DEL    ---     0.000      R43C4C.B0 to   R43C4C.WADO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1381
ROUTE         2     0.000   R43C4C.WADO1 to    R43C4B.WAD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WAD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT)
                    -------
                    0.365   (25.5% logic, 74.5% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                    -------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1383:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R43C4C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C4C.CLK to    R43C4C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1381
ROUTE         2     0.000    R43C4C.WCKO to     R43C4B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT
                    -------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.261ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/RAM0

   Delay:              0.365ns  (25.5% logic, 74.5% route), 2 logic levels.

 Constraint Details:

      0.365ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1391 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.261ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1391:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R42C4A.CLK to      R42C4A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        11     0.272      R42C4A.Q1 to      R43C3C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[1]
ZERO_DEL    ---     0.000      R43C3C.B0 to   R43C3C.WADO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1390
ROUTE         1     0.000   R43C3C.WADO1 to    R43C3A.WAD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WAD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT)
                    -------
                    0.365   (25.5% logic, 74.5% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                    -------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1391:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R43C3C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C3C.CLK to    R43C3C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1390
ROUTE         2     0.000    R43C3C.WCKO to     R43C3A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT
                    -------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.

Passed: The following path meets requirements by 0.265ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/RAM0

   Delay:               0.369ns  (25.2% logic, 74.8% route), 2 logic levels.

 Constraint Details:

      0.369ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1385 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.265ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1385:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R42C4A.CLK to      R42C4A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364 (from clk_125_c)
ROUTE        12     0.276      R42C4A.Q0 to      R43C6C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr[0]
ZERO_DEL    ---     0.000      R43C6C.A0 to   R43C6C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1384
ROUTE         2     0.000   R43C6C.WADO0 to    R43C6A.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT)
                  --------
                    0.369   (25.2% logic, 74.8% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/SLICE_3364:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R42C4A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1385:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R43C6C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C6C.CLK to    R43C6C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/SLICE_1384
ROUTE         2     0.000    R43C6C.WCKO to     R43C6A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_0/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.

Report:    0.192ns is the minimum delay for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr*" 6.000000 ns ;
            147 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.231ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (to clk_125_c +)

   Delay:               0.220ns  (67.7% logic, 32.3% route), 2 logic levels.

 Constraint Details:

      0.220ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.231ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R36C8C.CLK to      R36C8C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c)
ROUTE        30     0.071      R36C8C.Q0 to      R36C8C.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL    ---     0.056      R36C8C.C0 to      R36C8C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332
ROUTE         1     0.000      R36C8C.F0 to     R36C8C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr_3[0] (to clk_125_c)
                  --------
                    0.220   (67.7% logic, 32.3% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.272ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (to clk_125_c +)

   Delay:               0.261ns  (57.1% logic, 42.9% route), 2 logic levels.

 Constraint Details:

      0.261ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.272ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R36C8C.CLK to      R36C8C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c)
ROUTE        29     0.112      R36C8C.Q1 to      R36C8C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL    ---     0.056      R36C8C.A1 to      R36C8C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332
ROUTE         1     0.000      R36C8C.F1 to     R36C8C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr_3[1] (to clk_125_c)
                  --------
                    0.261   (57.1% logic, 42.9% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.313ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (to clk_125_c +)

   Delay:               0.302ns  (49.3% logic, 50.7% route), 2 logic levels.

 Constraint Details:

      0.302ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.313ns

 Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.093 | R36C8C.CLK to | R36C8C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c) |
| ROUTE | 30 | 0.153 | R36C8C.Q0 to | R36C8C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0] |
| CTOF_DEL | --- | 0.056 | R36C8C.B1 to | R36C8C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 |
| ROUTE | 1 | 0.000 | R36C8C.F1 to | R36C8C.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr_3[1] (to clk_125_c) |
| | | 0.302 | (49.3% logic, 50.7% route), 2 logic levels. | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 0.527 | *FF_TX_H_CLK_0 to | R36C8C.CLK clk_125_c |
| | | 0.527 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 0.527 | *FF_TX_H_CLK_0 to | R36C8C.CLK clk_125_c |
| | | 0.527 | (0.0% logic, 100.0% route), 0 logic levels. | |

Passed: The following path meets requirements by 0.599ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[10] (to clk_125_c +)

Delay: 0.588ns (34.9% logic, 65.1% route), 3 logic levels.

Constraint Details:

0.588ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817 meets
-0.011ns DIN_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.011ns) by 0.599ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.093 | R36C8C.CLK to | R36C8C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c) |
| ROUTE | 29 | 0.269 | R36C8C.Q1 to | R34C11C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1] |
| CTOF_DEL | --- | 0.056 | R34C11C.C1 to | R34C11C.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817 |
| ROUTE | 12 | 0.114 | R34C11C.F1 to | R34C11C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1ror_0 |
| CTOF_DEL | --- | 0.056 | R34C11C.A0 to | R34C11C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817 |
| ROUTE | 1 | 0.000 | R34C11C.F0 to | R34C11C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[10] (to clk_125_c) |
| | | 0.588 | (34.9% logic, 65.1% route), 3 logic levels. | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 0.527 | *FF_TX_H_CLK_0 to | R36C8C.CLK clk_125_c |
| | | 0.527 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 0.527 | *FF_TX_H_CLK_0 to | R34C11C.CLK clk_125_c |
| | | 0.527 | (0.0% logic, 100.0% route), 0 logic levels. | |

Passed: The following path meets requirements by 0.606ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[12] (to clk_125_c +)

Delay: 0.595ns (34.5% logic, 65.5% route), 3 logic levels.

Constraint Details:

0.595ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2786 meets
-0.011ns DIN_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.011ns) by 0.606ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2786:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.093 | R36C8C.CLK to | R36C8C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c) |
| ROUTE | 29 | 0.310 | R36C8C.Q1 to | R34C10B.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1] |
| CTOF_DEL | --- | 0.056 | R34C10B.D1 to | R34C10B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2816 |
| ROUTE | 12 | 0.080 | R34C10B.F1 to | R33C10B.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0ror_0 |
| CTOF_DEL | --- | 0.056 | R33C10B.D1 to | R33C10B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2786 |
| ROUTE | 1 | 0.000 | R33C10B.F1 to | R33C10B.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[12] (to clk_125_c) |
| | | 0.595 | (34.5% logic, 65.5% route), 3 logic levels. | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 0.527 | *FF_TX_H_CLK_0 to | R36C8C.CLK clk_125_c |
| | | 0.527 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2786:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 0.527 | *FF_TX_H_CLK_0 to | R33C10B.CLK clk_125_c |
| | | 0.527 | (0.0% logic, 100.0% route), 0 logic levels. | |

Passed: The following path meets requirements by 0.606ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1] (from clk_125_c +)
Destination: FF Data in pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[10] (to clk_125_c +)

Delay: 0.595ns (34.5% logic, 65.5% route), 3 logic levels.

Constraint Details:

0.595ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817 meets
-0.011ns DIN_HLD and
0.000ns delay constraint less
0.000ns skew requirement (totaling -0.011ns) by 0.606ns

Physical Path Details:

Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| REG_DEL | --- | 0.093 | R36C8C.CLK to | R36C8C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c) |
| ROUTE | 29 | 0.310 | R36C8C.Q1 to | R34C10D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1] |
| CTOF_DEL | --- | 0.056 | R34C10D.D0 to | R34C10D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_8603 |
| ROUTE | 12 | 0.080 | R34C10D.F0 to | R34C11C.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1ror_1 |
| CTOF_DEL | --- | 0.056 | R34C11C.D0 to | R34C11C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817 |
| ROUTE | 1 | 0.000 | R34C11C.F0 to | R34C11C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[10] (to clk_125_c) |
| | | 0.595 | (34.5% logic, 65.5% route), 3 logic levels. | |

Clock Skew Details:

Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 0.527 | *FF_TX_H_CLK_0 to | R36C8C.CLK clk_125_c |
| | | 0.527 | (0.0% logic, 100.0% route), 0 logic levels. | |

Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817:

| Name | Fanout | Delay (ns) | Site | Resource |
|---|---|---|---|---|
| ROUTE | 999 | 0.527 | *FF_TX_H_CLK_0 to | R34C11C.CLK clk_125_c |

                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.620ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[12]  (to clk_125_c +)

   Delay:               0.609ns  (33.7% logic, 66.3% route), 3 logic levels.

 Constraint Details:

      0.609ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2786 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.620ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2786:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R36C8C.CLK to      R36C8C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c)
ROUTE        30     0.324      R36C8C.Q0 to     R34C10B.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL    ---     0.056     R34C10B.A1 to     R34C10B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2816
ROUTE        12     0.080     R34C10B.F1 to     R33C10B.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0ror_0
CTOF_DEL    ---     0.056     R33C10B.D1 to     R33C10B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2786
ROUTE         1     0.000     R33C10B.F1 to    R33C10B.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[12] (to clk_125_c)
                  --------
                    0.609   (33.7% logic, 66.3% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2786:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R33C10B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.635ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data1[10]  (to clk_125_c +)

   Delay:               0.624ns  (32.9% logic, 67.1% route), 3 logic levels.

 Constraint Details:

      0.624ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.635ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R36C8C.CLK to      R36C8C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c)
ROUTE        30     0.339      R36C8C.Q0 to     R34C10D.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[0]
CTOF_DEL    ---     0.056     R34C10D.C0 to     R34C10D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_8603
ROUTE        12     0.080     R34C10D.F0 to     R34C11C.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1ror_1
CTOF_DEL    ---     0.056     R34C11C.D0 to     R34C11C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817
ROUTE         1     0.000     R34C11C.F0 to    R34C11C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_1[10] (to clk_125_c)
                  --------
                    0.624   (32.9% logic, 67.1% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2817:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R34C11C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.639ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[10]  (to clk_125_c +)

   Delay:               0.628ns  (32.6% logic, 67.4% route), 3 logic levels.

 Constraint Details:

      0.628ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2816 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.639ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2816:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R36C8C.CLK to      R36C8C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c)
ROUTE        29     0.310      R36C8C.Q1 to     R34C10D.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL    ---     0.056     R34C10D.D1 to     R34C10D.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_8603
ROUTE        12     0.113     R34C10D.F1 to     R34C10B.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0ror_1
CTOF_DEL    ---     0.056     R34C10B.A0 to     R34C10B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2816
ROUTE         1     0.000     R34C10B.F0 to    R34C10B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[10] (to clk_125_c)
                  --------
                    0.628   (32.6% logic, 67.4% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2816:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R34C10B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.640ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_data0[10]  (to clk_125_c +)

   Delay:               0.629ns  (32.6% logic, 67.4% route), 3 logic levels.

 Constraint Details:

      0.629ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2816 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.640ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2816:

```
   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R36C8C.CLK to      R36C8C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332 (from clk_125_c)
ROUTE        29     0.310      R36C8C.Q1 to     R34C10B.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr[1]
CTOF_DEL    ---     0.056     R34C10B.D1 to     R34C10B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2816
ROUTE        12     0.114     R34C10B.F1 to     R34C10B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0ror_0
CTOF_DEL    ---     0.056     R34C10B.B0 to     R34C10B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2816
ROUTE         1     0.000     R34C10B.F0 to    R34C10B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/rf_0[10] (to clk_125_c)
                  --------
                    0.629   (32.6% logic, 67.4% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_3332:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R36C8C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_rxrc/SLICE_2816:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R34C10B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Report:    0.220ns is the minimum delay for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr*" 6.000000 ns ;
            14 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.202ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]  (to clk_125_c +)

   Delay:               0.191ns  (78.0% logic, 22.0% route), 2 logic levels.

 Constraint Details:

      0.191ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.202ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R31C21A.CLK to     R31C21A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 (from clk_125_c)
ROUTE         5     0.042     R31C21A.Q0 to     R31C21A.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]
CTOF_DEL    ---     0.056     R31C21A.D0 to     R31C21A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231
ROUTE         1     0.000     R31C21A.F0 to    R31C21A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_e0 (to clk_125_c)
                  --------
                    0.191   (78.0% logic, 22.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.228ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]  (to clk_125_c +)

   Delay:               0.217ns  (68.7% logic, 31.3% route), 2 logic levels.

 Constraint Details:

      0.217ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.228ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R31C21C.CLK to     R31C21C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233 (from clk_125_c)
ROUTE         2     0.068     R31C21C.Q0 to     R31C21C.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]
CTOF_DEL    ---     0.056     R31C21C.C0 to     R31C21C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233
ROUTE         1     0.000     R31C21C.F0 to    R31C21C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n3 (to clk_125_c)
                  --------
                    0.217   (68.7% logic, 31.3% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.237ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_eidle_tx  (to clk_125_c +)

   Delay:               0.226ns  (65.9% logic, 34.1% route), 2 logic levels.

 Constraint Details:

      0.226ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.237ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R31C21C.CLK to     R31C21C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233 (from clk_125_c)
ROUTE         2     0.077     R31C21C.Q0 to     R30C21A.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]
CTOF_DEL    ---     0.056     R30C21A.D0 to     R30C21A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0
ROUTE         1     0.000     R30C21A.F0 to    R30C21A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/ltssm_eidle_tx (to clk_125_c)
                  --------
                    0.226   (65.9% logic, 34.1% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:
```

```
   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C21A.CLK clk_125_c
                    --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.238ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]  (to clk_125_c +)

   Delay:               0.227ns  (65.6% logic, 34.4% route), 2 logic levels.

 Constraint Details:

      0.227ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.238ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R31C21B.CLK to     R31C21B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 (from clk_125_c)
ROUTE         3     0.078     R31C21B.Q1 to     R31C21C.D0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]
CTOF_DEL    ---     0.056     R31C21C.D0 to     R31C21C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233
ROUTE         1     0.000     R31C21C.F0 to    R31C21C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n3 (to clk_125_c)
                    --------
                     0.227   (65.6% logic, 34.4% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21B.CLK clk_125_c
                    --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21C.CLK clk_125_c
                    --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.241ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]  (to clk_125_c +)

   Delay:               0.230ns  (64.8% logic, 35.2% route), 2 logic levels.

 Constraint Details:

      0.230ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.241ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R31C21A.CLK to     R31C21A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 (from clk_125_c)
ROUTE         5     0.081     R31C21A.Q0 to     R31C21B.D0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]
CTOF_DEL    ---     0.056     R31C21B.D0 to     R31C21B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232
ROUTE         1     0.000     R31C21B.F0 to    R31C21B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n1 (to clk_125_c)
                    --------
                     0.230   (64.8% logic, 35.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21A.CLK clk_125_c
                    --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21B.CLK clk_125_c
                    --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.241ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]  (to clk_125_c +)

   Delay:               0.230ns  (64.8% logic, 35.2% route), 2 logic levels.

 Constraint Details:

      0.230ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.241ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R31C21A.CLK to     R31C21A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 (from clk_125_c)
ROUTE         5     0.081     R31C21A.Q0 to     R31C21B.D1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]
CTOF_DEL    ---     0.056     R31C21B.D1 to     R31C21B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232
ROUTE         1     0.000     R31C21B.F1 to    R31C21B.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n2 (to clk_125_c)
                    --------
                     0.230   (64.8% logic, 35.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21A.CLK clk_125_c
                    --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21B.CLK clk_125_c
                    --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.267ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]  (to clk_125_c +)

   Delay:               0.256ns  (58.2% logic, 41.8% route), 2 logic levels.

 Constraint Details:

      0.256ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.267ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R31C21B.CLK to     R31C21B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 (from clk_125_c)
```

```
ROUTE         4     0.107     R31C21B.Q0 to     R31C21B.C0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]
CTOF_DEL    ---     0.056     R31C21B.C0 to     R31C21B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232
ROUTE         1     0.000     R31C21B.F0 to    R31C21B.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n1 (to clk_125_c)
                  --------
                    0.256   (58.2% logic, 41.8% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.274ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]  (to clk_125_c +)

   Delay:               0.263ns  (56.7% logic, 43.3% route), 2 logic levels.

 Constraint Details:

      0.263ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.274ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R31C21B.CLK to     R31C21B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 (from clk_125_c)
ROUTE         3     0.114     R31C21B.Q1 to     R31C21B.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[2]
CTOF_DEL    ---     0.056     R31C21B.B1 to     R31C21B.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232
ROUTE         1     0.000     R31C21B.F1 to    R31C21B.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n2 (to clk_125_c)
                  --------
                    0.263   (56.7% logic, 43.3% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.311ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]  (to clk_125_c +)

   Delay:               0.300ns  (49.7% logic, 50.3% route), 2 logic levels.

 Constraint Details:

      0.300ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.311ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R31C21A.CLK to     R31C21A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231 (from clk_125_c)
ROUTE         5     0.151     R31C21A.Q0 to     R31C21C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[0]
CTOF_DEL    ---     0.056     R31C21C.A0 to     R31C21C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233
ROUTE         1     0.000     R31C21C.F0 to    R31C21C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n3 (to clk_125_c)
                  --------
                    0.300   (49.7% logic, 50.3% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3231:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.312ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[3]  (to clk_125_c +)

   Delay:               0.301ns  (49.5% logic, 50.5% route), 2 logic levels.

 Constraint Details:

      0.301ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.312ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R31C21B.CLK to     R31C21B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232 (from clk_125_c)
ROUTE         4     0.152     R31C21B.Q0 to     R31C21C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr[1]
CTOF_DEL    ---     0.056     R31C21C.B0 to     R31C21C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233
ROUTE         1     0.000     R31C21C.F0 to    R31C21C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr_n3 (to clk_125_c)
                  --------
                    0.301   (49.5% logic, 50.5% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3232:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21B.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3233:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R31C21C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Report:    0.191ns is the minimum delay for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr*" 6.000000 ns ;
            18 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------
```

Passed: The following path meets requirements by 0.076ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT +)

   Delay:               0.180ns  (51.7% logic, 48.3% route), 2 logic levels.

 Constraint Details:

      0.180ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.076ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R30C22A.CLK to     R30C22A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 (from clk_125_c)
ROUTE         3     0.087     R30C22A.Q1 to     R30C21C.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]
ZERO_DEL    ---     0.000     R30C21C.D0 to  R30C21C.WADO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         1     0.000  R30C21C.WADO3 to   R30C21A.WAD3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WAD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT)
                  --------
                    0.180   (51.7% logic, 48.3% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C21C.CLK clk_125_c
ZERO_DEL    ---     0.000    R30C21C.CLK to   R30C21C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         2     0.000   R30C21C.WCKO to    R30C21A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.141ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT +)

   Delay:               0.245ns  (38.0% logic, 62.0% route), 2 logic levels.

 Constraint Details:

      0.245ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.141ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R30C22C.CLK to     R30C22C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 (from clk_125_c)
ROUTE         6     0.152     R30C22C.Q0 to     R30C21C.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]
ZERO_DEL    ---     0.000     R30C21C.A0 to  R30C21C.WADO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         1     0.000  R30C21C.WADO0 to   R30C21A.WAD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WAD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT)
                  --------
                    0.245   (38.0% logic, 62.0% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C21C.CLK clk_125_c
ZERO_DEL    ---     0.000    R30C21C.CLK to   R30C21C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         2     0.000   R30C21C.WCKO to    R30C21A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.179ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT +)

   Delay:               0.283ns  (32.9% logic, 67.1% route), 2 logic levels.

 Constraint Details:

      0.283ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.179ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R30C22A.CLK to     R30C22A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 (from clk_125_c)
ROUTE         4     0.190     R30C22A.Q0 to     R30C21C.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]
ZERO_DEL    ---     0.000     R30C21C.C0 to  R30C21C.WADO2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         1     0.000  R30C21C.WADO2 to   R30C21A.WAD2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WAD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT)
                  --------
                    0.283   (32.9% logic, 67.1% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C21C.CLK clk_125_c
ZERO_DEL    ---     0.000    R30C21C.CLK to   R30C21C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         2     0.000   R30C21C.WCKO to    R30C21A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.208ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT +)

   Delay:               0.312ns  (29.8% logic, 70.2% route), 2 logic levels.

 Constraint Details:

      0.312ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0 meets
      0.104ns WAD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.104ns) by 0.208ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource

```
REG_DEL     ---     0.093    R30C22C.CLK to     R30C22C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 (from clk_125_c)
ROUTE         5     0.219     R30C22C.Q1 to     R30C21C.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]
ZERO_DEL    ---     0.000     R30C21C.B0 to  R30C21C.WADO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         1     0.000  R30C21C.WADO1 to   R30C21A.WAD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WAD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT)
                  --------
                    0.312   (29.8% logic, 70.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0.0:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C21C.CLK clk_125_c
ZERO_DEL    ---     0.000    R30C21C.CLK to   R30C21C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0
ROUTE         2     0.000   R30C21C.WCKO to    R30C21A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/u1_pmi_distributed_dpram/mem_0_0/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.229ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]  (to clk_125_c +)

   Delay:               0.218ns  (68.3% logic, 31.7% route), 2 logic levels.

 Constraint Details:

      0.218ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.229ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R30C22C.CLK to     R30C22C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 (from clk_125_c)
ROUTE         6     0.069     R30C22C.Q0 to     R30C22C.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]
CTOF_DEL    ---     0.056     R30C22C.C0 to     R30C22C.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258
ROUTE         1     0.000     R30C22C.F0 to    R30C22C.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_i[0] (to clk_125_c)
                  --------
                    0.218   (68.3% logic, 31.7% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.241ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]  (to clk_125_c +)

   Delay:               0.230ns  (64.8% logic, 35.2% route), 2 logic levels.

 Constraint Details:

      0.230ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.241ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R30C22C.CLK to     R30C22C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 (from clk_125_c)
ROUTE         5     0.081     R30C22C.Q1 to     R30C22A.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]
CTOF_DEL    ---     0.056     R30C22A.D0 to     R30C22A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259
ROUTE         1     0.000     R30C22A.F0 to    R30C22A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[2] (to clk_125_c)
                  --------
                    0.230   (64.8% logic, 35.2% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.259ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]  (to clk_125_c +)

   Delay:               0.248ns  (60.1% logic, 39.9% route), 2 logic levels.

 Constraint Details:

      0.248ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 meets
     -0.011ns DIN_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling -0.011ns) by 0.259ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R30C22A.CLK to     R30C22A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 (from clk_125_c)
ROUTE         3     0.099     R30C22A.Q1 to     R30C22A.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]
CTOF_DEL    ---     0.056     R30C22A.D1 to     R30C22A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259
ROUTE         1     0.000     R30C22A.F1 to    R30C22A.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[3] (to clk_125_c)
                  --------
                    0.248   (60.1% logic, 39.9% route), 2 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.269ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)
```

```
   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[2]  (to clk_125_c +)

   Delay:               0.258ns  (57.8% logic, 42.2% route), 2 logic levels.

 Constraint Details:

     0.258ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 0.269ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R30C22C.CLK to     R30C22C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 (from clk_125_c)
ROUTE         6     0.109     R30C22C.Q0 to     R30C22A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]
CTOF_DEL    ---     0.056     R30C22A.C0 to     R30C22A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259
ROUTE         1     0.000     R30C22A.F0 to    R30C22A.DI0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[2] (to clk_125_c)
                  --------
                    0.258   (57.8% logic, 42.2% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.269ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]  (to clk_125_c +)

   Delay:               0.258ns  (57.8% logic, 42.2% route), 2 logic levels.

 Constraint Details:

     0.258ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 0.269ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R30C22C.CLK to     R30C22C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 (from clk_125_c)
ROUTE         6     0.109     R30C22C.Q0 to     R30C22A.C1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[0]
CTOF_DEL    ---     0.056     R30C22A.C1 to     R30C22A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259
ROUTE         1     0.000     R30C22A.F1 to    R30C22A.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[3] (to clk_125_c)
                  --------
                    0.258   (57.8% logic, 42.2% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.


Passed: The following path meets requirements by 0.311ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[3]  (to clk_125_c +)

   Delay:               0.300ns  (49.7% logic, 50.3% route), 2 logic levels.

 Constraint Details:

     0.300ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259 meets
    -0.011ns DIN_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling -0.011ns) by 0.311ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093    R30C22C.CLK to     R30C22C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258 (from clk_125_c)
ROUTE         5     0.151     R30C22C.Q1 to     R30C22A.B1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr[1]
CTOF_DEL    ---     0.056     R30C22A.B1 to     R30C22A.F1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259
ROUTE         1     0.000     R30C22A.F1 to    R30C22A.DI1 pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr_RNO[3] (to clk_125_c)
                  --------
                    0.300   (49.7% logic, 50.3% route), 2 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3258:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_ltssm/u1_osenc/SLICE_3259:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to    R30C22A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

Report:    0.180ns is the minimum delay for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data*" 6.000000 ns ;
            16 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.327ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[8]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0

   Delay:               0.389ns  (38.3% logic, 61.7% route), 3 logic levels.

 Constraint Details:

     0.389ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2793 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1388 meets
     0.062ns WD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.062ns) by 0.327ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2793 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1388:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R49C7C.CLK to      R49C7C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2793 (from clk_125_c)
ROUTE         1     0.084      R49C7C.Q0 to      R49C6D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[8]
```

CTOF_DEL    ---     0.056      R49C6D.D0 to      R49C6D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9720
ROUTE         1     0.156      R49C6D.F0 to      R48C6C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[8]
ZERO_DEL    ---     0.000      R48C6C.A1 to    R48C6C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1387
ROUTE         1     0.000    R48C6C.WDO0 to     R48C6A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT)
                  --------
                    0.389   (38.3% logic, 61.7% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2793:

   Name    Fanout   Delay (ns)          Site              Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R49C7C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1388:

   Name    Fanout   Delay (ns)          Site              Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R48C6C.CLK clk_125_c
ZERO_DEL    ---     0.000     R48C6C.CLK to    R48C6C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1387
ROUTE         2     0.000    R48C6C.WCKO to     R48C6A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.359ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[11]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM1

   Delay:               0.421ns  (35.4% logic, 64.6% route), 3 logic levels.

 Constraint Details:

      0.421ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2794 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1389 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.359ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2794 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1389:

   Name    Fanout   Delay (ns)          Site              Resource
REG_DEL     ---     0.093     R50C6C.CLK to      R50C6C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2794 (from clk_125_c)
ROUTE         1     0.112      R50C6C.Q1 to      R49C6A.C0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[11]
CTOF_DEL    ---     0.056      R49C6A.C0 to      R49C6A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9723
ROUTE         1     0.160      R49C6A.F0 to      R48C6C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[11]
ZERO_DEL    ---     0.000      R48C6C.D1 to    R48C6C.WDO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1387
ROUTE         1     0.000    R48C6C.WDO3 to     R48C6B.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT)
                  --------
                    0.421   (35.4% logic, 64.6% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2794:

   Name    Fanout   Delay (ns)          Site              Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R50C6C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1389:

   Name    Fanout   Delay (ns)          Site              Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R48C6C.CLK clk_125_c
ZERO_DEL    ---     0.000     R48C6C.CLK to    R48C6C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1387
ROUTE         2     0.000    R48C6C.WCKO to     R48C6B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.366ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[10]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM1

   Delay:               0.428ns  (34.8% logic, 65.2% route), 3 logic levels.

 Constraint Details:

      0.428ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2794 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1389 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.366ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2794 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1389:

   Name    Fanout   Delay (ns)          Site              Resource
REG_DEL     ---     0.093     R50C6C.CLK to      R50C6C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2794 (from clk_125_c)
ROUTE         1     0.213      R50C6C.Q0 to      R48C6D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[10]
CTOF_DEL    ---     0.056      R48C6D.B0 to      R48C6D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9722
ROUTE         1     0.066      R48C6D.F0 to      R48C6C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[10]
ZERO_DEL    ---     0.000      R48C6C.C1 to    R48C6C.WDO2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1387
ROUTE         1     0.000    R48C6C.WDO2 to     R48C6B.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT)
                  --------
                    0.428   (34.8% logic, 65.2% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2794:

   Name    Fanout   Delay (ns)          Site              Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R50C6C.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1389:

   Name    Fanout   Delay (ns)          Site              Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R48C6C.CLK clk_125_c
ZERO_DEL    ---     0.000     R48C6C.CLK to    R48C6C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1387
ROUTE         2     0.000    R48C6C.WCKO to     R48C6B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.384ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[1]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0

   Delay:               0.446ns  (33.4% logic, 66.6% route), 3 logic levels.

 Constraint Details:

      0.446ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2789 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1396 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.384ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2789 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1396:

   Name    Fanout   Delay (ns)          Site              Resource
REG_DEL     ---     0.093     R48C7C.CLK to      R48C7C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2789 (from clk_125_c)
ROUTE         1     0.149      R48C7C.Q1 to      R48C5D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[1]
CTOF_DEL    ---     0.056      R48C5D.D0 to      R48C5D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9713
ROUTE         1     0.148      R48C5D.F0 to      R48C5C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[1]
ZERO_DEL    ---     0.000      R48C5C.B1 to    R48C5C.WDO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1395
ROUTE         1     0.000    R48C5C.WDO1 to     R48C5A.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
                  --------
                    0.446   (33.4% logic, 66.6% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2789:

   Name    Fanout   Delay (ns)          Site              Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R48C7C.CLK clk_125_c
                  --------

```
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1396:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R48C5C.CLK clk_125_c
ZERO_DEL    ---     0.000     R48C5C.CLK to    R48C5C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1395
ROUTE         2     0.000    R48C5C.WCKO to     R48C5A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
                   --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.428ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM0

   Delay:               0.490ns  (30.4% logic, 69.6% route), 3 logic levels.

 Constraint Details:

     0.490ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2789 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1396 meets
     0.062ns WD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.062ns) by 0.428ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2789 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1396:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R48C7C.CLK to      R48C7C.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2789 (from clk_125_c)
ROUTE         1     0.075      R48C7C.Q0 to      R48C7D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[0]
CTOF_DEL    ---     0.056      R48C7D.D0 to      R48C7D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9712
ROUTE         1     0.266      R48C7D.F0 to      R48C5C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[0]
ZERO_DEL    ---     0.000      R48C5C.A1 to    R48C5C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1395
ROUTE         1     0.000    R48C5C.WDO0 to     R48C5A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
                   --------
                    0.490   (30.4% logic, 69.6% route), 3 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2789:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R48C7C.CLK clk_125_c
                   --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1396:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R48C5C.CLK clk_125_c
ZERO_DEL    ---     0.000     R48C5C.CLK to    R48C5C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1395
ROUTE         2     0.000    R48C5C.WCKO to     R48C5A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
                   --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.440ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[5]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM0

   Delay:               0.502ns  (29.7% logic, 70.3% route), 3 logic levels.

 Constraint Details:

     0.502ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2791 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1393 meets
     0.062ns WD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.062ns) by 0.440ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2791 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1393:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R50C6A.CLK to      R50C6A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2791 (from clk_125_c)
ROUTE         1     0.075      R50C6A.Q1 to      R50C7D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[5]
CTOF_DEL    ---     0.056      R50C7D.D0 to      R50C7D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9717
ROUTE         1     0.278      R50C7D.F0 to      R43C7C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[5]
ZERO_DEL    ---     0.000      R43C7C.B1 to    R43C7C.WDO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1392
ROUTE         1     0.000    R43C7C.WDO1 to     R43C7A.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT)
                   --------
                    0.502   (29.7% logic, 70.3% route), 3 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2791:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R50C6A.CLK clk_125_c
                   --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1393:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R43C7C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C7C.CLK to    R43C7C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1392
ROUTE         2     0.000    R43C7C.WCKO to     R43C7A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT
                   --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.451ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[4]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM0

   Delay:               0.513ns  (29.0% logic, 71.0% route), 3 logic levels.

 Constraint Details:

     0.513ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2791 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1393 meets
     0.062ns WD_HLD and
     0.000ns delay constraint less
     0.000ns skew requirement (totaling 0.062ns) by 0.451ns

 Physical Path Details:

     Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2791 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1393:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R50C6A.CLK to      R50C6A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2791 (from clk_125_c)
ROUTE         1     0.217      R50C6A.Q0 to      R43C7D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[4]
CTOF_DEL    ---     0.056      R43C7D.D0 to      R43C7D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9716
ROUTE         1     0.147      R43C7D.F0 to      R43C7C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[4]
ZERO_DEL    ---     0.000      R43C7C.A1 to    R43C7C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1392
ROUTE         1     0.000    R43C7C.WDO0 to     R43C7A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT)
                   --------
                    0.513   (29.0% logic, 71.0% route), 3 logic levels.

 Clock Skew Details:

     Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2791:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R50C6A.CLK clk_125_c
                   --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

     Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1393:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R43C7C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C7C.CLK to    R43C7C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1392
ROUTE         2     0.000    R43C7C.WCKO to     R43C7A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT
                   --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.467ns
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 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[2]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/RAM1

   Delay:               0.529ns  (28.2% logic, 71.8% route), 3 logic levels.

 Constraint Details:

      0.529ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2790 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1397 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.467ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2790 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1397:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R50C5B.CLK to      R50C5B.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2790 (from clk_125_c)
ROUTE         1     0.212      R50C5B.Q0 to      R49C4A.A0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[2]
CTOF_DEL    ---     0.056      R49C4A.A0 to      R49C4A.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9714
ROUTE         1     0.168      R49C4A.F0 to     R48C5C.C1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[2]
ZERO_DEL    ---     0.000     R48C5C.C1 to    R48C5C.WDO2 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1395
ROUTE         1     0.000    R48C5C.WDO2 to     R48C5B.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WD2_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT)
                   --------
                     0.529   (28.2% logic, 71.8% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2790:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R50C5B.CLK clk_125_c
                   --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1397:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R48C5C.CLK clk_125_c
ZERO_DEL    ---     0.000     R48C5C.CLK to    R48C5C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/SLICE_1395
ROUTE         2     0.000    R48C5C.WCKO to     R48C5B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram/WCK_INT
                   --------
                     0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.494ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[7]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/RAM1

   Delay:               0.556ns  (26.8% logic, 73.2% route), 3 logic levels.

 Constraint Details:

      0.556ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2792 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1394 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.494ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2792 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1394:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R49C7B.CLK to      R49C7B.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2792 (from clk_125_c)
ROUTE         1     0.148      R49C7B.Q1 to      R48C7B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[7]
CTOF_DEL    ---     0.056      R48C7B.B0 to      R48C7B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9719
ROUTE         1     0.259      R48C7B.F0 to      R43C7C.D1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[7]
ZERO_DEL    ---     0.000      R43C7C.D1 to    R43C7C.WDO3 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1392
ROUTE         1     0.000    R43C7C.WDO3 to     R43C7B.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WD3_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT)
                   --------
                     0.556   (26.8% logic, 73.2% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2792:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R49C7B.CLK clk_125_c
                   --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1394:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R43C7C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C7C.CLK to    R43C7C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/SLICE_1392
ROUTE         2     0.000    R43C7C.WCKO to     R43C7B.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_0/WCK_INT
                   --------
                     0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.502ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data[9]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/RAM0

   Delay:               0.564ns  (26.4% logic, 73.6% route), 3 logic levels.

 Constraint Details:

      0.564ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2793 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1388 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.502ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2793 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1388:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R49C7C.CLK to      R49C7C.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2793 (from clk_125_c)
ROUTE         1     0.148      R49C7C.Q1 to      R49C7D.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16[9]
CTOF_DEL    ---     0.056      R49C7D.B0 to      R49C7D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9721
ROUTE         1     0.267      R49C7D.F0 to      R48C6C.B1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_data_16_m[9]
ZERO_DEL    ---     0.000      R48C6C.B1 to    R48C6C.WDO1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1387
ROUTE         1     0.000    R48C6C.WDO1 to     R48C6A.WD1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WD1_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT)
                   --------
                     0.564   (26.4% logic, 73.6% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2793:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R49C7C.CLK clk_125_c
                   --------
                     0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1388:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R48C6C.CLK clk_125_c
ZERO_DEL    ---     0.000     R48C6C.CLK to    R48C6C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/SLICE_1387
ROUTE         2     0.000    R48C6C.WCKO to     R48C6A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram/WCK_INT
                   --------
                     0.527   (0.0% logic, 100.0% route), 1 logic levels.

Report:    0.389ns is the minimum delay for this preference.


================================================================================
Preference: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl*" 6.000000 ns ;
            2 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------


Passed: The following path meets requirements by 0.439ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q              pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl[0]  (from clk_125_c +)
   Destination:    FF         Data in        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT +)
                   FF                        pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/RAM0
```

```
   Delay:               0.501ns  (29.7% logic, 70.3% route), 3 logic levels.

 Constraint Details:

      0.501ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1391 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.439ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1391:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R49C5A.CLK to      R49C5A.Q0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798 (from clk_125_c)
ROUTE         1     0.205      R49C5A.Q0 to      R43C4D.D0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_kcntl_16[0]
CTOF_DEL    ---     0.056      R43C4D.D0 to      R43C4D.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9710
ROUTE         1     0.147      R43C4D.F0 to      R43C3C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_kcntl_16_m[0]
ZERO_DEL    ---     0.000      R43C3C.A1 to    R43C3C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1390
ROUTE         1     0.000    R43C3C.WDO0 to     R43C3A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT)
                  --------
                    0.501   (29.7% logic, 70.3% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R49C5A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1391:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R43C3C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C3C.CLK to    R43C3C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/SLICE_1390
ROUTE         2     0.000    R43C3C.WCKO to     R43C3A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_0_ram_1/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.


Passed: The following path meets requirements by 0.641ns

 Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)

   Source:         FF         Q             pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl[1]  (from clk_125_c +)
   Destination:    FF         Data in       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM0  (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT +)
                   FF                       pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/RAM0

   Delay:               0.703ns  (21.2% logic, 78.8% route), 3 logic levels.

 Constraint Details:

      0.703ns physical path delay pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1382 meets
      0.062ns WD_HLD and
      0.000ns delay constraint less
      0.000ns skew requirement (totaling 0.062ns) by 0.641ns

 Physical Path Details:

      Data path pcie/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1382:

   Name    Fanout   Delay (ns)          Site               Resource
REG_DEL     ---     0.093     R49C5A.CLK to      R49C5A.Q1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798 (from clk_125_c)
ROUTE         1     0.278      R49C5A.Q1 to      R46C4B.B0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_kcntl_16[1]
CTOF_DEL    ---     0.056      R46C4B.B0 to      R46C4B.F0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/SLICE_9711
ROUTE         1     0.276      R46C4B.F0 to      R43C4C.A1 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/frm_kcntl_16_m[1]
ZERO_DEL    ---     0.000      R43C4C.A1 to    R43C4C.WDO0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1381
ROUTE         1     0.000    R43C4C.WDO0 to     R43C4A.WD0 pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WD0_INT (to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT)
                  --------
                    0.703   (21.2% logic, 78.8% route), 3 logic levels.

 Clock Skew Details:

      Source Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_frm/u1_frm_ins/SLICE_2798:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R49C5A.CLK clk_125_c
                  --------
                    0.527   (0.0% logic, 100.0% route), 0 logic levels.

      Destination Clock Path pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0 to pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1382:

   Name    Fanout   Delay (ns)          Site               Resource
ROUTE       999     0.527 *FF_TX_H_CLK_0 to     R43C4C.CLK clk_125_c
ZERO_DEL    ---     0.000     R43C4C.CLK to    R43C4C.WCKO pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/SLICE_1381
ROUTE         2     0.000    R43C4C.WCKO to     R43C4A.WCK pcie/u1_dut/u1_dut/u1_dut/u1_dut/u1_phy/u1_scram/u1_txrc/rf_1_ram_1/WCK_INT
                  --------
                    0.527   (0.0% logic, 100.0% route), 1 logic levels.

Report:    0.501ns is the minimum delay for this preference.
```

## Report Summary

```
--------------
----------------------------------------------------------------------------
Preference(MIN Delays)                  |   Constraint|       Actual|Levels
----------------------------------------------------------------------------
                                        |             |             |
FREQUENCY NET "clk_125_c" 125.000000    |             |             |
MHz ;                                   |            -|           -|   1
                                        |             |             |
FREQUENCY NET "can_clk_c" 25.000000 MHz |             |             |
;                                       |            -|           -|   2
                                        |             |             |
FREQUENCY NET "uart_clk_c" 25.000000    |             |             |
MHz ;                                   |            -|           -|   2
                                        |             |             |
FREQUENCY NET "pcie/pclk" 250.000000    |             |             |
MHz ;                                   |            -|           -|   2
                                        |             |             |
FREQUENCY NET                           |             |             |
"pcie/u1_pcs_pipe/ff_rx_fclk_0"         |             |             |
250.000000 MHz ;                        |            -|           -|   1
                                        |             |             |
MULTICYCLE FROM CELL                    |             |             |
"*nfts_rx_skp_cnt*" TO CELL             |             |             |
"*cnt_done_nfts_rx*" 2.000000 X ;       |            -|           -|  10
                                        |             |             |
MULTICYCLE FROM CELL                    |             |             |
"*nfts_rx_skp_cnt*" TO CELL             |             |             |
"*ltssm_nfts_rx_skp*" 2.000000 X ;      |            -|           -|  11
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr|             |             |
*" 6.000000 ns ;                        |     0.000 ns|     0.192 ns|   2
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr|             |             |
*" 6.000000 ns ;                        |     0.000 ns|     0.220 ns|   2
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr|             |             |
*" 6.000000 ns ;                        |     0.000 ns|     0.191 ns|   2
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr|             |             |
*" 6.000000 ns ;                        |     0.000 ns|     0.180 ns|   2
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_da|             |             |
ta*" 6.000000 ns ;                      |     0.000 ns|     0.389 ns|   3
                                        |             |             |
MAXDELAY FROM CELL                      |             |             |
"*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kc|             |             |
ntl*" 6.000000 ns ;                     |     0.000 ns|     0.501 ns|   3
                                        |             |             |
----------------------------------------------------------------------------


All preferences were met.
```

## Clock Domains Analysis

```
------------------------

Found 8 clocks:

Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0   Loads: 3230
   Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_kcntl*" 6.000000 ns ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_frm/u1_frm_ins/frm_data*" 6.000000 ns ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/rd_ptr*" 6.000000 ns ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_ltssm/u1_osenc/wr_ptr*" 6.000000 ns ;
```

   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_rxrc/rd_pntr*" 6.000000 ns ;
   Covered under: MAXDELAY FROM CELL "*u1_dut/u1_phy/u1_scram/u1_txrc/wr_pntr*" 6.000000 ns ;
   Covered under: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*ltssm_nfts_rx_skp*" 2.000000 X ;
   Covered under: MULTICYCLE FROM CELL "*nfts_rx_skp_cnt*" TO CELL "*cnt_done_nfts_rx*" 2.000000 X ;

   Data transfers from:
   Clock Domain: can_clk_c   Source: pll_can/PLLInst_0.CLKOP
      Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ;   Transfers: 10

   Clock Domain: uart_clk_c   Source: pll_uarts/PLLInst_0.CLKOP
      Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ;   Transfers: 63

   Clock Domain: pcie/pclk   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_F_CLK_0
      Covered under: FREQUENCY NET "clk_125_c" 125.000000 MHz ;   Transfers: 37

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: can_clk_c   Source: pll_can/PLLInst_0.CLKOP   Loads: 399
   Covered under: FREQUENCY NET "can_clk_c" 25.000000 MHz ;

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
      Covered under: FREQUENCY NET "can_clk_c" 25.000000 MHz ;   Transfers: 20

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: uart_clk_c   Source: pll_uarts/PLLInst_0.CLKOP   Loads: 1176
   Covered under: FREQUENCY NET "uart_clk_c" 25.000000 MHz ;

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
      Covered under: FREQUENCY NET "uart_clk_c" 25.000000 MHz ;   Transfers: 22

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: pcie/pclk   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_F_CLK_0   Loads: 192
   Covered under: FREQUENCY NET "pcie/pclk" 250.000000 MHz ;
   Blocked under: BLOCK PATH FROM CELL "*ctc_reset_chx*" ;

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
      Covered under: FREQUENCY NET "pcie/pclk" 250.000000 MHz ;   Transfers: 41

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: pcie/u1_pcs_pipe/ff_rx_fclk_0   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_RX_F_CLK_0   Loads: 1
   Covered under: FREQUENCY NET "pcie/u1_pcs_pipe/ff_rx_fclk_0" 250.000000 MHz ;

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0
      Not reported because source and destination domains are unrelated.

   Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK

Clock Domain: jtaghub16_jtck   Source: ep5chub/genblk5_jtage_u.JTCK   Loads: 653
   No transfer within this clock domain is found

   Data transfers from:
   Clock Domain: clk_125_c   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_H_CLK_0

   Clock Domain: pcie/pclk   Source: pcie/u1_pcs_pipe/pcs_top_0/pcs_inst_0.FF_TX_F_CLK_0

Clock Domain: ep5cht/rdcnt_inferred_clock_9   Source: ep5cht/SLICE_1098.Q0   Loads: 23
   No transfer within this clock domain is found

Clock Domain: ep5cht/lclk   Source: ep5cht/losc/SLICE_8253.F0   Loads: 10
   No transfer within this clock domain is found

**Timing summary (Hold):**

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Timing errors: 0  Score: 0
Cumulative negative slack: 0

Constraints cover 202753 paths, 114 nets, and 65996 connections (94.9% coverage)

**Timing summary (Setup and Hold):**

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Timing errors: 0 (setup), 0 (hold)
Score: 0 (setup), 0 (hold)
Cumulative negative slack: 0 (0+0)
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