Application Note AN2292

Layout Guidelines for PSoC™ CapSense™

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Abstract

This Application Note describes layout guidelines for PSoC CapSense applications with regard to PCB layout, overlay thickness and material selection, and chassis design.

Introduction

Capacitive sensing is an interface technology fast gaining traction in front panel display, consumer electronics, and automotive applications. The possibilities truly are endless. With so many applications, design rules must function more as guidelines. This document describes some of these guidelines as layout and system design pertain to PSoC CapSense.

The basic circuit and firmware of the PSoC CapSense solution are relatively simple, the physical design of the switch-operating environment is less so. There are three major categories for consideration when designing with capacitive sensing: the printed circuit board (PCB), the overlay material, and other elements not related to the PCB or capacitive sensing.

For an electrical and physical description of PSoC CapSense, please refer to Application Note AN2233a "Capacitive Key Scan." For a description of the CSR User Module (UM), please refer to the UM data sheet.

PCB Guidelines

The goal of PCB layout is to minimize the effect of non-button, slider and touch-pad elements. Button, slider and touch-pad elements are described as conductive material, such as copper, that makes up the button, slider or touch-pad only.

Traces running from the button, slider or touch-pad to the PSoC are not part of the active sensing area and, hence, are not part of the button, slider or touch-pad. Non-active parts of the circuit serve only to decrease the ability of the sensing area to detect objects.

PCB traces and objects that are not affiliated with capacitive sensing also affect the buttons, slider and touch-pads; this effect is usually detrimental.
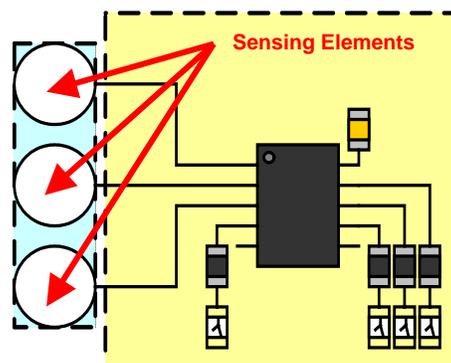

Figure 1. Sensing Element Definition

The goal of PCB layout should be to minimize these interactions or, if they cannot be minimized, make them uniform for all capacitive elements. While the CSR User Module does contain algorithms that adjust for differences in native capacitance across objects in an array, it is good practice to keep things as balanced as possible. The following sections describe the most obvious factors and give guidance for board layout.

Buttons

A button is a single capacitive object connected to the PSoC. It does not need to react to fine changes in capacitance created by partial coverage of the activation area by a conductive object, such as a finger. A button needs only to determine the presence or absence of a conductive object.

Shape

In many capacitive switch designs, the two "plates" of the sensing capacitor are actually adjacent PCB pads or traces. Some example button shapes are shown in Figure 2.

Figure 2 shows a variety of button shapes that can be used with capacitive touch sensing. The top row of buttons in Figure 2 shows inter-digitated traces for use where the cover of the switch is very thin. This construction allows for greater isolation of active buttons when button pitch is very small. The bottom row of buttons in the figure shows single large pads, well spaced from a surrounding ground plane, allowing for longer range sensing.
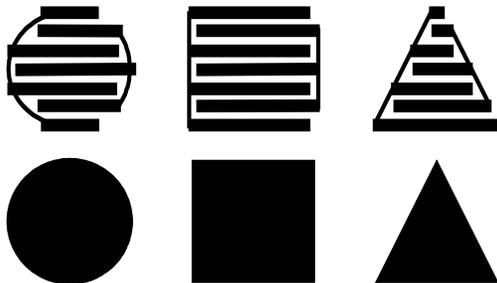

Figure 2. Button Shapes

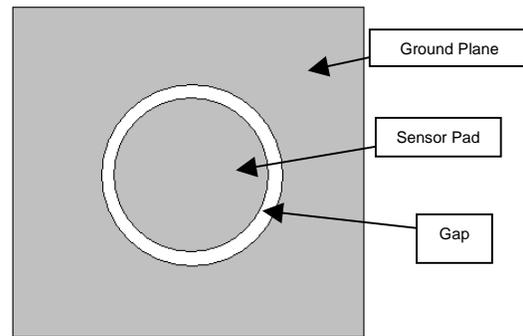An example of a single large button shape surrounded by a ground plane is shown in Figure 3.

Figure 3. Large Button with Ground Plane

Size

All things being equal, larger buttons are typically better. Two buttons connected to the PSoC with identical traces will have different sensitivities if they are different in size.

The effective button area seen by the PSoC is the large conductive pad at the end of the trace (Figure 1). A general rule of thumb (no pun intended) is to size the button to the contact area of the finger. This is demonstrated in Figure 4.
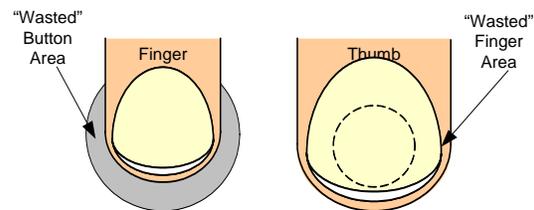

Figure 4. Button Size and Finger Size

Larger buttons are more sensitive. However, the upper limit of button size is set by the effective area of the conductive object to be sensed (approximately 0.8 inches in the case of a human thumb). Figure 5 shows the general trend in button sensitivity versus button size.
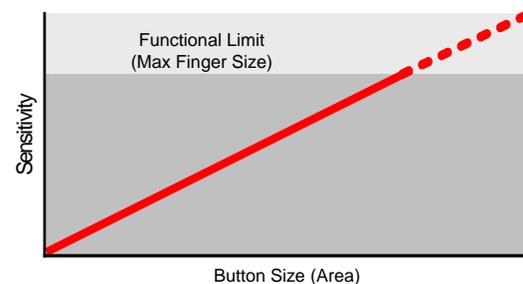

Figure 5. Button Size versus Sensitivity

For sensing through thicker materials (>2.5 mm), buttons with a diameter of at least 0.4 inches (10 mm) are recommended. Smaller buttons can work, but performance is diminished.

Button-Button Spacing
When button pitch is small and buttons are very close together, there may be interaction between buttons. Capacitive elements should be tied to ground when not active to minimize this interaction and decrease sensitivity to noise. Inputs associated with unused capacitive buttons should be programmed to the "Strong" GPIO drive mode.

Button-Ground Clearance
When possible, the ground plane should be placed on the same layer of the board as the buttons. The clearance between the button and ground plane plays an important role in setting the capacitance of the button. This button capacitance is denoted as C_p in this Application Note. Electric field lines fringing between a button and the ground plane are illustrated in Figure 6. C_p is related to this electric field.
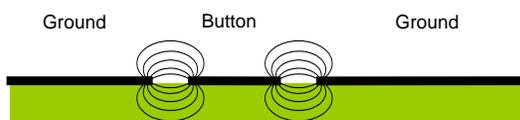

Figure 6. Button-Ground Plane Fringing Fields

The capacitance C_p decreases as the clearance surrounding the button is increased. An example of this dependence of C_p on the gap is shown in Figure 7 for three button sizes (5 mm, 10 mm, 15 mm diameter). In this example, the board is FR4 material with thickness of 0.062 inches (1.57 mm), there is no overlay on top of the buttons, the ground plane is on top of the board with the buttons, and there is no metal layer under the buttons.

A good starting point for most designs is to use a button diameter of 10 mm and a button-ground plane clearance of 0.020-inch (0.5 mm).
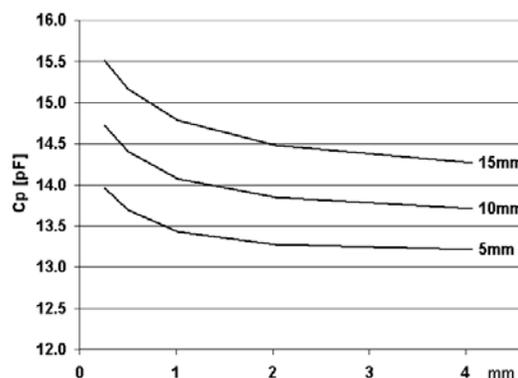

Figure 7. Button Capacitance, C_p, as a Function of Button-Ground Clearance and Button Diameter

Effect of Metal Backing Under Buttons
Figure 6 shows details of the button side of the circuit board. The non-button side of the board is not shown, but it is recommended that a metal fill area be located under the button to control the capacitance of the button. The metal backing increases the signal level of the button counts without increasing the noise level. For a 0.062" (1.57 mm) thick FR4 board, the raw counts from the button without a finger present increase with a metal backing by anywhere from 2% to 20%, depending on a number of factors of the configuration. The raw counts with a finger on the button will also increase with this metal backing, but by a slightly smaller amount. This difference in response tends to regulate the sensitivity (difference in counts). Sensitivity does not improve with a metal layer below the buttons, but the raw counts increase.

The metal backing can be left floating or grounded, since this setting will have little effect on the sensitivity of the buttons. There may be other reasons to float or ground this metal backing, but button sensitivity is not one of these reasons.

Noise
The relaxation oscillator configured by the CSR User Module contains a current source that is digitally programmable. This current source is a Digital-to-Analog Converter (DAC). The parameter ScanSpeed is set in software using the function SetScanSpeed. This function is described in the CSR User Module data sheet. For a given DAC current level, increasing ScanSpeed increases the number of counts from the buttons. The CSR User Module can be configured to operate in either the period measurement or frequency measurement method.

In both methods, if n is the number of counts, then n grows linearly with ScanSpeed, and the noise envelope grows as the square root of n. Looking at these relations between noise, counts and ScanSpeed, it is seen that the ratio of counts-to-noise scales as the square root of ScanSpeed. This means that if your system can tolerate longer scan rates for the buttons, you can improve the signal-to-noise ratio (SNR) by increasing the ScanSpeed.

The DAC current at the heart of the relaxation oscillator in the CSR User Module is set in software by the function SetDacCurrent. As is common in analog circuits, the noise level drops with increasing bias current. In one application, it was observed that a DAC current of 8.8 µA produced a 3-sigma noise level of +/-10%, 4.4 µA produced +/-20%, and 2.2 µA produced +/-30%. These noise levels are for raw counts with a finger touching the buttons. When no buttons are touched, the noise level is well below 1% of the signal level.

If the sensitivity is high, then DAC current can be decreased to save power without sacrificing button performance. With thick overlays or in noisy environments, there may not be enough noise margin at a given current level. In this situation, there may be no choice but to increase the DAC current to make the buttons work.

The overlay thickness influences the noise level. The measured characteristics presented in Figures 8, 9 and 10 demonstrate how increasing overlay thickness relates to noise. In Figure 8, average raw button counts with and without a finger on the buttons are shown as a function of overlay thickness. The 3-sigma noise envelope is shown in Figures 9 and 10, in absolute counts and as a percentage of average raw counts as a function of overlay thickness.

The noise level with a finger touching the button is highly dependent on the environment. The finger acts as an antenna that couples noise into the buttons from fluorescents lights, electric motors, and other noise sources.
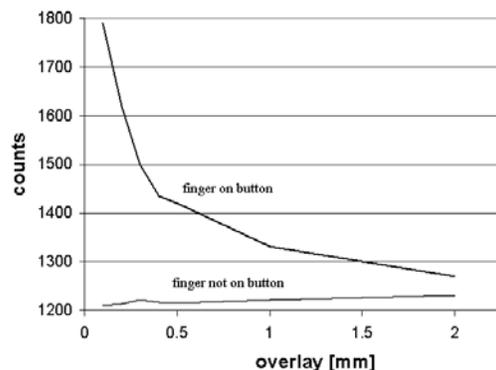

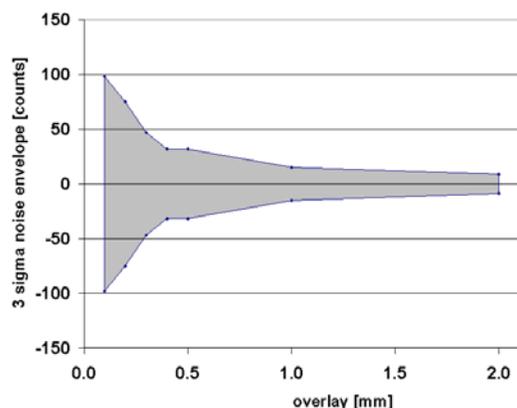**Figure 8. Average Counts as a Function of Overlay Thickness**

Figure 9. Envelope of Noise as a Function of Overlay Thickness with Finger on Button
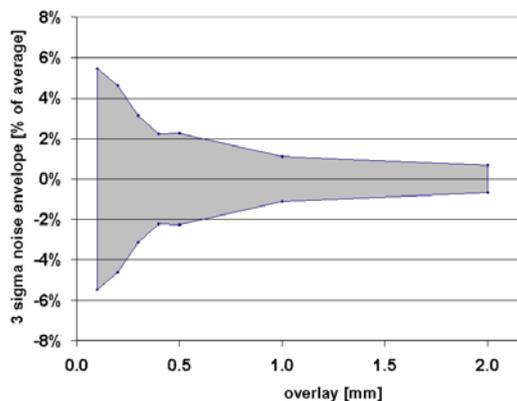

Figure 10. Envelope of Noise as a Percent of the Average Counts

The CSR User Module contains a finger threshold and a noise threshold, which are illustrated in Figure 11. These parameters are set in the Device Editor of PSoC Designer. Counts will change when a finger is placed on the button.

When the change rises above the finger threshold, the button is set to the ON state. When the change falls below the noise threshold, the button is set to the OFF state. The noise envelopes define a Design Margin as shown in Figure 11. The finger and noise thresholds need to be set as shown. The noise threshold is set above the noise envelope associated with no finger on the button. The finger threshold is set below the noise envelope associated with a finger on the button. As mentioned previously, the noise associated with the finger on the button is highly dependent on noise sources that are present in the environment where the buttons are used.
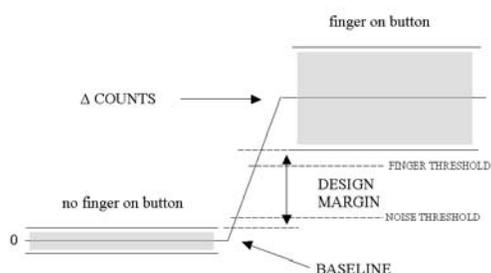

Figure 11. Finger and Noise Threshold Levels Determine the Design Margin

Button Design Example
Time for a design example. Let's say you are an experienced PSoC user that wants to use CapSense buttons in a project. The CSR User Module data sheet contains example code that provides a good stating point for the software side of the design. Here is a list of things to define: button diameter and ground clearance, board material, board thickness, overlay material, overlay thickness, button scan rate and CSR method. The DAC current level and ScanSpeed will be determined as part of the design process. Refer to Application Note AN2233a for more background on CapSense.

Let's select a button diameter of 10 mm and 1 mm clearance, board material of FR4, board thickness of 0.062" (1.57 mm), overlay material of acrylic, and overlay thickness of 1 mm. This allows us to use the graph in Figure 7 to determine C_p. With no overlay, the button has a C_p of 14.1 pF. This value includes the routing capacitance and PSoC pin capacitance. The relaxation oscillator has a ramp time, T_{charge}, which is found with Equation (1).

$$T_{charge} = C_{Button} * V_{BG} / I_{charge} + t_x \qquad (1)$$

- C_{Button} is the button capacitance
- V_{BG} is the bandgap voltage of CSR
- I_{charge} is the DAC current
- t_x is a constant due to CSR internals

C_{Button} is either C_p, the capacitance with no finger present, or $C_p + C_F$, the increased capacitance of the button with a finger present. V_{BG} is 1.3V. t_x is 0.2us. I_{charge} is set in software, with 8.8 μA being a good starting point for designs. Currents lower than this increase the noise level of the counts. Currents higher than this increase the power consumption of the system. To set I_{charge} at 8.8 μA, the function SetDacCurrent is passed the parameters 0x80 and 0 (128*0.069 μA). See the CSR User Module for more details on this function. T_{charge} is typically set in the range of 10 μs to 20 μs. Longer charge times lead to slower scan rates. Shorter charge times lead to quantization effects, as discussed later in this section.

Counts are accumulated in the CSR User Module over a time period, T_{count}, that is set by the ScanSpeed parameter. In period measurement:

$$T_{count} = (ScanSpeed - 2) * T_{charge} \qquad (2)$$

In frequency measurement:

$$T_{count} = (ScanSpeed - 2) / (f_{clock} / 255) \qquad (3)$$

where:

f_{clock} is 24 MHz.

Using the period measurement method, the presence of a finger on the buttons increases the raw counts, n, of the button. Using the frequency measurement method, the presence of a finger decreases the counts. Equations (4) and (5) describe this. In period measurement:

$$n = T_{count} * f_{clock} \qquad (4)$$

In frequency measurement:

$$n = T_{count} / T_{charge} \qquad (5)$$

The period measurement method is used for this example, with a scan rate, T_{count}, of approximately 40 μsec per button. Using Equation (1):

$$T_{charge} = 14.1pF * 1.3V / 8.8 \ \mu A + 0.2 \ \mu s$$
$$= 2.28 \ \mu s \qquad (6)$$

Using Equation (2):

$$40us = (ScanSpeed - 2) * 2.28 \ \mu s \qquad (7)$$

Rearranging Equation (7), and solving for an integer ScanSpeed:

$$\text{ScanSpeed} = 20, \text{ and } T_{count} = 41 \text{ μs} \qquad \textbf{(8)}$$

Using Equation (4), when a finger is not present, the switch is unactuated, and the raw count is given by:

$$n = 41 \text{ μs} * 24 \text{ MHz} = 984 \text{ counts} \qquad \textbf{(9)}$$

As seen in Figure 8, the 1 mm overlay should increase the counts using the period method approximately 10%.

$$n_{finger} = 984 * 1.1 = 1082 \text{ counts} \qquad \textbf{(10)}$$

The noise level without a finger on the button is very low, less than 1% of baseline counts. The noise level with a finger on the button is a function of the overlay thickness. From Figure 10, with a 1 mm overlay, the noise level with a finger present is approximately 1.2%. Plugging the 3-sigma noise levels into Equations (9) and (10), the estimates of the button counts are:

$$n = 984 +/- 5 \text{ counts} \qquad \textbf{(11)}$$

$$n_{finger} = 1082 +/- 13 \text{ counts} \qquad \textbf{(12)}$$

The button counts without a finger present vary randomly between 979 and 989 counts. The button counts with a finger on the button will vary between 1069 and 1095 counts. The design margin between a finger on and off the button is 1069 – 989 = 80 counts.

That is the theory of operation. The system was configured, and then counts were monitored during a button press so that the theory could be compared to actual performance. Figure 12 shows the raw counts of the system during the button press. The measured response agrees quite well with predictions.
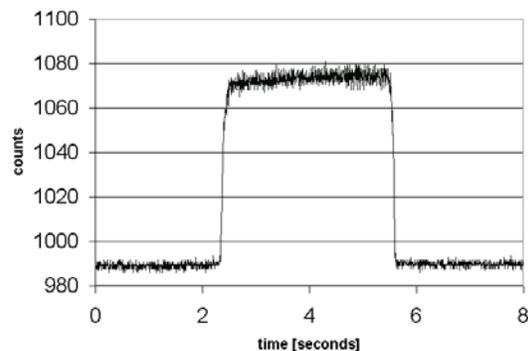

Figure 12. Measured Counts of a Button Press Event for Design Example

Sensitivity and Quantization Error

The nominal frequency of the relaxation oscillator, f_{osc}, is the reciprocal of the charge time without a finger on the button:

$$f_{osc} = 1 / T_{charge} \qquad \textbf{(13)}$$

The sensitivity of the system is the difference in counts between a finger on the button and no finger. The counts using the period method decrease with a finger present, so sensitivity using the period measurement method is:

$$senitivity = n_{finger} - n \qquad \textbf{(14)}$$

Counts using the frequency measurement method increase with a finger present, so sensitivity using the frequency method is:

$$senitivity = n - n_{finger} \qquad \textbf{(15)}$$

The PSoC responds to the comparator in the relaxation oscillator in sync with the 24 MHz clock:

$$T_{sync} = 1/f_{clock} * \text{INT}(T_{charge} * f_{clock}) \qquad \textbf{(16)}$$

Using the period measurement method, an estimate of sensitivity that includes quantization effects is found by substituting T_{sync} for T_{charge} in Equation (2). Figure 13 shows the period method sensitivity as a function of f_{osc}. The parameters in this example are ScanSpeed of 20, Cbutton = 15 pF without a finger and 16.5 pF with a finger. With DAC current of 2.2 μA, the relaxation oscillator will be approximately 100 kHz, which is the recommended operating frequency. Note that sensitivity using the period method decreases as the nominal relaxation oscilllator frequency increases, and the function is smooth even though quantization effects are included. Increasing the oscillator frequency to speed up the scan rate of the buttons decreases the sensitivity of the buttons. This is one of the trade-offs to consider when designing a system using the period measurement method.
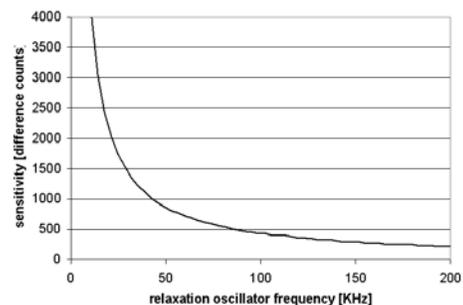

Figure 13. Estimate of Button Sensitivity using Period Measurement Including Quantization Effects

Sensitivity is computed in a similar manner using the frequency measurement method. Figure 14 shows frequency method sensitivity as a function of f_{osc}. The parameters in this example are ScanSpeed of 255, Cbutton = 15 pF without a finger and 16.5 pF with a finger. With DAC current of 2.2 µA, the relaxation oscillator is approximately 100 kHz.
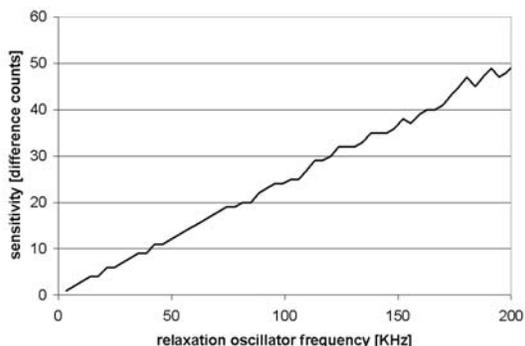

Figure 14. Estimate of Button Sensitivity using Frequency Measurement Including Quantization Effects

Note that sensitivity using the frequency method increases as the nominal relaxation oscilllator frequency increases.

Increasing the oscillator frequency to speed up the scan rate of the buttons increases the sensitivity of the buttons. This is an advantage of using the frequency measurement method, but this advantage has limits. When the oscillator frequency is set to 1 MHz or higher, the sensitivity of the buttons is not well defined, as shown in Figure 15.
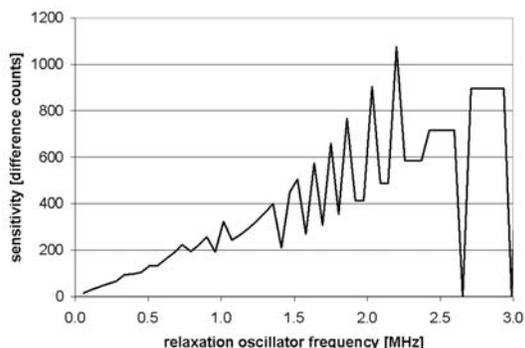

Figure 15. Quantization Effects seen in Frequency Measurement at High Frequency

It is temping to set the oscillator frequency between 2.0 - 2.5 MHz using the frequency method to take advantage of the high sensitivity, but this is not recommended.

With a high oscillator frequency, small changes in system parameters lead to large changes in sensitivity. It is possible for sensitivity to drop to zero as shown in Figure 15.

Sliders
A slider is a set of contiguous capacitive objects connected to the PSoC that are placed in a single line. Sliders are typically linear, running only along a single axis, however, they can follow a contour to any shape provided that it does not intersect any other capacitive sensing element. Sliders use differential capacitance changes between adjacent capacitive elements to determine centroid (center of mass) position of a conductive object with greater resolution than is native using an interpolation algorithm.

Size and Layout
While the general principle of larger elements being longer holds true for sliders as well, there is an upper limit of effectiveness. It is important that a conductive object, such as a finger, not be able to couple to only one element of a slider at a time. This is because interpolated position requires data from more than one element.

To ensure that a conductive object couples to more than one element, each element must be small enough so that the finger overlaps its outside edge. However, it must also be large enough to function (sense) through the application overlay.

Since a slider element is in effect a button sandwiched between two other buttons, the same sizing practices apply to slider elements as to buttons. The area of a slider element should be the same as a 0.4-inch (1.0 cm) button, 0.125 inches^2 (3.14 cm^2). Again, it is possible to utilize slider elements that are smaller than this, but their sensitivity will be diminished.

To create more overlap between slider elements, which provides better differential change between elements, a saw tooth pattern can be used. This pattern can have any number of points, though one or two points is often enough. Figure 16 shows this design with relative dimensions.
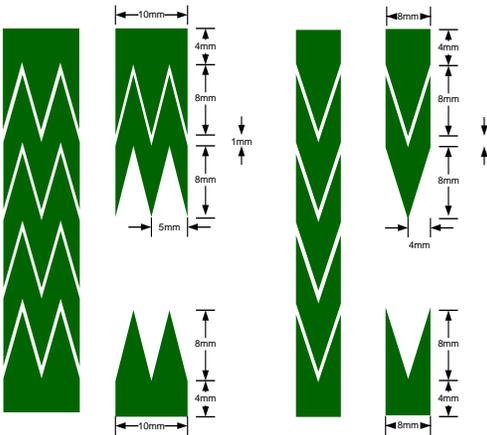
Figure 16. Slider Element Shapes

Spacing

Slider element spacing with regard to the surrounding ground plane is the same as for buttons. The 0.020 inches (0.5 mm) between the slider element and the ground plane reduces the fringe capacitance between the two enough that its impact on sensing is low.

Because sensing pins, when not being actively sensed by the PSoC, are grounded, an active slider element is surrounded on both sides by more ground. For this reason, the same spacing between slider elements should be used, 0.020 inches (0.5 mm). Decreasing this spacing does bring the buttons closer together, however, the positive impact of buttons being closer together for interpolation is outweighed by additional fringe capacitance between slider elements during sensing.

Diplexing

If IOs are at a premium, connecting two slider elements to a single PSoC pin increases the number of slider elements that can be sensed by the PSoC (and thus the lineal distance) two-fold. The CSR User Module Wizard allows the user to select this as an option, however, the pin assignment for elements in the slider is prescribed. An example of a diplexed slider is shown in Figure 17. Six is the minimum practical number of pins to use in a diplexed slider. Table 1 shows some basic diplexing tables. Figures 18 and 19 represent the data collected by the PSoC relative to finger position.

In Figures 18 and 19, note that the capacitance of both elements connected to the PSoC pin increases. Though changes in capacitance are detected in more than one place, there is only one location (of the two) at which all the adjacent elements have a higher capacitance than the baseline.
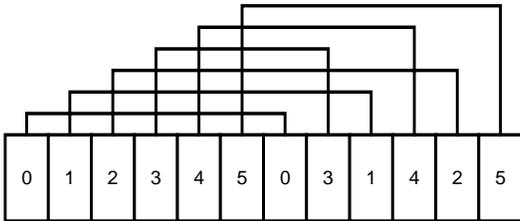

Figure 17. Diplexed Slider Basic Example (Six Pins)

Table 1. Common Diplexing Tables

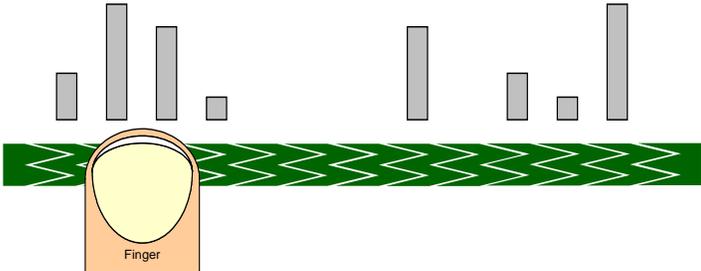| 6 Pins, 12 Elements	8 Pins, 16 Elements	10 Pins, 20 Elements
0	0	0
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
0	6	6
3	7	7
1	0	8
4	3	9
2	6	0
5	1	3
	4	6
	7	9
	2	1
	5	4
		7
		2
		5
		8

Figure 18. Slider Data from Finger Press on Left Side of Slider
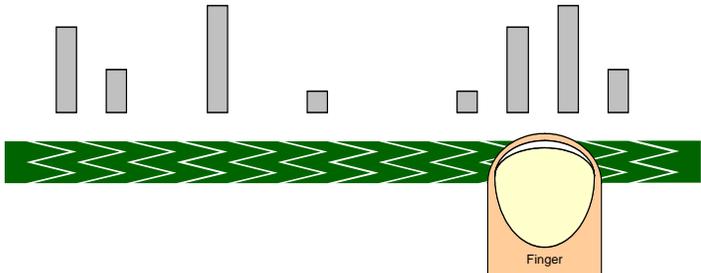

Figure 19. Slider Data from Finger Press on Right Side of Slider

Touch-Pads

A touch-pad, like a slider, is a collection of capacitive elements that detect the position of a conductive object, such as finger, to a resolution greater than that which is native. Touch-pads are capable of defining position on two axes. However, this added functionality comes at a price: overlay material is limited to 0.5 mm and sensing area is diminished.

Size

The size of a touch-pad is a product of the design requirements but is restricted by the physical limitations of capacitive element size. As in a slider, it is necessary for the conductive object to contact or couple to more than one element.

Patterns

There are many different patterns that can be used in touch-pad applications. These patterns involve two sets of capacitive elements: x- and y-axes. The patterns of x- and y-corresponding elements must overlap in their coverage of the area, not in absolute terms but rather to ensure that a finger press is detected by more than one row and column. Multiple x- and y-dimension detection is a requirement for interpolation, covered in the slider description.

Note that the following patterns are suggestions only. These suggestions do not guarantee freedom from existing patents.

The goal of any touch-pad layout pattern is to maximize the area covered by conductive material, such as copper, in relation to the spaces necessary to define the rows and columns. Shapes such as triangles, squares, hexagons, octagons, etc., are all viable options. Examples of some of these shapes are shown in Figures 20 and 21.
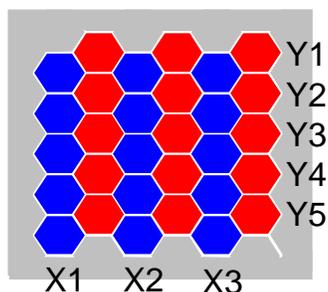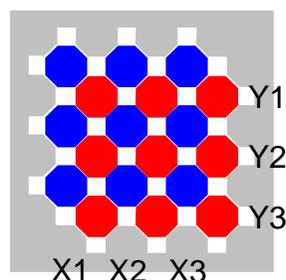
Figure 20. Hexagon Touch-Pad Layout

Figure 21. Octagon Touch-Pad Layout

In both of the above layouts and for touch-pads in general, it is good practice to surround the touch-pad with a ground plane that follows the contours of the sensing elements. This is to simulate the effect of the grounded sensing elements that surround elements on the inside when only one pin of the PSoC device is active.

Traces that run to the touch-pad from the PSoC are on the bottom layer of a 2-layer PCB. It is important to extend all traces to the end of the board; this makes PSoC pins along a given access behave more uniformly.

Non-CapSense PCB Elements

When designing for capacitive sensing, it is important to account for more than just the circuit that is involved directly with the sensing. The entire circuit has an effect on the capacitance of the sensor elements and their traces. Most often, PCB elements have a negative effect on sensitivity. Hardware elements such as capacitors, connectors, resistors, other ICs, etc., add to the C_P (native capacitance) of buttons to which they make contact. Traces, even those not involved with sensing, can couple to sensing elements. High-frequency communication lines can impact the relaxation oscillator. It is for this reason and many others that the whole of board layout must be considered and optimized for capacitive sensing.

Board Dimensions

PCB dimensions are most often determined by the physical limitations of the design, be they small or large.

Board Area

For capacitive sensing, the total board area is not important. What is important is the area covered by the sensing elements and traces. It is good practice to keep this area down by keeping the distance between the PSoC and the sensors to a minimum. Centering the PSoC among the sensor elements is one way to ensure optimized board area.

Board Thickness

Standard PCB thicknesses does not routinely create a problem for capacitive sensing. Designs built on 0.020-, 0.047-, and 0.063-inch thick PCBs are quite capable of sensing through necessary material overlays. Thinner FR4 or even Kapton may sacrifice some sensitivity. If design guidelines do not exist for a circuit board material or board thickness required for an application, it is recommended that a PCB be prototyped with representative buttons and ground plane so that C_p can be characterized. As board thicknesses decreases, C_p increases. As discussed earlier in this Application Note, sensitivity is controlled by C_p, so board thickness plays an important role in the performance of the CapSense system.

A metal layer or ground plane under the buttons on the non-button side of the circuit board is often helpful. If a multi-layer board is used, the area under switches on inner layers should be clear. Refer to the Button section of this Application Note for a discussion of the effect of metal backing under buttons.

Capacitive Sensing Traces

A described above, traces that run from the PSoC to the sensors decrease the sensitivity of the sensors by increasing C_P and decreasing the SNR. The signal is decreased by the trace length because it adds parallel capacitance to the sensing circuit that does not interact with finger position, and therefore does not contribute to the signal. Noise is increased by trace length because the trace picks up noise from both in-circuit and external noise sources.

Length

Shortening trace lengths from the PSoC to the sensor reduces the opportunity for other design elements to couple to sensing traces. Make traces from the PSoC to the sensor as short as possible. Use the minimum number of vias consistent with routing for minimum length.

Width

Trace width adds to the sensor C_P by adding copper area to the system. It also increases coupling to elements on other layers by way of the increased copper area. Trace widths between 0.0065 inches and 0.008 inches suffice for most applications.

Placement

Placement of capacitive sense traces must minimize interaction with other design elements, including other capacitive sense traces, whenever possible.

Also, keeping traces on the side of the PCB opposite the user decreases the impact of a finger on the traces, ensuring that all capacitive change on the sensor pin is from the finger's (or other conducting object's) interaction with the active sensing area, and not from interaction between the finger and trace.

Do not run capacitive sensing traces in close proximity with and parallel to high-frequency communication lines, such as an I2C or SPI master. The frequency in communication lines can alter the performance of the oscillator and impair performance of the capacitive sensors. If it is necessary to cross communication lines with sensor pins, be sure the intersection is orthogonal, as shown in Figures 22 and 23.
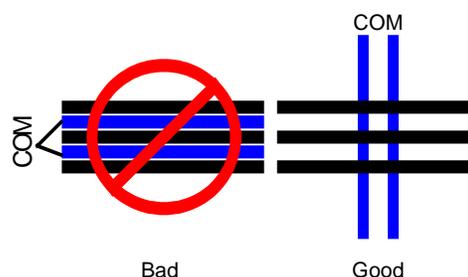

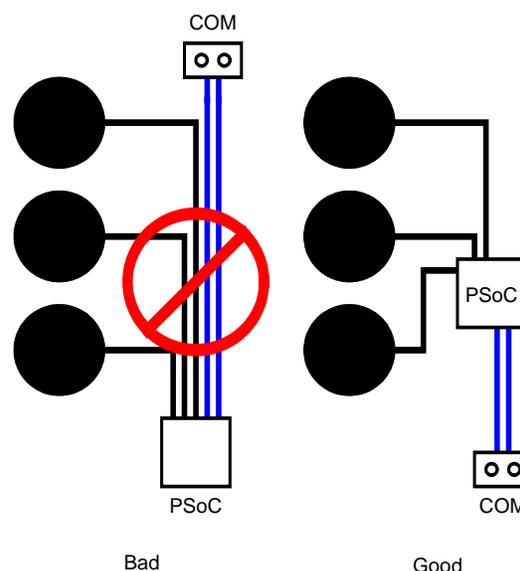**Figure 22. Multi-Layer Treatment of Sensing and Communication Lines**

Figure 23. Same-Layer Treatment of Sensing and Communication Lines

One effective method for reducing the interaction between communication traces and sensor traces is to isolate each by port assignment. Figure 24 shows a basic version of this isolation for a 32-pin QFN package. Communication and addressing pins are assigned to Port 1. Sensing is achieved on the other three ports. Because each function is isolated, the PSoC can be oriented so that there is no crossing for communication and sensing traces.
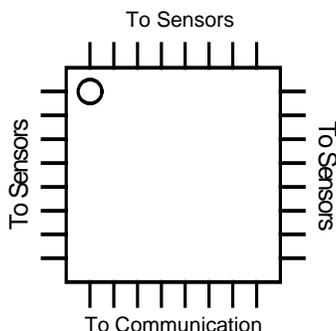

Figure 24. Port Isolation for Communication and Sensing

Ground Plane
Most work with a ground plane in CapSense circuits seeks to decrease the interaction between ground and the sensing traces. However, there are cases when interaction between ground and the sensing traces is both prescribed and welcome. The ground plane in most applications should be on the sensor side of the board. Refer to the Button section of this Application Note for a discussion on buttons, the ground plane, and the clearance between them.

In designs where vertical height restrictions are aggressive and metal and other objects are positioned near the sensing PCB, a ground plane between the sensors protects the circuit and yields more consistent results at some cost in sensitivity. Often the most important aspect of sensing is reliability of the data. This is increased with a constant interaction between metal and sensing elements.
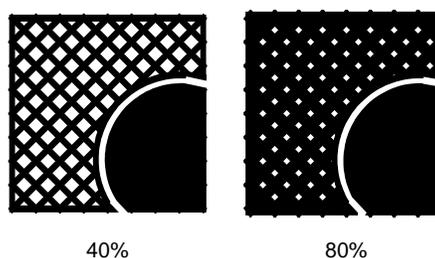
Location
When board height restrictions are not important and there is nothing of consequence close to the non-sensor side of the PCB, run the sense traces along the non-sensor layer of the PCB and via them to the sensors. The ground plane is located on the top layer of the board to protect the system from accidental detection through interaction with the sense lines rather than the sensors.

When board height restrictions are important and there are elements on the non-sensor side of the PCB, traces can run along the same layer as the buttons or not. The ground plane should be placed on the non-sensor side and cover area even underneath the buttons.

% Fill
For designs that have the ground plane on the sensor layer, a 40% fill protects the sensing traces while not interacting with them too much. For designs that have the ground plane on the non-sensor layer and require shielding from other design elements, a 60-80% fill protects the circuit. A 100% fill is not necessary and only serves to increase the C_P value of each sensor without offering any appreciable protection over 60-80%.

Figure 25. Partial Ground Fill

Other Board Elements
Other PCB elements, such as connectors, capacitors, resistors, and other ICs, impact sensing and sensitivity by coupling to capacitive sensors and traces. Efforts made to limit this interaction will improve the SNR and ultimately the sensitivity of the sensor circuit.

Sensing lines that are attached to other board elements, such as ISSP programming headers, are more sensitive to external noise and have a higher C_P value due to the increased area of metal in the line. It is recommended that sensing lines in capacitive sensing applications be connected to sensors only. This means avoiding placing switches on the programming pins, P1[0] and P1[1].

Sensor and sensing traces near large metal elements on the circuit will interact with these objects. This interaction is most often detrimental. It is recommended that sensor and sensing traces be isolated from other circuit elements. This is especially true of antennae and other signal sending/receiving elements. Refer to Application Note AN2318 "EMC Design Considerations for PSoC CapSense(TM) Applications" for information on this topic.

Overlay

It is rare that a design gives the end user access to the bare PCB or one using only soldermask. Rather, there is usually a material overlay across the surface of the PCB that protects the user from the circuit and the circuit from the environment.

Properties

Overlays in CapSense applications MUST not be conductive. Metals and other conductive materials do not form the dielectric of the capacitor when placed between two conductive plates, such as the finger and the sensor.

The capacitance of a parallel plate capacitor is given in Equation (17).

$$C = \frac{\varepsilon_r \varepsilon_0 A}{d} \qquad \textbf{(17)}$$

The geometry of this simple system is captured in the ratio A/d. A is the area of the conductive plates, d is the distance between the plates, ε_r is the dielectric constant (permittivity) of the material between the sensors, and ε_0 is the permittivity of free space.

The geometry of the capacitive sensor is more complex than the parallel plate capacitor. The conductors in the sensor include the finger and PCB copper. In general, the geometry of this capacitive system is captured by the function $f(A,d)$. Equation (18) states the relation between geometry, the dielectric constant, and the system capacitance.

$$C = \varepsilon_r \varepsilon_0 f(A,d) \qquad \textbf{(18)}$$

Like the parallel plate capacitor, the capacitance of the sensor is directly proportional to ε_r.

Different Materials
Dielectric constants of some common overlay materials are listed in Table 2. Materials with dielectrics between 2.0 and 8.0 are well suited to capacitive sensing applications.

Table 2. Dielectric Constants of Common Materials

Material	ε_r
Air	1.0
Formica	4.6 – 4.9
Glass (Standard)	7.6 – 8.0
Glass (Ceramic)	6.0
Mylar®	3.2
Plexiglass	2.8
ABS	3.8 – 4.5
Wood	1.2 – 2.5

Air, with a dielectric on 1.0, is not well suited to capacitive sensing applications. In fact, it is four times more difficult to sense through air as it is to sense through ABS plastic. This does not necessarily translate into four times the sensitivity with an ABS overlay as compared to air. A high dielectric constant material will have slightly higher counts as compared to a different material with the same overlay thickness of a lower dielectric constant. It is for this reason the air gaps between sensors and the overlay material are not recommended. Eliminating air gaps is also a good practice from a mechanical point of view. See the Adhesives section below.

A design parameter that has a bigger influence on raw counts than the dielectric constant of the overlay material is the clearance between the button and ground plane. Raw counts can be increased more easily through adjustment of this clearance than through selection of the overlay. It is good that the system has this characteristic since the dielectric constant of the overlay material may not be well controlled from batch to batch, while PCB features are tightly controlled.

Thickness

Overlay thickness is inversely proportional to sensitivity, as shown in Figure 26. See the Button section of this Application Note for a specific example of this characteristic.
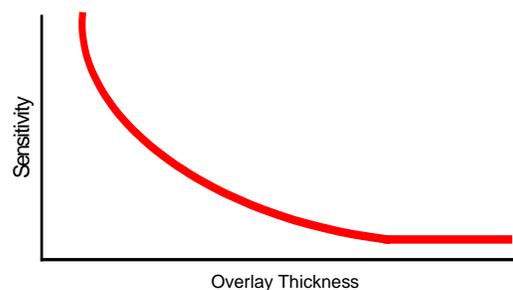

Figure 26. Overlay Thickness versus Sensitivity

Table 3 lists the recommended maximum overlay thicknesses for PSoC CapSense applications.

Table 3. Design Element Overlay Thickness

Design Element	ε
Button	<4.0 mm
Slider	<1.0 mm
Touch-Pad	<0.5 mm

Adhesives

Overlay materials must not have intermittent contact with the sensing PCB. To ensure constant contact, an adhesive may be necessary. When choosing an adhesive, it is important that it not be able to hold a charge at all. Use of "double-sided tape" will impair performance of the capacitive sensing circuit since the tape itself has some conductive charge absorptive properties.

Two widely used adhesives for overlays are made by 3M, 467 and 468. Both these adhesives are sticky on two sides and do not hold a charge. They have been commonly used by label and membrane switch manufacturers for years and are considered industry standard. They are also thin enough not to impair sensing. For complete information on these adhesives and to find out how to get samples for prototyping, see the "Products" page of the 3M web site at http://www.3m.com.

Chassis

The chassis of a CapSense application, as discussed with reference to specific design elements in the previous sections, impacts the sensitivity of capacitive sensors by interacting with the sensors and the traces from the IC to the sensors.

The three most common chassis design elements that impact sensing are metal support structures, communication cables, and separation between the sensing PCB and the overlay material.

The latter is discussed in the Overlay section above. Metal support structures must be kept away from sensing elements and traces when possible. Where support structures are necessary, non-metal structures are recommended. If metal is required, a bottom-side ground plane of 80% fill is recommended to protect the circuit.

Communication cables and wires interact with the sensing elements by imposing their own high-frequency signals on that of the relaxation oscillator. Communication cables must be kept away from sensors and traces when possible or shielded from sensors through the use of an 80%-fill ground plane. Refer to Application Note AN2318 for information on this topic.

Conclusion

The nature of capacitive sensing, the mystery of electric fields, creates some difficult challenges in design. There is no silver bullet for all designs. Rather, there are only functional, empirical design guidelines to help layout and design engineers find the golden path to design. Capacitive sensing may take multiple design revisions to find the best layout for the application. However, knowledge of what has worked in the past and an understanding of the physics at work can reduce design revisions and accelerate design time.

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