Three Phase PWM Motor Driver

Check for Samples: DRV8312, DRV8332

FEATURES

- **High-Efficiency Power Stage (up to 97%) with Low $R_{DS(on)}$ MOSFETs (80 mΩ at T_J = 25°C)**
- **Operating Supply Voltage up to 50 V (70 V Absolute Maximum)**
- **DRV8312 (power pad down): up to 3.5 A Continuous Phase Current (6.5 A Peak)**
- **DRV8332 (power pad up): up to 8 A Continuous Phase Current (13 A Peak)**
- **Independent Control of Three Phases**
- **PWM Operating Frequency up to 500 kHz**
- **Integrated Self-Protection Circuits Including Undervoltage, Overtemperature, Overload, and Short Circuit**
- **Programmable Cycle-by-Cycle Current Limit Protection**
- **Independent Supply and Ground Pins for Each Half Bridge**
- **Intelligent Gate Drive and Cross Conduction Prevention**
- **No External Snubber or Schottky Diode is Required**

APPLICATIONS

- **BLDC Motors**
- **Three Phase Permanent Magnet Synchronous Motors**
- **Inverters**
- **Half Bridge Drivers**
- **Robotic Control Systems**

DESCRIPTION

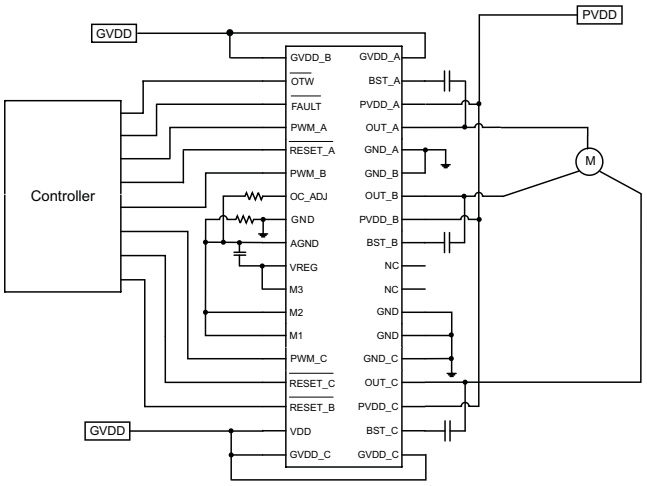
The DRV8312/32 are high performance, integrated three phase motor drivers with an advanced protection system.

Because of the low $R_{DS(on)}$ of the power MOSFETs and intelligent gate drive design, the efficiency of these motor drivers can be up to 97%, which enables the use of smaller power supplies and heatsinks, and are good candidates for energy efficient applications.

The DRV8312/32 require two power supplies, one at 12 V for GVDD and VDD, and another up to 50 V for PVDD. The DRV8312/32 can operate at up to 500-kHz switching frequency while still maintain precise control and high efficiency. They also have an innovative protection system safeguarding the device against a wide range of fault conditions that could damage the system. These safeguards are short-circuit protection, overcurrent protection, undervoltage protection, and two-stage thermal protection. The DRV8312/32 have a current-limiting circuit that prevents device shutdown during load transients such as motor start-up. A programmable overcurrent detector allows adjustable current limit and protection level to meet different motor requirements.

The DRV8312/32 have unique independent supply and ground pins for each half bridge, which makes it possible to provide current measurement through external shunt resistor and support half bridge drivers with different power supply voltage requirements.

Simplified Application Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted (1)

	VALUE
VDD to GND	–0.3 V to 13.2 V
GVDD_X to GND	–0.3 V to 13.2 V
PVDD_X to GND_X (2)	–0.3 V to 70 V
OUT_X to GND_X (2)	–0.3 V to 70 V
BST_X to GND_X (2)	–0.3 V to 80 V
Transient peak output current (per pin), pulse width limited by internal over-current protection circuit.	16 A
Transient peak output current for latch shut down (per pin)	20 A
VREG to AGND	–0.3 V to 4.2 V
GND_X to GND	–0.3 V to 0.3 V
GND to AGND	–0.3 V to 0.3 V
PWM_X, $\overline{\text{RESET\_X}}$ to GND	–0.3 V to 4.2 V
OC_ADJ, M1, M2, M3 to AGND	–0.3 V to 4.2 V
$\overline{\text{FAULT}}$, $\overline{\text{OTW}}$ to GND	–0.3 V to 7 V
Maximum continuous sink current ($\overline{\text{FAULT}}$, $\overline{\text{OTW}}$)	9 mA
Maximum operating junction temperature range, T_J	-40°C to 150°C
Storage temperature, T_{STG}	–55°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represent the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV8312 DDW PACKAGE 44 PINS	DRV8332 DKD PACKAGE 36 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	24.5	13.3 (with heat sink)	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	7.8	0.4	
θ_{JB}	Junction-to-board thermal resistance(4)	5.5	13.3	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.1	0.4	
ψ_{JB}	Junction-to-board characterization parameter(6)	5.4	13.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.2	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
PVDD_X	Half bridge X (A, B, or C) DC supply voltage	0	50	52.5	V
GVDD_X	Supply for logic regulators and gate-drive circuitry	10.8	12	13.2	V
VDD	Digital regulator supply voltage	10.8	12	13.2	V
I_{O_PULSE}	Pulsed peak current per output pin (could be limited by thermal)			15	A
I_O	Continuous current per output pin (DRV8332)			8	A
F_{SW}	PWM switching frequency			500	kHz
R_{OCP_CBC}	OC programming resistor range in cycle-by-cycle current limit modes	22		200	kΩ
R_{OCP_OCL}	OC programming resistor range in OC latching shutdown modes	19		200	kΩ
C_{BST}	Bootstrap capacitor range	33		220	nF
t_{ON_MIN}	Minimum PWM pulse duration, low side, for charging the Bootstrap capacitor		50		ns
T_A	Operating ambient temperature	-40		85 (1)	°C

(1) Depending on power dissipation and heat-sinking, the DRV8312/32 can support ambient temperature in excess of 85°C. Refer to the package heat dissipation ratings table and package power deratings table.

PACKAGE HEAT DISSIPATION RATINGS

PARAMETER	DRV8312	DRV8332
$R_{\theta JC}$, junction-to-case (power pad / heat slug) thermal resistance	1.1 °C/W	0.9 °C/W
$R_{\theta JA}$, junction-to-ambient thermal resistance	25 °C/W	This device is not intended to be used without a heatsink. Therefore, $R_{\theta JA}$ is not specified. See the *Thermal Information* section.
Exposed power pad / heat slug area	34 mm^2	80 mm^2

PACKAGE POWER DERATINGS (DRV8312) (1)

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
44-PIN TSSOP (DDW)	5.0 W	40.0 mW/°C	3.2 W	2.6 W	1.0 W

(1) Based on EVM board layout

MODE SELECTION PINS

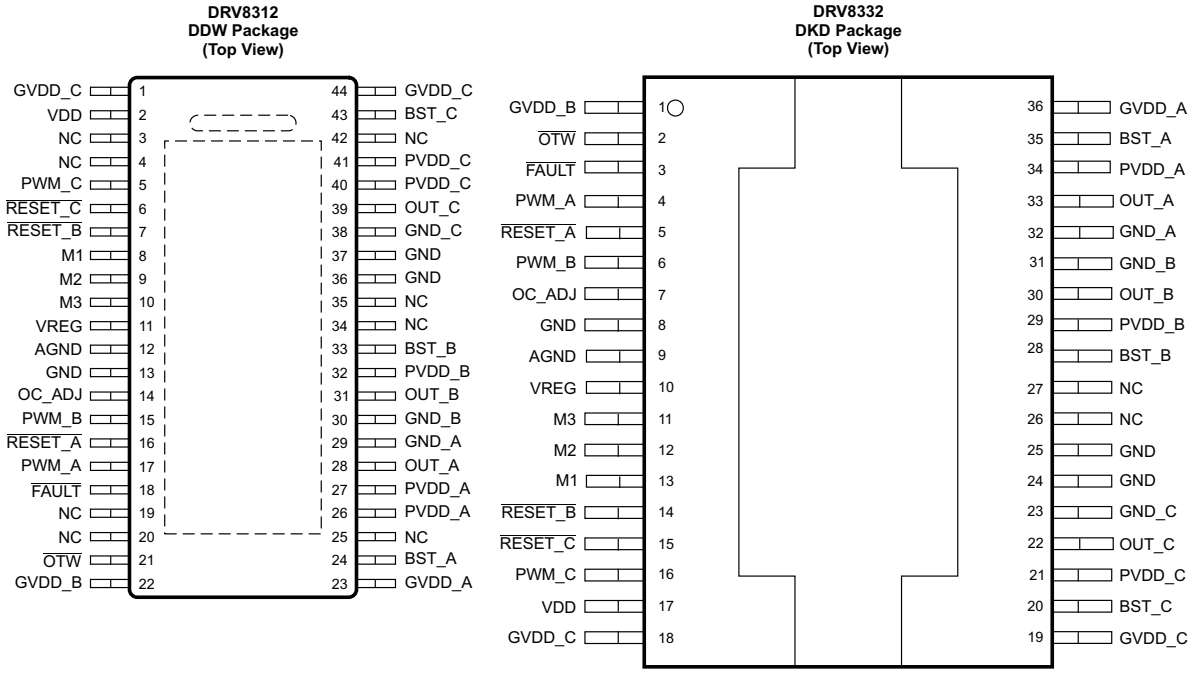
MODE PINS			OUTPUT CONFIGURATION	DESCRIPTION
M3	M2	M1		
1	0	0	1 3PH or 3 HB	Three-phase or three half bridges with cycle-by-cycle current limit
1	0	1	1 3PH or 3 HB	Three-phase or three half bridges with OC latching shutdown (no cycle-by-cycle current limit)
0	x	x	Reserved	
1	1	x	Reserved	

DEVICE INFORMATION

Pin Assignment

Here are the pinouts for the DRV8312/32:

- DRV8312: 44-pin TSSOP power pad down DDW package. This package contains a thermal pad that is located on the bottom side of the device for dissipating heat through PCB.
- DRV8332: 36-pin PSOP3 DKD package. This package contains a thick heat slug that is located on the top side of the device for dissipating heat through heatsink.



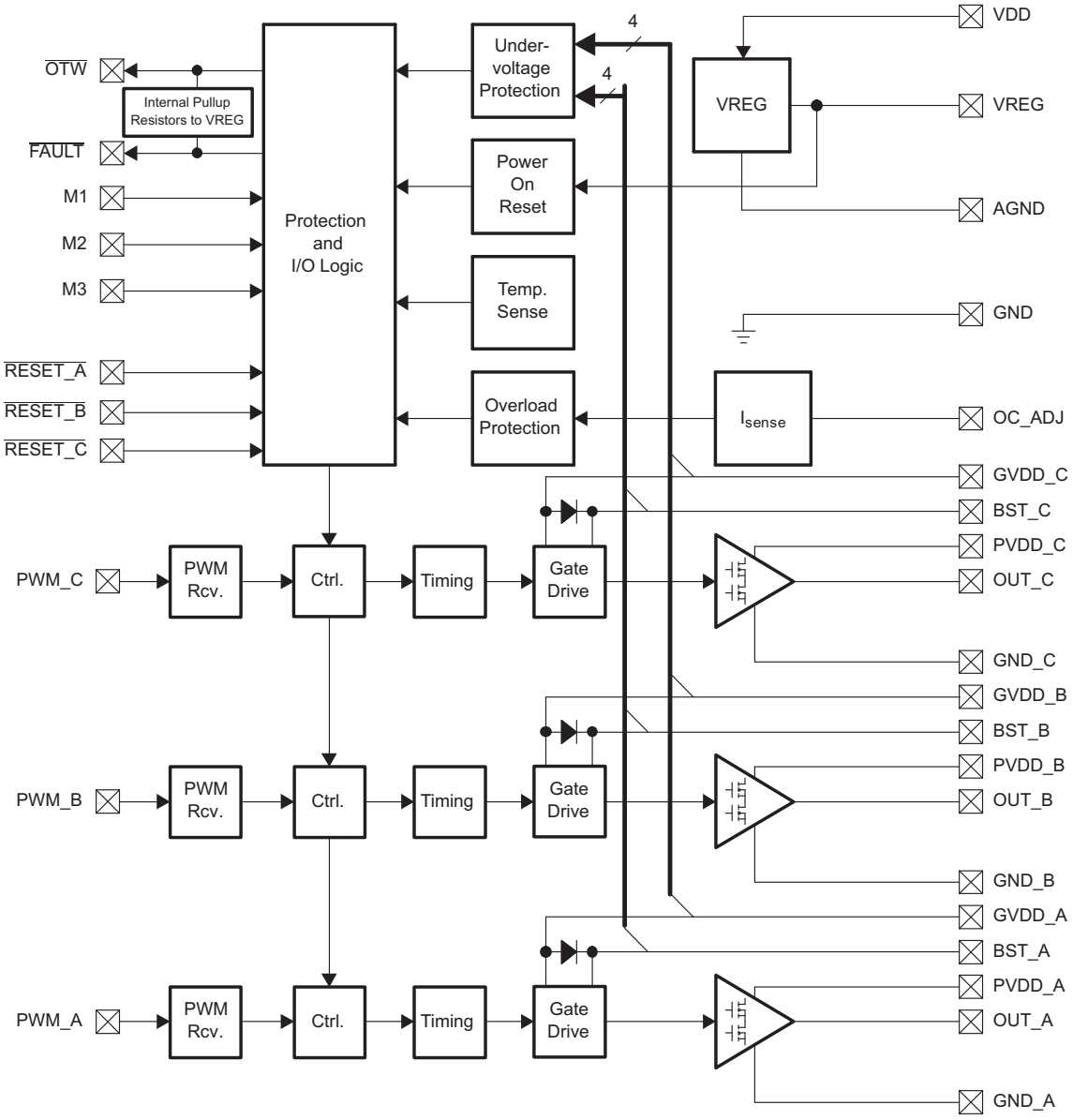
Pin Functions

PIN			FUNCTION (1)	DESCRIPTION
NAME	DRV8312	DRV8332		
AGND	12	9	P	Analog ground
BST_A	24	35	P	High side bootstrap supply (BST), external capacitor to OUT_A required
BST_B	33	28	P	High side bootstrap supply (BST), external capacitor to OUT_B required
BST_C	43	20	P	High side bootstrap supply (BST), external capacitor to OUT_C required
GND	13, 36, 37	8	P	Ground
GND_A	29	32	P	Power ground for half-bridge A
GND_B	30	31	P	Power ground for half-bridge B
GND_C	38	23	P	Power ground for half-bridge C
GVDD_A	23	36	P	Gate-drive voltage supply
GVDD_B	22	1	P	Gate-drive voltage supply
GVDD_C	1, 44	18, 19	P	Gate-drive voltage supply
M1	8	13	I	Mode selection pin
M2	9	12	I	Reserved mode selection pin. AGND connection is recommended
M3	10	11	I	Reserved mode selection pin, VREG connection is recommended
NC	3,4,19,20,25,34,35 ,42	26,27	-	No connection pin. Ground connection is recommended
OC_ADJ	14	7	O	Analog overcurrent programming pin, requires resistor to AGND

(1) I = input, O = output, P = power, T = thermal

PIN			FUNCTION (1)	DESCRIPTION
NAME	DRV8312	DRV8332		
$\overline{\text{OTW}}$	21	2	O	Overtemperature warning signal, open-drain, active-low. An internal pull-up resistor to VREG (3.3 V) is provided on output. Level compliance for 5-V logic can be obtained by adding external pull-up resistor to 5 V
OUT_A	28	33	O	Output, half-bridge A
OUT_B	31	30	O	Output, half-bridge B
OUT_C	39	22	O	Output, half-bridge C
PVDD_A	26,27	34	P	Power supply input for half-bridge A requires close decoupling capacitor to ground.
PVDD_B	32	29	P	Power supply input for half-bridge B requires close decoupling capacitor to gound.
PVDD_C	40,41	21	P	Power supply input for half-bridge C requires close decoupling capacitor to ground.
PWM_A	17	4	I	Input signal for half-bridge A
PWM_B	15	6	I	Input signal for half-bridge B
PWM_C	5	16	I	Input signal for half-bridge C
$\overline{\text{RESET\_A}}$	16	5	I	Reset signal for half-bridge A, active-low
$\overline{\text{RESET\_B}}$	7	15	I	Reset signal for half-bridge B, active-low
$\overline{\text{RESET\_C}}$	6	15	I	Reset signal for half-bridge C, active-low
$\overline{\text{FAULT}}$	18	3	O	Fault signal, open-drain, active-low. An internal pull-up resistor to VREG (3.3 V) is provided on output. Level compliance for 5-V logic can be obtained by adding external pull-up resistor to 5 V
VDD	2	17	P	Power supply for digital voltage regulator requires capacitor to ground for decoupling.
VREG	11	10	P	Digital regulator supply filter pin requires 0.1-µF capacitor to AGND.
THERMAL PAD	--	N/A	T	Solder the exposed thermal pad at the bottom of the DRV8312DDW package to the landing pad on the PCB. Connect the landing pad through vias to large ground plate for better thermal dissipation.
HEAT SLUG	N/A	--	T	Mount heatsink with thermal interface to the heat slug on the top of the DRV8332DKD package to improve thermal dissipation.

SYSTEM BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

T_A = 25 °C, PVDD = 50 V, GVDD = VDD = 12 V, f_{SW} = 400 kHz, unless otherwise noted. All performance is in accordance with recommended operating conditions unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal Voltage Regulator and Current Consumption						
V_{REG}	Voltage regulator, only used as a reference node	VDD = 12 V	2.95	3.3	3.65	V
I_{VDD}	VDD supply current	Idle, reset mode		9	12	mA
		Operating, 50% duty cycle		10.5		
I_{GVDD_X}	Gate supply current per half-bridge	Reset mode		1.7	2.5	mA
		Operating, 50% duty cycle		8		
I_{PVDD_X}	Half-bridge X (A, B, or C) idle current	Reset mode		0.7	1	mA
Output Stage						
$R_{DS(on)}$	MOSFET drain-to-source resistance, low side (LS)	T_J = 25°C, GVDD = 12 V		80		mΩ
	MOSFET drain-to-source resistance, high side (HS)	T_J = 25°C, GVDD = 12 V		80		mΩ
V_F	Diode forward voltage drop	T_J = 25°C - 125°C, I_O = 5 A		1		V
t_R	Output rise time	Resistive load, I_O = 5 A		14		ns
t_F	Output fall time	Resistive load, I_O = 5 A		14		ns
t_{PD_ON}	Propagation delay when FET is on	Resistive load, I_O = 5 A		38		ns
t_{PD_OFF}	Propagation delay when FET is off	Resistive load, I_O = 5 A		38		ns
t_{DT}	Dead time between HS and LS FETs	Resistive load, I_O = 5 A		5.5		ns
I/O Protection						
$V_{uvp,G}$	Gate supply voltage GVDD_X undervoltage protection threshold			8.5		V
$V_{uvp,hyst}$ (1)	Hysteresis for gate supply undervoltage event			0.8		V
OTW (1)	Overtemperature warning		115	125	135	°C
OTW_{hyst} (1)	Hysteresis temperature to reset $\overline{OTW}$ event			25		°C
OTSD (1)	Overtemperature shut down			150		°C
$OTE\text{-}OTW_{differential}$ (1)	OTE-OTW overtemperature detect temperature difference			25		°C
$OTSD_{HYST}$ (1)	Hysteresis temperature for $\overline{FAULT}$ to be released following an OTSD event			25		°C
I_{OC}	Overcurrent limit protection	Resistor—programmable, nominal, R_{OCP} = 27 kΩ		9.7		A
I_{OCT}	Overcurrent response time	Time from application of short condition to Hi-Z of affected FET(s)		250		ns
Static Digital Specifications						
V_{IH}	High-level input voltage	PWM_A, PWM_B, PWM_C, M1, M2, M3	2		3.6	V
V_{IH}	High-level input voltage	$\overline{RESET\_A}$, $\overline{RESET\_B}$, $\overline{RESET\_C}$	2		3.6	V
V_{IL}	Low-level input voltage	PWM_A, PWM_B, PWM_C, M1, M2, M3, $\overline{RESET\_A}$, $\overline{RESET\_B}$, $\overline{RESET\_C}$			0.8	V
I_{lkg}	Input leakage current		-100		100	µA
OTW / FAULT						
R_{INT_PU}	Internal pullup resistance, $\overline{OTW}$ to VREG, $\overline{FAULT}$ to VREG		20	26	35	kΩ
V_{OH}	High-level output voltage	Internal pullup resistor only	2.95	3.3	3.65	V
		External pullup of 4.7 kΩ to 5 V	4.5		5	
V_{OL}	Low-level output voltage	I_O = 4 mA		0.2	0.4	V

(1) Specified by design

TYPICAL CHARACTERISTICS

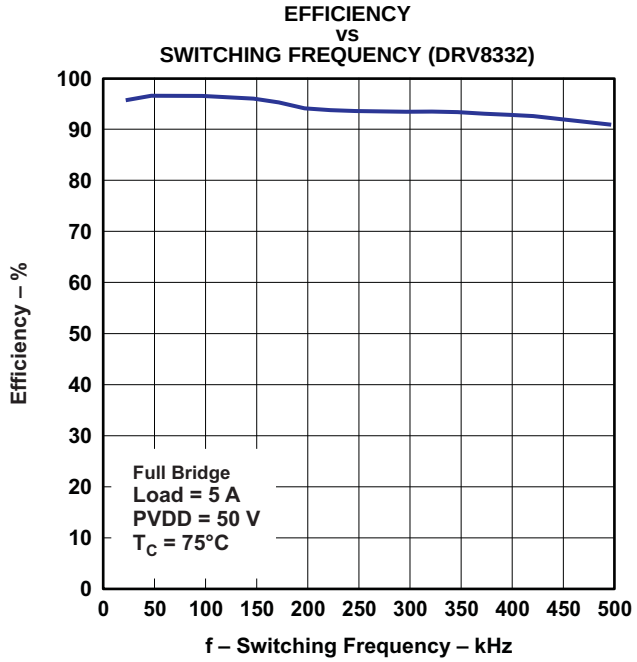


Figure 1.

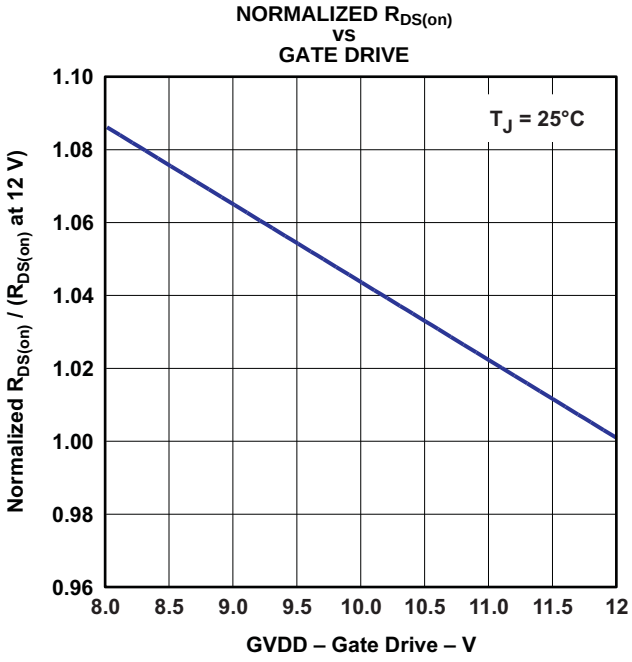


Figure 2.

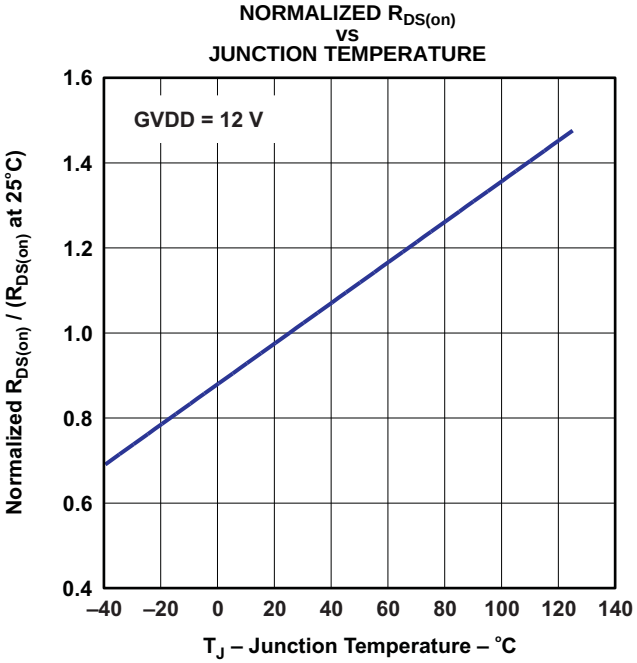


Figure 3.

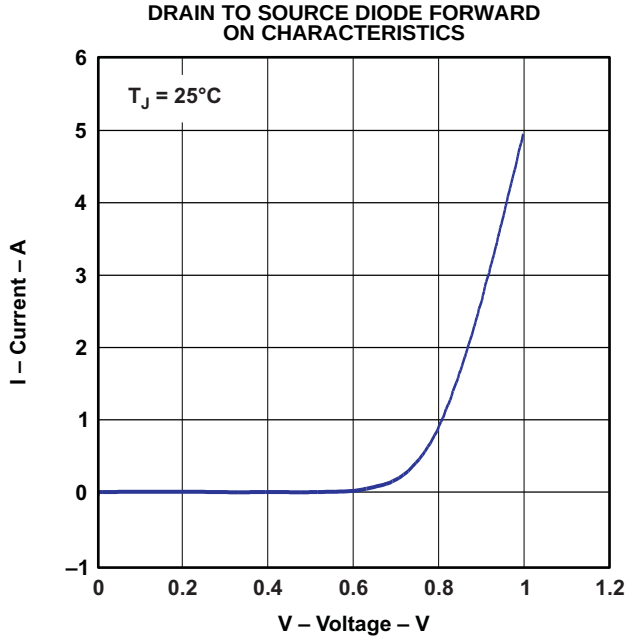


Figure 4.

TYPICAL CHARACTERISTICS (continued)

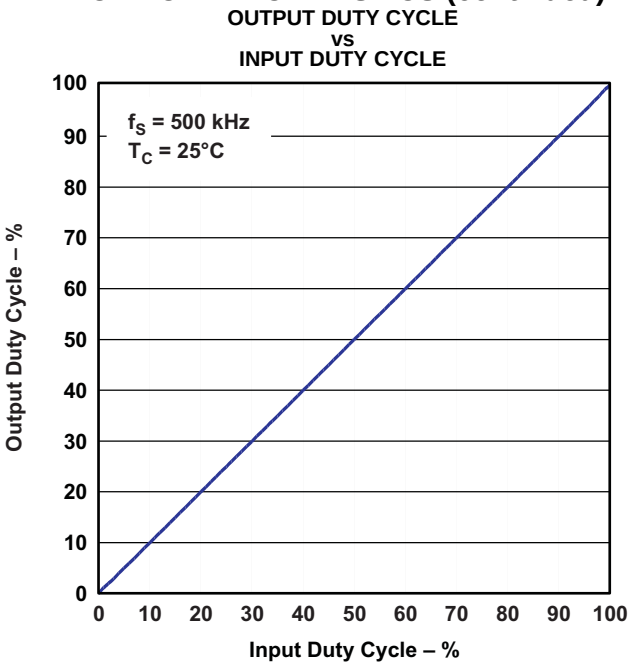


Figure 5.

THEORY OF OPERATION

POWER SUPPLIES

To facilitate system design, the DRV8312/32 need only a 12-V supply in addition to H-Bridge power supply (PVDD). An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, the high-side gate drive requiring a floating voltage supply, which is accommodated by built-in bootstrap circuitry requiring external bootstrap capacitor.

To provide symmetrical electrical characteristics, the PWM signal path, including gate drive and output stage, is designed as identical, independent half-bridges. For this reason, each half-bridge has a separate gate drive supply (GVDD_X), a bootstrap pin (BST_X), and a power-stage supply pin (PVDD_X). Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Special attention should be paid to place all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. Furthermore, decoupling capacitors need a short ground path back to the device.

For a properly functioning bootstrap circuit, a small ceramic capacitor (an X5R or better) must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 10 kHz to 500 kHz, the use of 100-nF ceramic capacitors (X5R or better), size 0603 or 0805, is recommended for the bootstrap supply. These 100-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET fully turned on during the remaining part of the PWM cycle. In an application running at a switching frequency lower than 10 kHz, the bootstrap capacitor might need to be increased in value.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pin (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a ceramic capacitor (X5R or better) placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the DRV8312/32 EVM board.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 50-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the DRV8312/32 are fully protected against erroneous power-stage turn-on due to parasitic gate charging. Thus, voltage-supply ramp rates (dv/dt) are non-critical within the specified voltage range (see the *Recommended Operating Conditions* section of this data sheet).

SYSTEM POWER-UP/POWER-DOWN SEQUENCE

Powering Up

The DRV8312/32 do not require a power-up sequence. The outputs of the H-bridges remain in a high impedance state until the gate-drive supply voltage GVDD_X and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, holding RESET_A, RESET_B, and RESET_C in a low state while powering up the device is recommended. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

Powering Down

The DRV8312/32 do not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the UVP voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is a good practice to hold RESET_A, RESET_B and RESET_C low during power down to prevent any unknown state during this transition.

ERROR REPORTING

The $\overline{\text{FAULT}}$ and $\overline{\text{OTW}}$ pins are both active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown, such as overtemperatue shut down, overcurrent shut-down, or undervoltage protection, is signaled by the $\overline{\text{FAULT}}$ pin going low. Likewise, $\overline{\text{OTW}}$ goes low when the device junction temperature exceeds 125°C (see Table 1).

Table 1. Protection Mode Signal Descriptions

$\overline{\text{FAULT}}$	$\overline{\text{OTW}}$	DESCRIPTION
0	0	Overtemperature warning and (overtemperature shut down or overcurrent shut down or undervoltage protection) occurred
0	1	Overcurrent shut-down or GVDD undervoltage protection occurred
1	0	Overtemperature warning
1	1	Device under normal operation

TI recommends monitoring the $\overline{\text{OTW}}$ signal using the system microcontroller and responding to an $\overline{\text{OTW}}$ signal by reducing the load current to prevent further heating of the device resulting in device overtemperature shutdown (OTSD).

To reduce external component count, an internal pullup resistor to internal VREG (3.3 V) is provided on both $\overline{\text{FAULT}}$ and $\overline{\text{OTW}}$ outputs. Level compliance for 5-V logic can be obtained by adding external pull-up resistors to 5 V (see the *Electrical Characteristics* section of this data sheet for further specifications).

DEVICE PROTECTION SYSTEM

The DRV8312/32 contain advanced protection circuits carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overcurrent, overtemperature, and undervoltage. The DRV8312/32 respond to a fault by immediately setting the half bridge outputs in a high-impedance (Hi-Z) state and asserting the $\overline{\text{FAULT}}$ pin low. In situations other than overcurrent or overtemperature, the device automatically recovers when the fault condition has been removed or the gate supply voltage has increased. For highest possible reliability, reset the device externally no sooner than 1 second after the shutdown when recovering from an overcurrent shut down (OCSD) or OTSD fault.

Bootstrap Capacitor Under Voltage Protection

When the device runs at a low switching frequency (e.g. less than 10 kHz with a 100-nF bootstrap capacitor), the bootstrap capacitor voltage might not be able to maintain a proper voltage level for the high-side gate driver. A bootstrap capacitor undervoltage protection circuit (BST_UVP) will prevent potential failure of the high-side MOSFET. When the voltage on the bootstrap capacitors is less than the required value for safe operation, the DRV8312/32 will initiate bootstrap capacitor recharge sequences (turn off high side FET for a short period) until the bootstrap capacitors are properly charged for safe operation. This function may also be activated when PWM duty cycle is too high (e.g. less than 20 ns off time at 10 kHz). Note that bootstrap capacitor might not be able to be charged if no load or extremely light load is presented at output during BST_UVP operation, so it is recommended to turn on the low side FET for at least 50 ns for each PWM cycle to avoid BST_UVP operation if possible.

For applications with lower than 10 kHz switching frequency and not to trigger BST_UVP protection, a larger bootstrap capacitor can be used (e.g., 1 uF cap for 800 Hz operation). When using a bootstrap cap larger than 220 nF, it is recommended to add 5 ohm resistors between 12V GVDD power supply and GVDD_X pins to limit the inrush current on the internal bootstrap diodes.

Overcurrent (OC) Protection

The DRV8312/32 have independent, fast-reacting current detectors with programmable trip threshold (OC threshold) on all high-side and low-side power-stage FETs. There are two settings for OC protection through mode selection pins: cycle-by-cycle (CBC) current limiting mode and OC latching (OCL) shut down mode.

In CBC current limiting mode, the detector outputs are monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current from further increasing, i.e., it performs a CBC current-limiting function rather than prematurely shutting down the device. This feature can effectively limit the inrush current during motor start-up or transient without damaging the device. During short to power and short to ground conditions, since the current limit circuitry might not be able to control the current to a proper level, a second protection system triggers a latching shutdown, resulting in the related half bridge being set in the high-impedance (Hi-Z) state. Current limiting and overcurrent protection are independent for half-bridges A, B, and C, respectively.

Figure 6 illustrates cycle-by-cycle operation with high side OC event and Figure 7 shows cycle-by-cycle operation with low side OC. Dashed lines are the operation waveforms when no CBC event is triggered and solide lines show the waveforms when CBC event is triggered. In CBC current limiting mode, when low side FET OC is detected, the device will turn off the affected low side FET and keep the high side FET at the same half bridge off until next PWM cycle; when high side FET OC is detected, the device will turn off the affected high side FET and turn on the low side FET at the half bridge until next PWM cycle.

It is important to note that if the input to a half bridge is held to a constant value when an over current event occurs in CBC, then the associated half bridge will be in a HI-Z state upon the over current event ending. Cycling IN_X will allow OUT_X to resume normal operation.

In OC latching shut down mode, the CBC current limit and error recovery circuits are disabled and an overcurrent condition will cause the device to shutdown. After shutdown, RESET_A, RESET_B, and RESET_C must be asserted to restore normal operation after the overcurrent condition is removed.

For added flexibility, the OC threshold is programmable using a single external resistor connected between the OC_ADJ pin and AGND pin. See Table 2 for information on the correlation between programming-resistor value and the OC threshold.

The values in Table 2 show typical OC thresholds for a given resistor. Assuming a fixed resistance on the OC_ADJ pin across multiple devices, a 20% device-to-device variation in OC threshold measurements is possible. Therefore, this feature is designed for system protection and not for precise current control.

Table 2. Programming-Resistor Values and OC Threshold

OC-ADJUST RESISTOR VALUES (kΩ)	MAXIMUM CURRENT BEFORE OC OCCURS (A)
19 (1)	13.2
22	11.6
24	10.7
27	9.7
30	8.8
36	7.4
39	6.9
43	6.3
47	5.8
56	4.9
68	4.1
82	3.4
100	2.8
120	2.4
150	1.9
200	1.4

(1) Recommended to use in OC Latching Mode Only

It should be noted that a properly functioning overcurrent detector assumes the presence of a proper inductor or power ferrite bead at the power-stage output. Short-circuit protection is not ensured with a direct short at the output pins of the power stage.

Overtemperature Protection

The DRV8312/32 have a two-level temperature-protection system that asserts an active-low warning signal (OTW) when the device junction temperature exceeds 125°C (nominal) and, if the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and FAULT being asserted low. OTSD is latched in this case and RESET_A, RESET_B, and RESET_C must be asserted low to clear the latch.

Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the DRV8312/32 fully protect the device in any power-up / down and brownout situation. While powering up, the POR circuit resets the overcurrent circuit and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach 9.8 V (typical). Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and FAULT being asserted low. The device automatically resumes operation when all supply voltage on the bootstrap capacitors have increased above the UVP threshold.

DEVICE RESET

Three reset pins are provided for independent control of half-bridges A, B, and C. When RESET_X is asserted low, two power-stage FETs in half-bridges X are forced into a high-impedance (Hi-Z) state.

A rising-edge transition on reset input allows the device to resume operation after a shut-down fault. That is, when half-bridge X has OC shutdown in CBC mode, a low to high transition of RESET_X pin will clear the fault and FAULT pin. When an OTSD or OC shutdown in Latching mode occurs, all three RESET_A, RESET_B, and RESET_C need to have a low to high transition to clear the fault and reset FAULT signal.

DIFFERENT OPERATIONAL MODES

The DRV8312/32 support two different modes of operation:

1. Three-phase (3PH) or three half bridges (HB) with CBC current limit
2. Three-phase or three half bridges with OC latching shutdown (no CBC current limit)

Because each half bridge has independent supply and ground pins, a shunt sensing resistor can be inserted between PVDD to PVDD_X or GND_X to GND (ground plane). A high side shunt resistor between PVDD and PVDD_X is recommended for differential current sensing because a high bias voltage on the low side sensing could affect device operation. If low side sensing has to be used, a shunt resistor value of 10 mΩ or less or sense voltage 100 mV or less is recommended.

Figure 8 and Figure 9 show the three-phase application examples, and Figure 10 shows how to connect to DRV8312/32 with some simple logic to accommodate conventional 6 PWM inputs control.

We recommend using a complementary control scheme for switching phases to prevent circulated energy flowing inside the phases and to make current limiting feature active all the time. Complementary control scheme also forces the current flowing through sense resistors all the time to have a better current sensing and control of the system.

Figure 11 shows six steps trapezoidal scheme with hall sensor control and Figure 12 shows six steps trapezoidal scheme with sensorless control. The hall sensor sequence in real application might be different than the one we showed in Figure 11 depending on the motor used. Please check motor manufacture datasheet for the right sequence in applications. In six step trapezoidal complementary control scheme, a half bridge with larger than 50% duty cycle will have a positive current and a half bridge with less than 50% duty cycle will have a negative current. For normal operation, changing PWM duty cycle from 50% to 100% will adjust the current from 0 to maximum value with six steps control. It is recommanded to apply a minimum 50ns to 100 ns PWM pulse at each switching cycle at lower side to properly charge the bootstrap cap. The impact of minimum pulse at low side FET is pretty small, e.g., the maximum duty cycle is 99.9% with 100ns minimum pulse on low side. RESET_Xpin can be used to get channel X into high impedance mode. If you prefer PWM switching one channel but hold low side FET of the other channel on (and third channel in Hi-Z) for 2-quadrant mode, OT latching shutdown mode is recommended to prevent the channel with low side FET on stuck in Hi-Z during OC event in CBC mode.

The DRV8312/32 can also be used for sinusoidal waveform control and field oriented control. Please check TI website MCU motor control library for control algorithms.

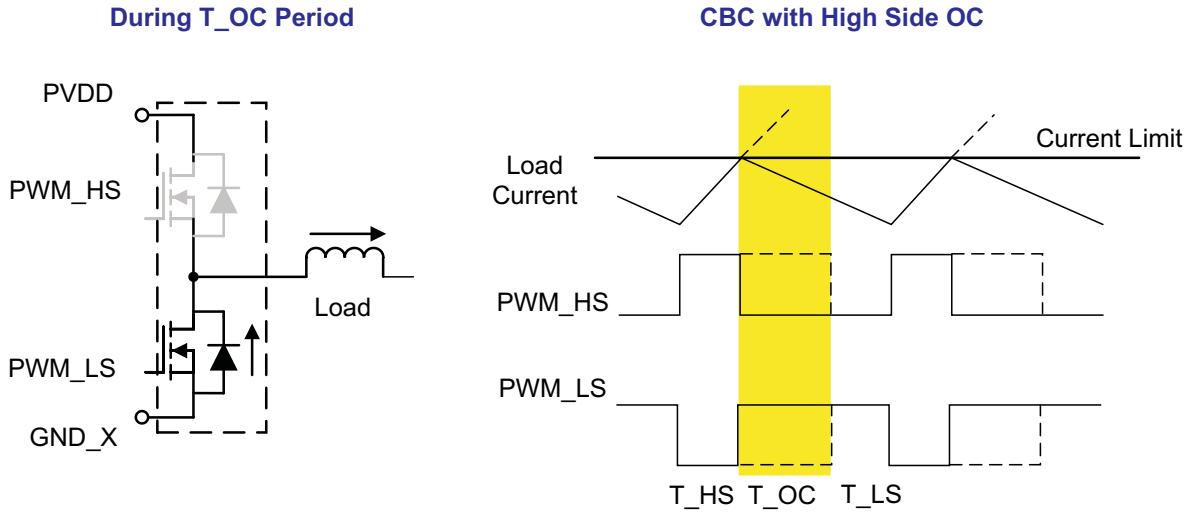


Figure 6. Cycle-by-Cycle Operation with High Side OC (dashed line: normal operation; solid line: CBC event)

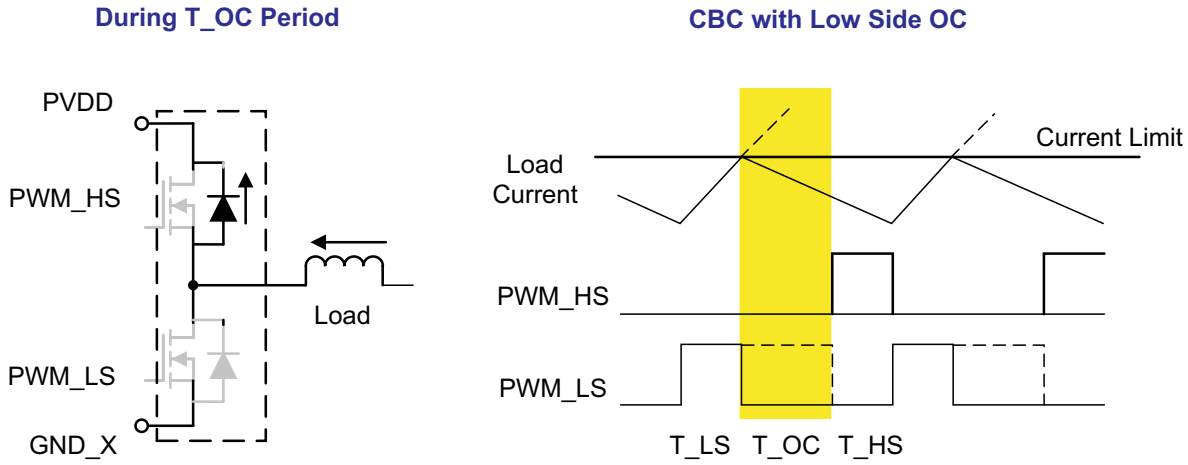


Figure 7. Cycle-by-Cycle Operation with Low Side OC (dashed line: normal operation; solid line: CBC event)

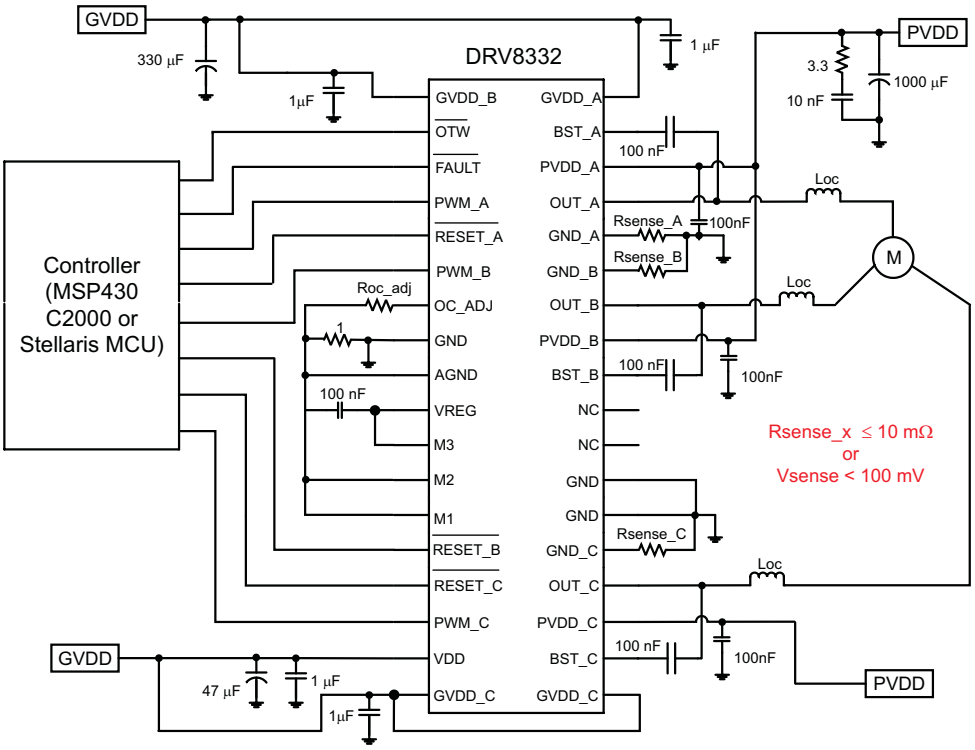


Figure 8. DRV8332 Application Diagram for Three-Phase Operation

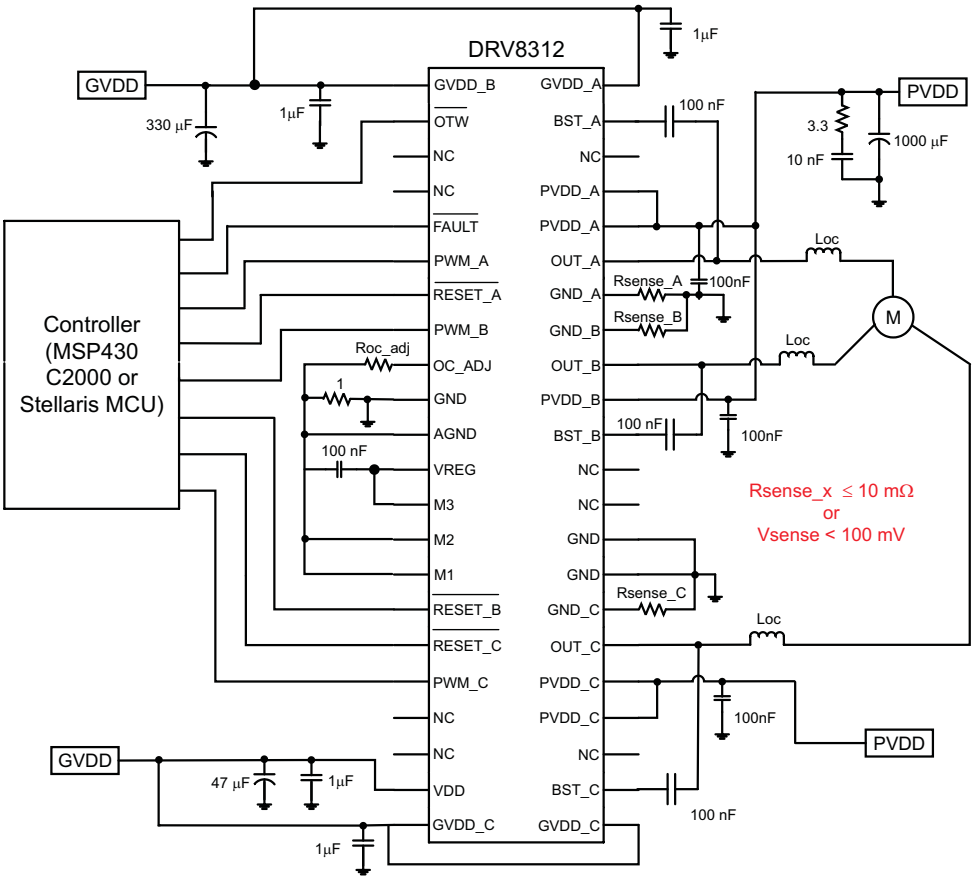


Figure 9. DRV8312 Application Diagram for Three-Phase Operation

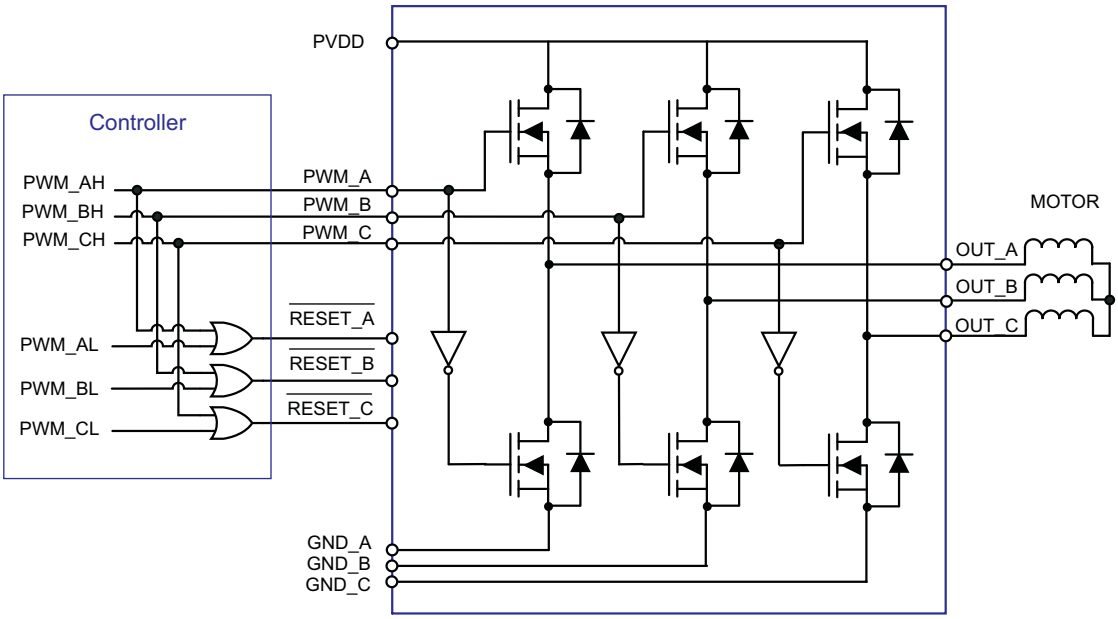


Figure 10. Control Signal Logic with Conventional 6 PWM Input Scheme

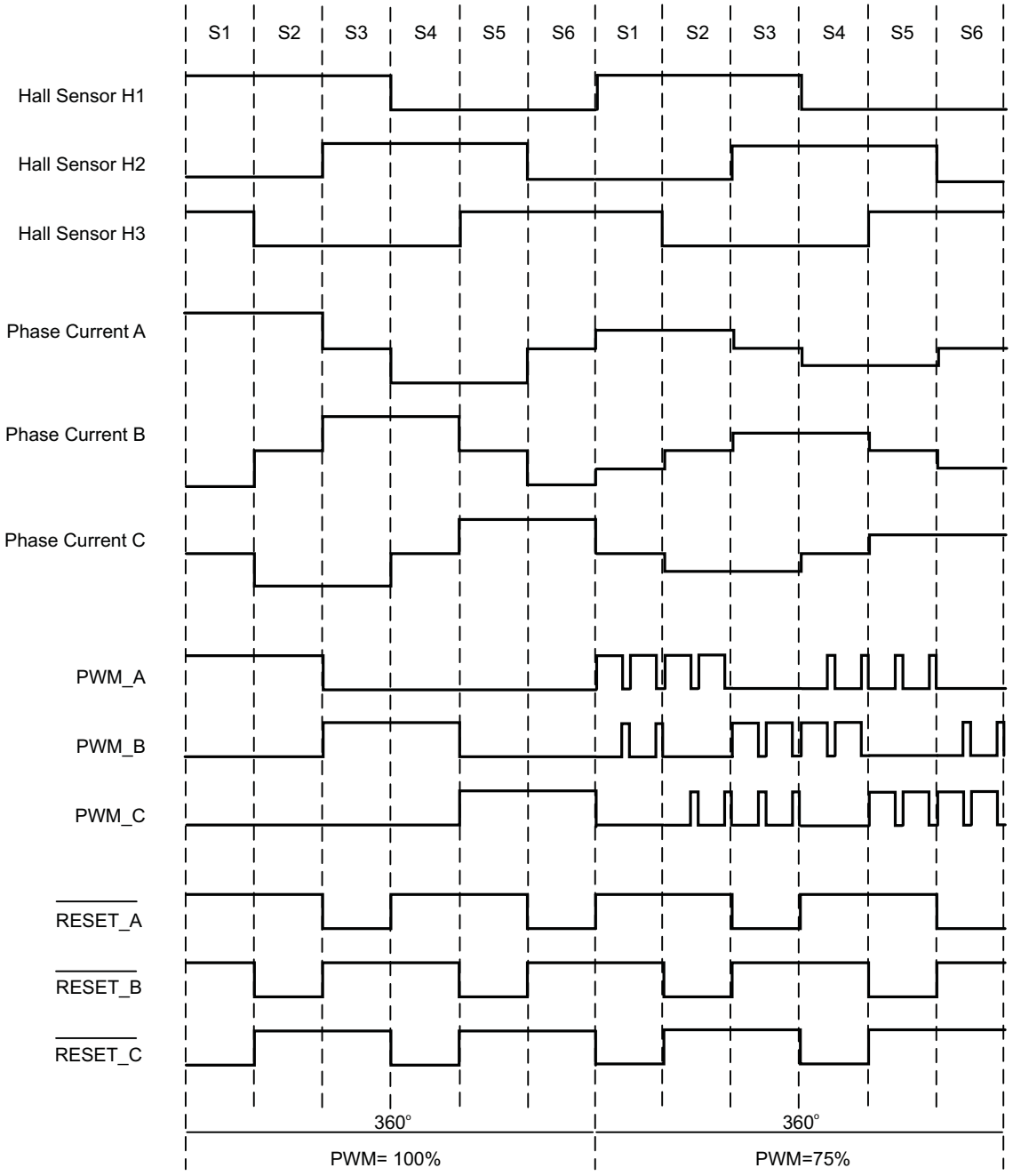


Figure 11. Hall Sensor Control with 6 Steps Trapezoidal Scheme

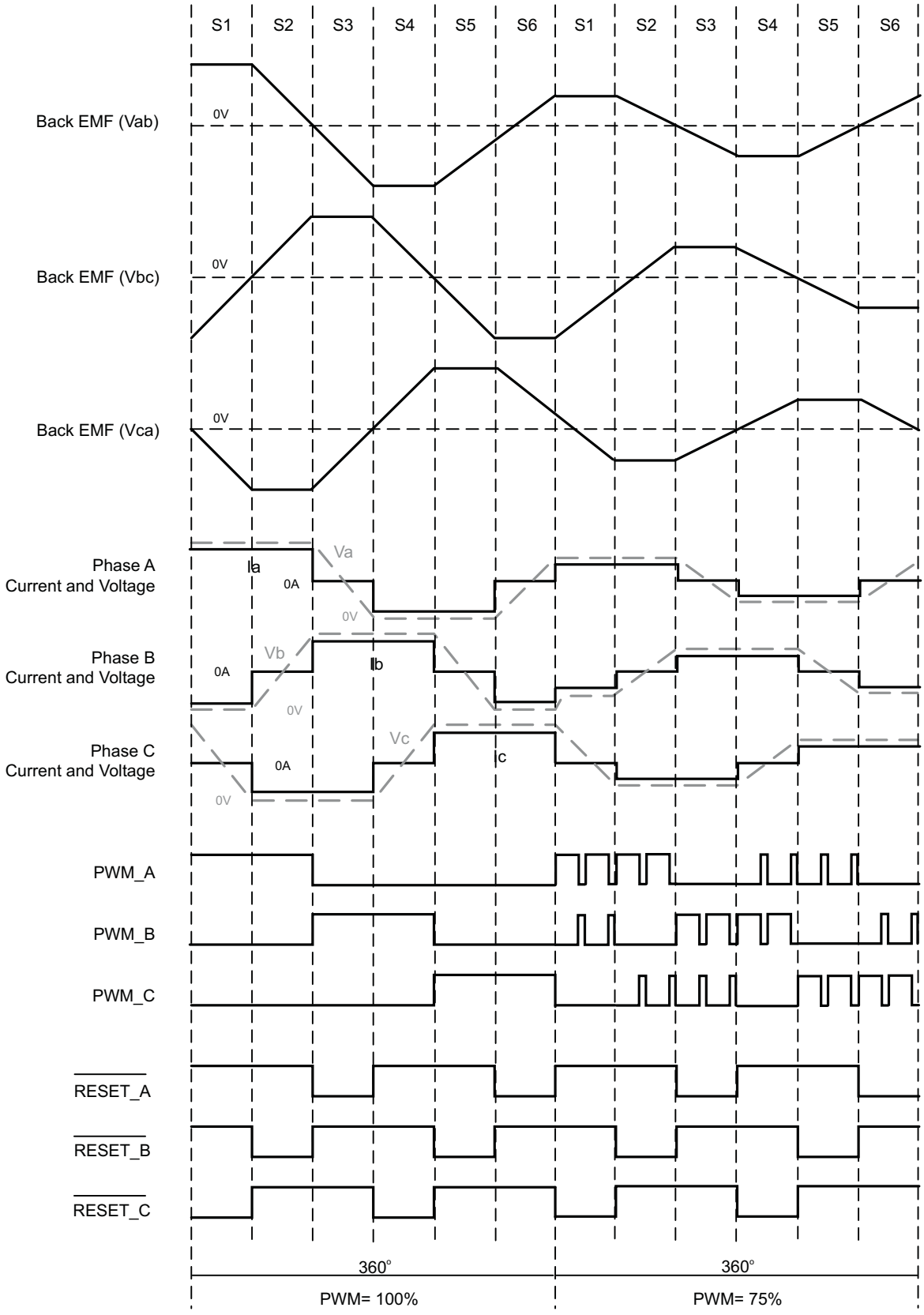


Figure 12. Sensorless Control with 6 Steps Trapezoidal Scheme

APPLICATION INFORMATION

SYSTEM DESIGN RECOMMENDATIONS

Voltage of Decoupling Capacitor

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. The high frequency decoupling capacitor should use ceramic capacitor with X5R or better rating. For a 50-V application, a minimum voltage rating of 63 V is recommended.

Current Requirement of 12V Power Supply

The DRV8312/32 require a 12V power supply for GVDD and VDD pins. The total supply current is pretty low at room temp (less than 50mA), but the current could increase significantly when the device temperature goes too high (e.g. above 125°C), especially at heave load conditions due to substrate current collection by 12V guard rings. So it is recommended to design the 12V power supply with current capability at least 5-10% of your load current and no less than 100mA to assure the device performance across all temperature range.

VREG Pin

The VREG pin is used for internal logic and should not be used as a voltage source for external circuitries. The capacitor on VREG pin should be connected to AGND.

VDD Pin

The transient current in VDD pin could be significantly higher than average current through VDD pin. A low resistive path to GVDD should be used. A 22-µF to 47-µF capacitor should be placed on VDD pin beside the 100-nF to 1-µF decoupling capacitor to provide a constant voltage during transient.

OTW Pin

$\overline{\text{OTW}}$ reporting indicates the device approaching high junction temperature. This signal can be used with MCU to decrease system power when $\overline{\text{OTW}}$ is low in order to prevent OT shut down at a higher temperature.

No external pull up resistor or 3.3V power supply is needed for 3.3V logic. The $\overline{\text{OTW}}$ pin has an internal pullup resistor connecting to an internal 3.3V to reduce external component count. For 5V logic, an external pull up resistor to 5V is needed.

FAULT Pin

The $\overline{\text{FAULT}}$ pin reports any fault condition resulting in device shut down. No external pull up resistor or 3.3V power supply is needed for 3.3V logic. The $\overline{\text{FAULT}}$ pin has an internal pullup resistor connecting to an internal 3.3V to reduce external component count. For 5V logic, an external pull upresistor to 5V is needed.

OC_ADJ Pin

For accurate control of the overcurrent protection, the OC_ADJ pin has to be connected to AGND through an OC adjust resistor.

PWM_X and RESET_X Pins

It is recommanded to connect these pins to either AGND or GND when they are not used, and these pins only support 3.3V logic.

Mode Select Pins

Mode select pins (M1, M2, and M3) should be connected to either VREG (for logic high) or AGND for logic low. It is not recommended to connect mode pins to board ground if 1-Ω resistor is used between AGND and GND.

Output Inductor Selection

For normal operation, inductance in motor (assume larger than 10 µH) is sufficient to provide low di/dt output (e.g. for EMI) and proper protection during overload condition (CBC current limiting feature). So no additional output inductors are needed during normal operation.

However during a short condition, the motor (or other load) could be shorted, so the load inductance might not present in the system anymore; the current in short condition can reach such a high level that may exceed the abs max current rating due to extremely low impendence in the short circuit path and high di/dt before oc detection circuit kicks in. So a ferrite bead or inductor is recommended to utilize the short circuit protection feature in DRV8312/32. With an external inductor or ferrite bead, the current will rise at a much slower rate and reach a lower current level before oc protection starts. The device will then either operate CBC current limit or OC shut down automatically (when current is well above the current limit threshold) to protect the system.

For a system that has limited space, a power ferrite bead can be used instead of an inductor. The current rating of ferrite bead has to be higher than the RMS current of the system at normal operation. A ferrite bead designed for very high frequency is NOT recommended. A minimum impedance of 10 Ω or higher is recommended at 10 MHz or lower frequency to effectively limit the current rising rate during short circuit condition.

The TDK MPZ2012S300A and MPZ2012S101A (with size of 0805 inch type) have been tested in our system to meet short circuit conditions in the DRV8312. But other ferrite beads that have similar frequency characteristics can be used as well.

For higher power applications, such as in the DRV8332, there might be limited options to select suitable ferrite bead with high current rating. If an adequate ferrite bead cannot be found, an inductor can be used.

The inductance can be calculated as:

$$Loc\_\min = \frac{PVDD \cdot Toc\_delay}{Ipeak - Iave} \quad (1)$$

Where Toc_delay = 250 nS, Ipeak = 15 A (below abs max rating).

Because an inductor usually saturates pretty quickly after reaching its current rating, it is recommended to use an inductor with a doubled value or an inductor with a current rating well above the operating condition.

PCB LAYOUT RECOMMENDATION

PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. copper on both top and bottom layer is recommended for improved thermal performance (better heat sinking) and less noise susceptibility (lower PCB trace inductance).

Ground Plane

Because of the power level of these devices, it is recommended to use a big unbroken single ground plane for the whole system / board. The ground plane can be easily made at bottom PCB layer. In order to minimize the impedance and inductance of ground traces, the traces from ground pins should keep as short and wide as possible before connected to bottom ground plane through vias. Multiple vias are suggested to reduce the impedance of vias. Try to clear the space around the device as much as possible especially at bottom PCB side to improve the heat spreading.

Decoupling Capacitor

High frequency decoupling capacitors (100 nF) should be placed close to PVDD_X pins and with a short ground return path to minimize the inductance on the PCB trace.

AGND

AGND is a localized internal ground for logic signals. A 1-Ω resistor is recommended to be connected between GND and AGND to isolate the noise from board ground to AGND. There are other two components are connected to this local ground: 0.1-µF capacitor between VREG to AGND and Roc_adj resistor between OC_ADJ and AGND. Capacitor for VREG should be placed close to VREG and AGND pins and connected without vias.

Current Shunt Resistor

If current shunt resistor is connected between GND_X to GND or PVDD_X to PVDD, make sure there is only one single path to connect each GND_X or PVDD_X pin to shunt resistor, and the path is short and symmetrical on each sense path to minimize the measurement error due to additional resistance on the trace.

PCB LAYOUT EXAMPLE

An example of the schematic and PCB layout of DRV8312 are shown in Figure 13, Figure 14, and Figure 15.

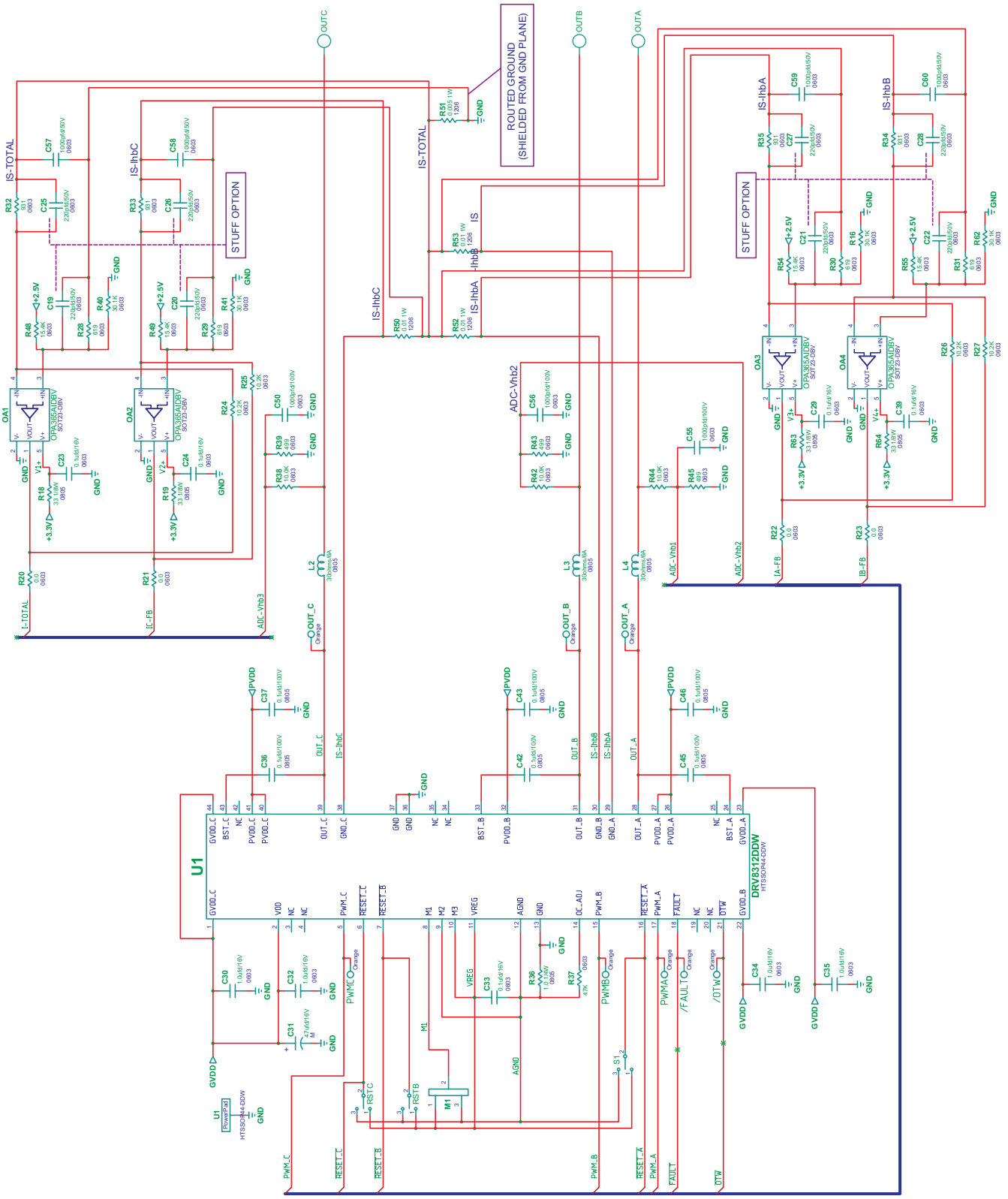
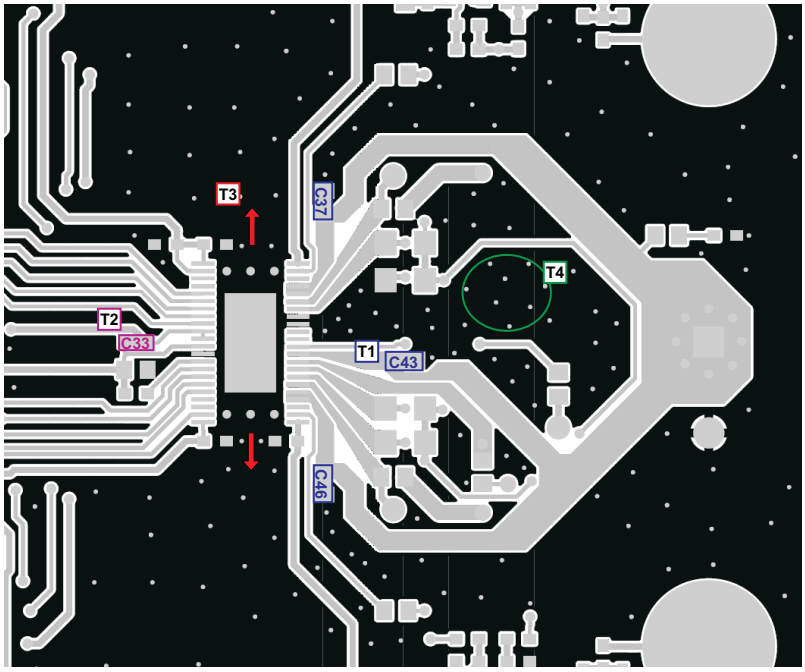


Figure 13. DRV8312 Schematic Example



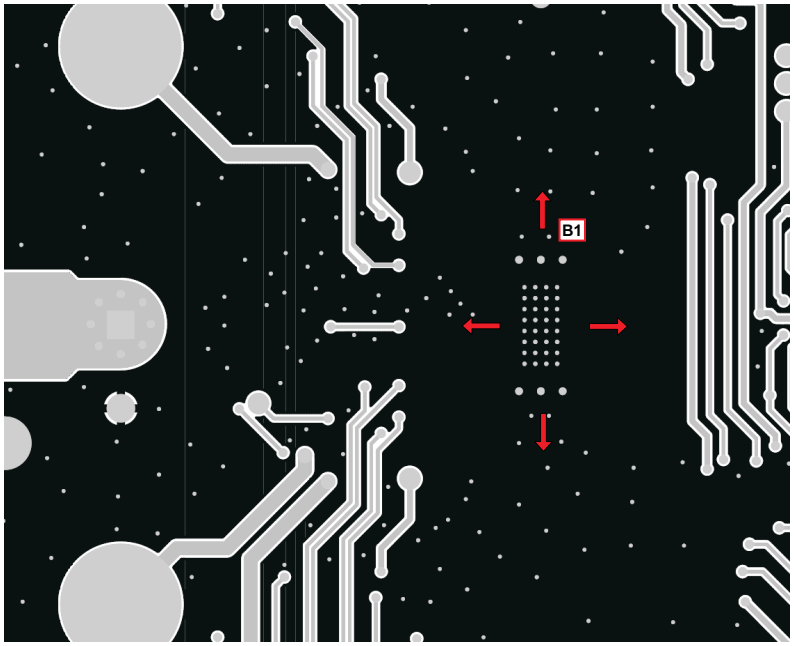
T1: PVDD decoupling capacitors C37, C43, and C46 should be placed very close to PVDD_X pins and ground return path.

T2: VREG decoupling capacitor C33 should be placed very close to VREG abd AGND pins.

T3: Clear the space above and below the device as much as possible to improve the thermal spreading.

T4: Add many vias to reduce the impedance of ground path through top to bottom side. Make traces as wide as possible for ground path such as GND_X path.

Figure 14. Printed Circuit Board – Top Layer



B1: Do not block the heat transfer path at bottom side. Clear as much space as possible for better heat spreading.

Figure 15. Printed Circuit Board – Bottom Layer

THERMAL INFORMATION

The thermally enhanced package provided with the DRV8332 is designed to interface directly to heat sink using a thermal interface compound in between, (e.g., Ceramique from Arctic Silver, TIMTronics 413, etc.). The heat sink then absorbs heat from the ICs and couples it to the local air. It is also a good practice to connect the heatsink to system ground on the PCB board to reduce the ground noise.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this example the power pad or heat slug)
- Thermal grease thermal resistance
- Heat sink thermal resistance

The thermal grease thermal resistance can be calculated from the exposed power pad or heat slug area and the thermal grease manufacturer's area thermal resistance (expressed in °C-in ^{2}/W or °C-mm^2/W). The approximate exposed heat slug size is as follows:

- DRV8332, 36-pin PSOP3 …… 0.124 in^2 (80 mm ^{2})

The thermal resistance of a thermal pad is considered higher than a thin thermal grease layer and is not recommended. Thermal tape has an even higher thermal resistance and should not be used at all. Heat sink thermal resistance is predicted by the heat sink vendor, modeled using a continuous flow dynamics (CFD) model, or measured.

Thus the system $R_{\theta JA} = R_{\theta JC}$ + thermal grease resistance + heat sink resistance.

See the TI application report, *IC Package Thermal Metrics* (SPRA953A), for more thermal information.

DRV8312 Thermal Via Design Recommendation

Thermal pad of the DRV8312 is attached at bottom of device to improve the thermal capability of the device. The thermal pad has to be soldered with a very good coverage on PCB in order to deliver the power specified in the datasheet. The figure below shows the recommended thermal via and land pattern design for the DRV8312. For additional information, see TI application report, PowerPad Made Easy (SLMA004B) and PowerPad Layout Guidelines (SOLA120).

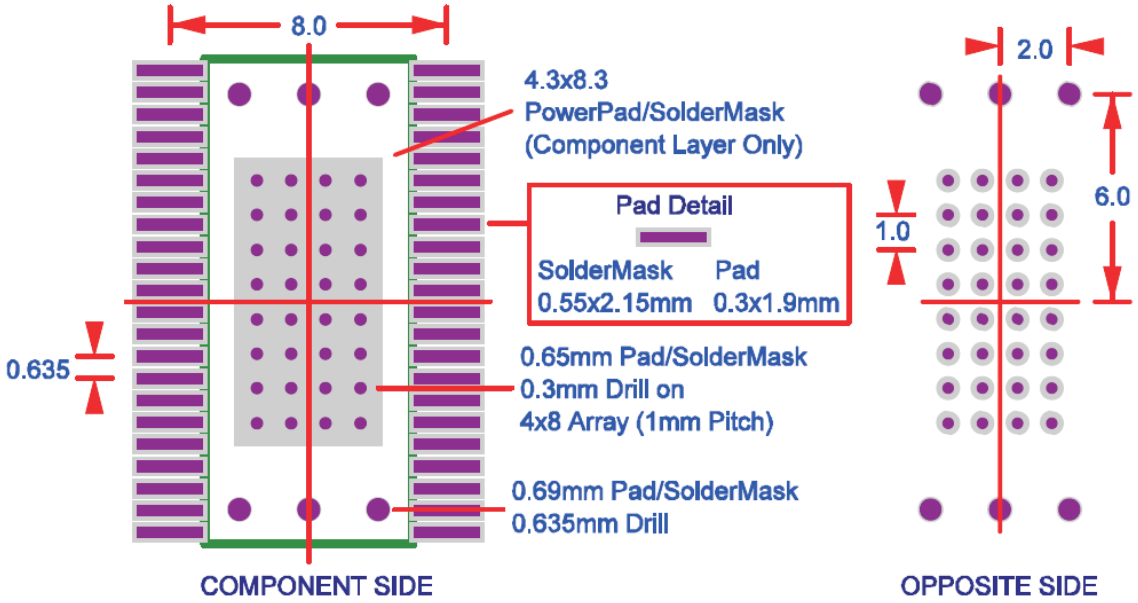


Figure 16. DRV8312 Thermal Via Footprint

REVISION HISTORY

Changes from Original (May 2010) to Revision A **Page**

- Changed text in the OC_ADJ Pin section From: "For accurate control of the oevercurrent protection..." To: "For accurate control of the overcurrent protection..." 19

Changes from Revision A (July 2013) to Revision B **Page**

- Changed the description of pin M3 From: AGND connection is recommended To: VREG connection is recommended 4

Changes from Revision B (September 2013) to Revision C **Page**

- Changed text in the Overcurrent (OC) Protection section From: "cause the device to shutdown immediately." To: "cause the device to shutdown." 12
- Changed text in the Overcurrent (OC) Protection section From: "$\overline{\text{RESET\_B}}$, and / or $\overline{\text{RESET\_C}}$ must be asserted." To: "$\overline{\text{RESET\_B}}$, and $\overline{\text{RESET\_C}}$ must be asserted" 12
- Changed paragraph in the DEVICE RESET "A rising-edge transition..." 13

Changes from Revision C (October 2013) to Revision D **Page**

- Added the THERMAL INFORMATION table 2
- Changed the t_{ON_MIN} description to include "for charging the Bootstrap capacitor" 3
- Changed GND_A, GND_B, and GND_C pins description to remove text "requires close decoupling capacitor to ground" 4
- Changed M2 pin description From: Mode selection pin 4
- Added text to the Overcurrent (OC) Protection section - "It is important to note..." 12
- Added text to the Overcurrent (OC) Protection section - "The values in Table 2 show typical..." 12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8312DDW	ACTIVE	HTSSOP	DDW	44	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8312	Samples
DRV8312DDWR	ACTIVE	HTSSOP	DDW	44	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8312	Samples
DRV8332DKD	ACTIVE	HSSOP	DKD	36	29	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 85	DRV8332	Samples
DRV8332DKDR	ACTIVE	HSSOP	DKD	36	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 85	DRV8332	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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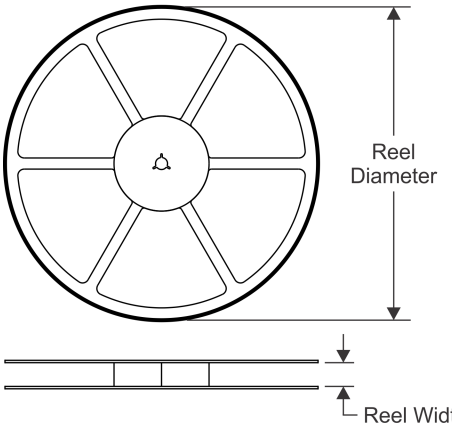
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DRV8332 :

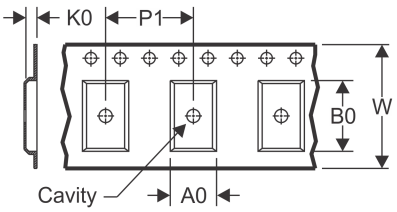
NOTE: Qualified Version Definitions:

TAPE AND REEL INFORMATION

REEL DIMENSIONS

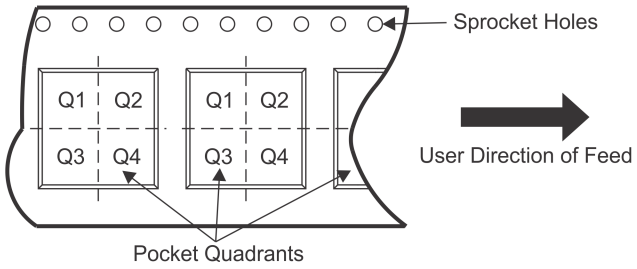


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

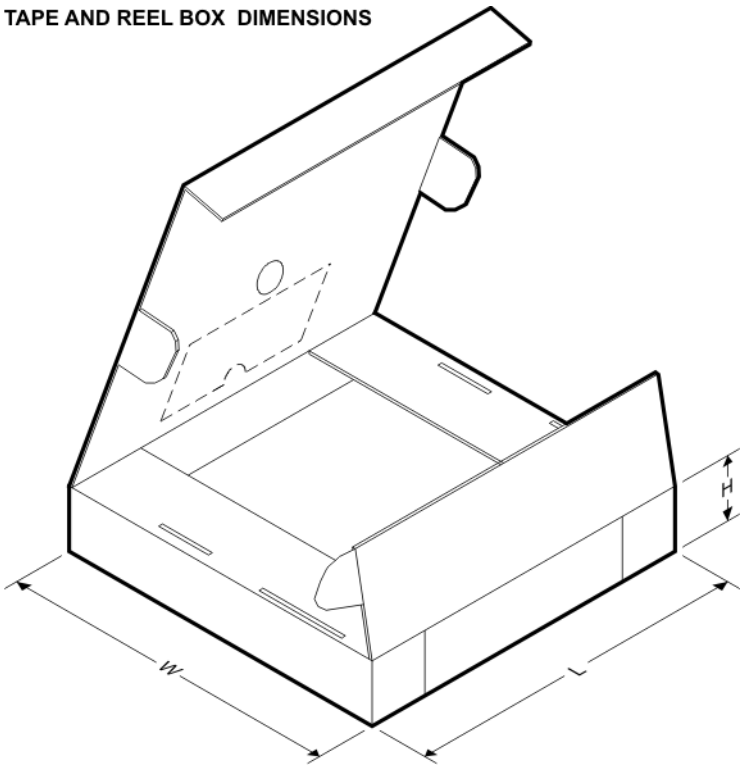
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8312DDWR	HTSSOP	DDW	44	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
DRV8332DKDR	HSSOP	DKD	36	500	330.0	24.4	14.7	16.4	4.0	20.0	24.0	Q1

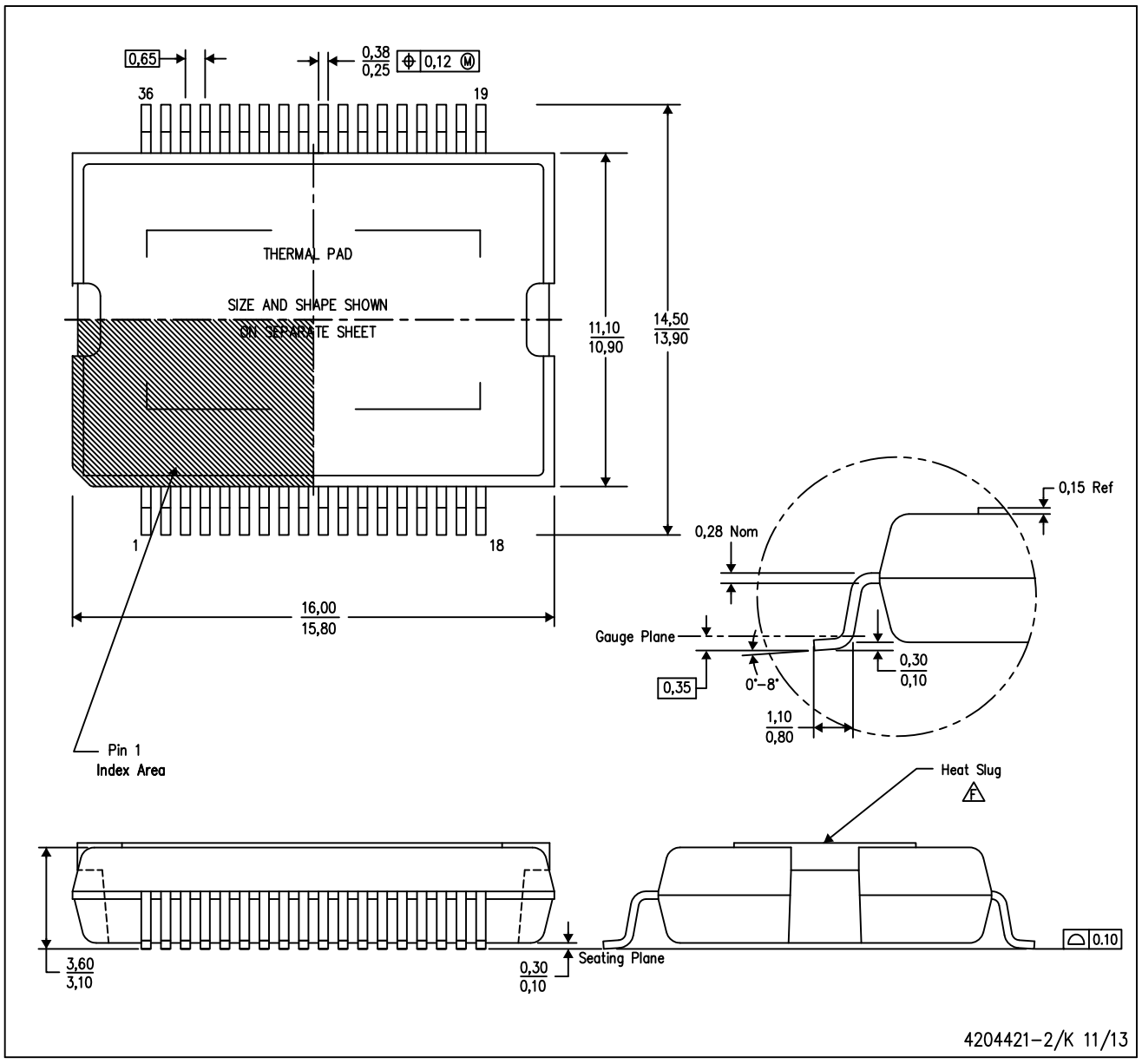
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8312DDWR	HTSSOP	DDW	44	2000	367.0	367.0	45.0
DRV8332DKDR	HSSOP	DKD	36	500	367.0	367.0	45.0

DKD (R–PDSO–G36) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15mm.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. The package thermal performance is optimized for conductive cooling with attachment to an external heat sink.

PowerPAD is a trademark of Texas Instruments.

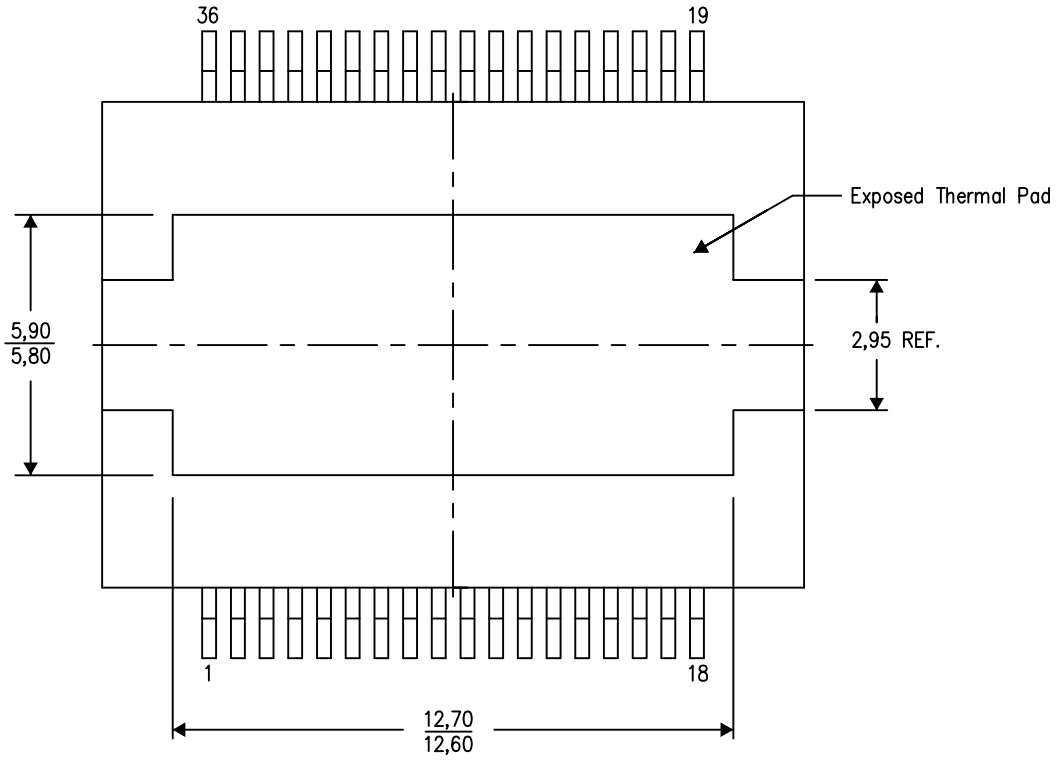
DKD (R–PDSO–G36) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

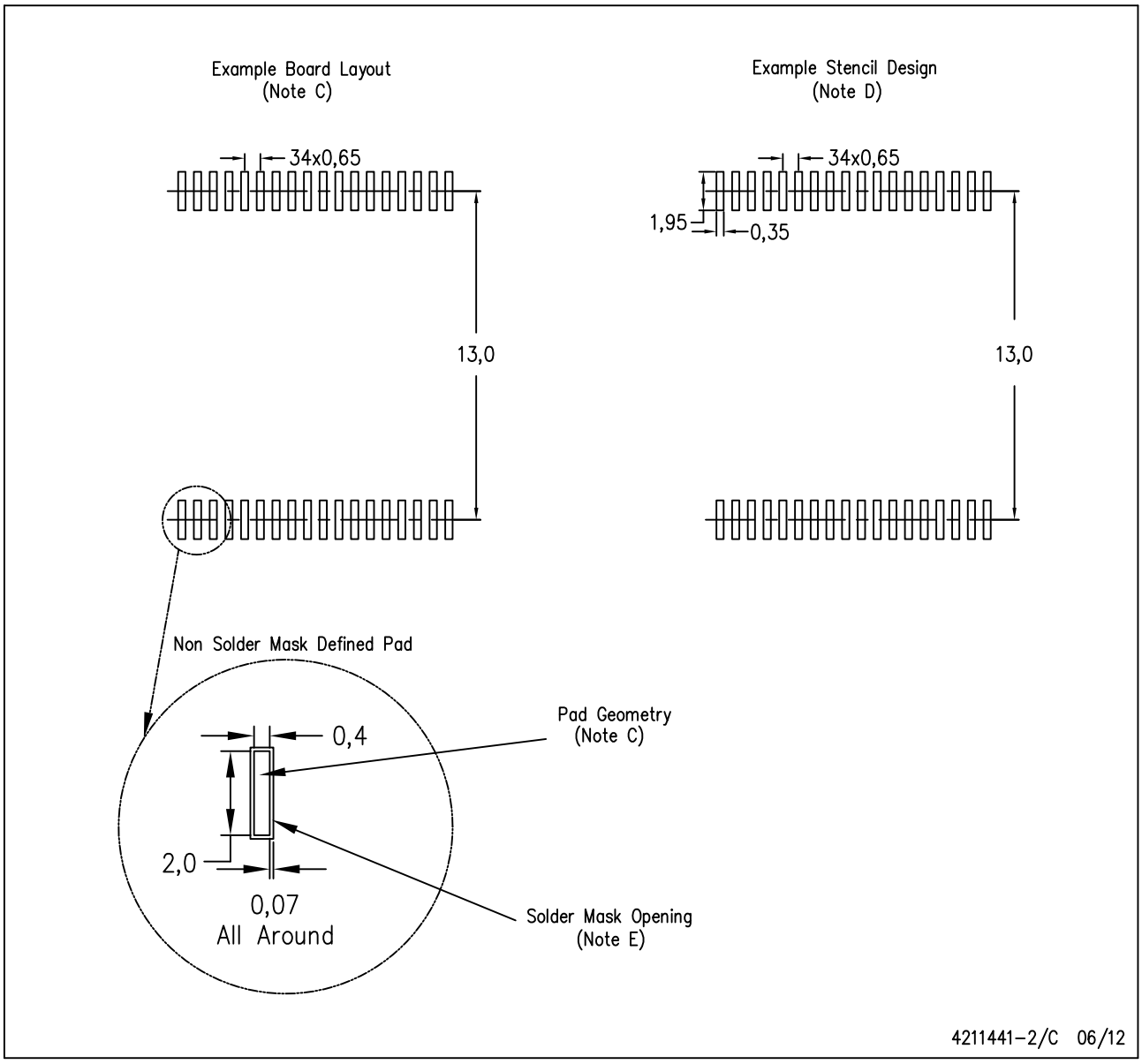
Top View

Exposed Thermal Pad Dimensions

4210894–2/E 06/12

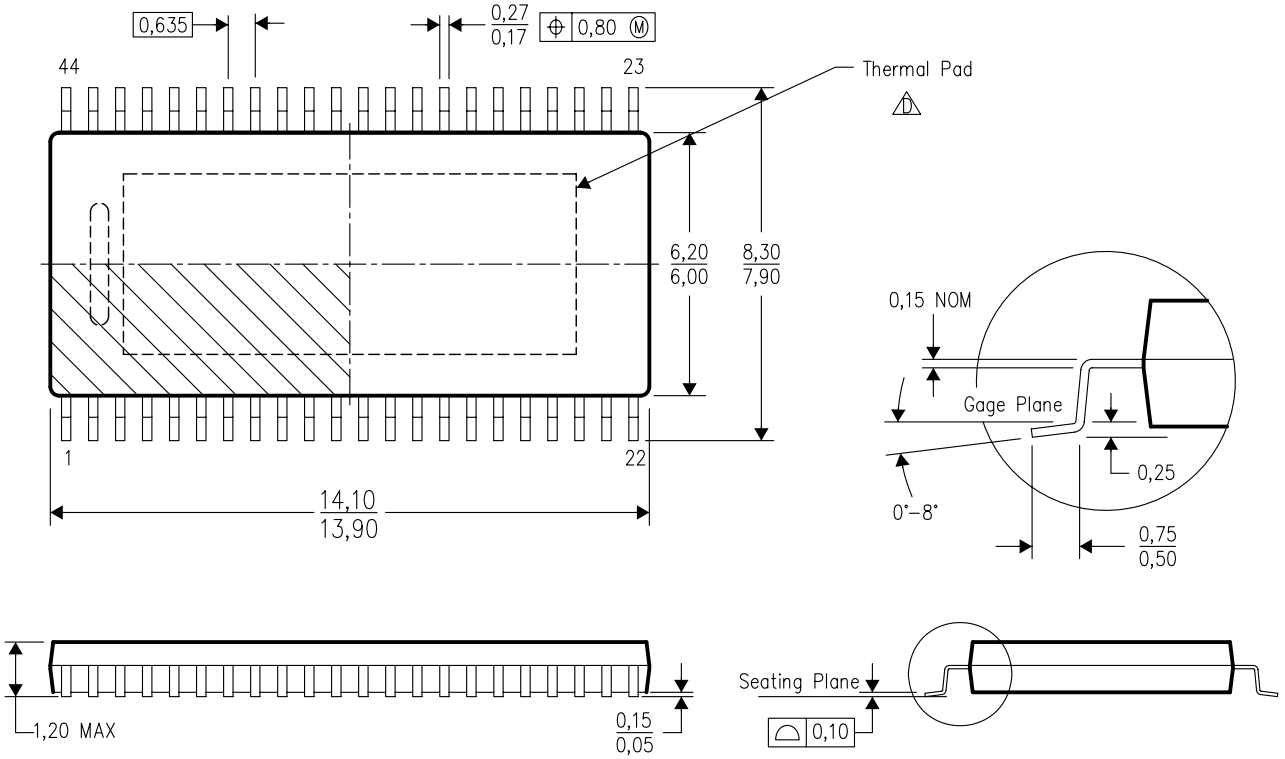
NOTE: All linear dimensions are in millimeters

DKD (R–PDSO–G36) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DDW (R–PDSO–G44) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE (PAD DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package thermal performance is optimized for conductive cooling with attachment to an external heat sink. See the product data sheet for details regarding the exposed thermal pad dimensions.

PowerPAD is a trademark of Texas Instruments.

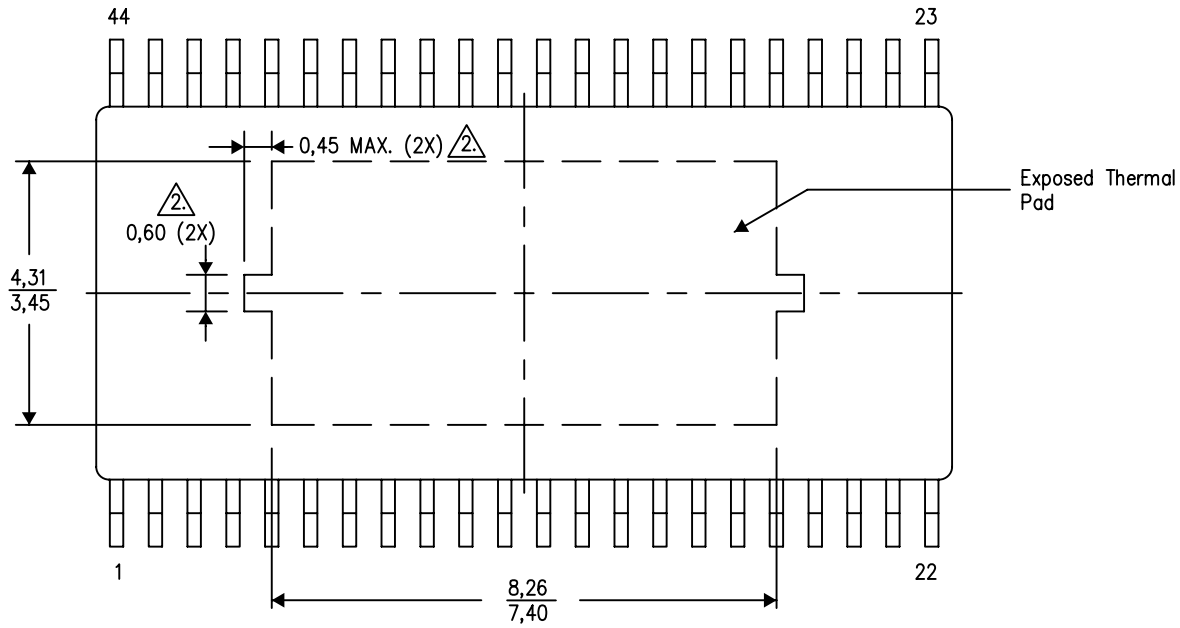
DDW (R–PDSO–G44) PowerPAD™ SMALL OUTLINE PACKAGE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

1. All linear dimensions are in millimeters
2. These features may not be present.

Exposed Thermal Pad Dimensions

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