Spartan-6 LX9 MicroBoard	
Avnet Design Services	
www.em.avnet.com/s6microboard	
Function	**Sheet Number**
Lead Sheet	1
Block Diagram	2
Architecture	3
FPGA Bank 0	4
FPGA Bank 1	5
FPGA Bank 2	6
FPGA Bank 3	7
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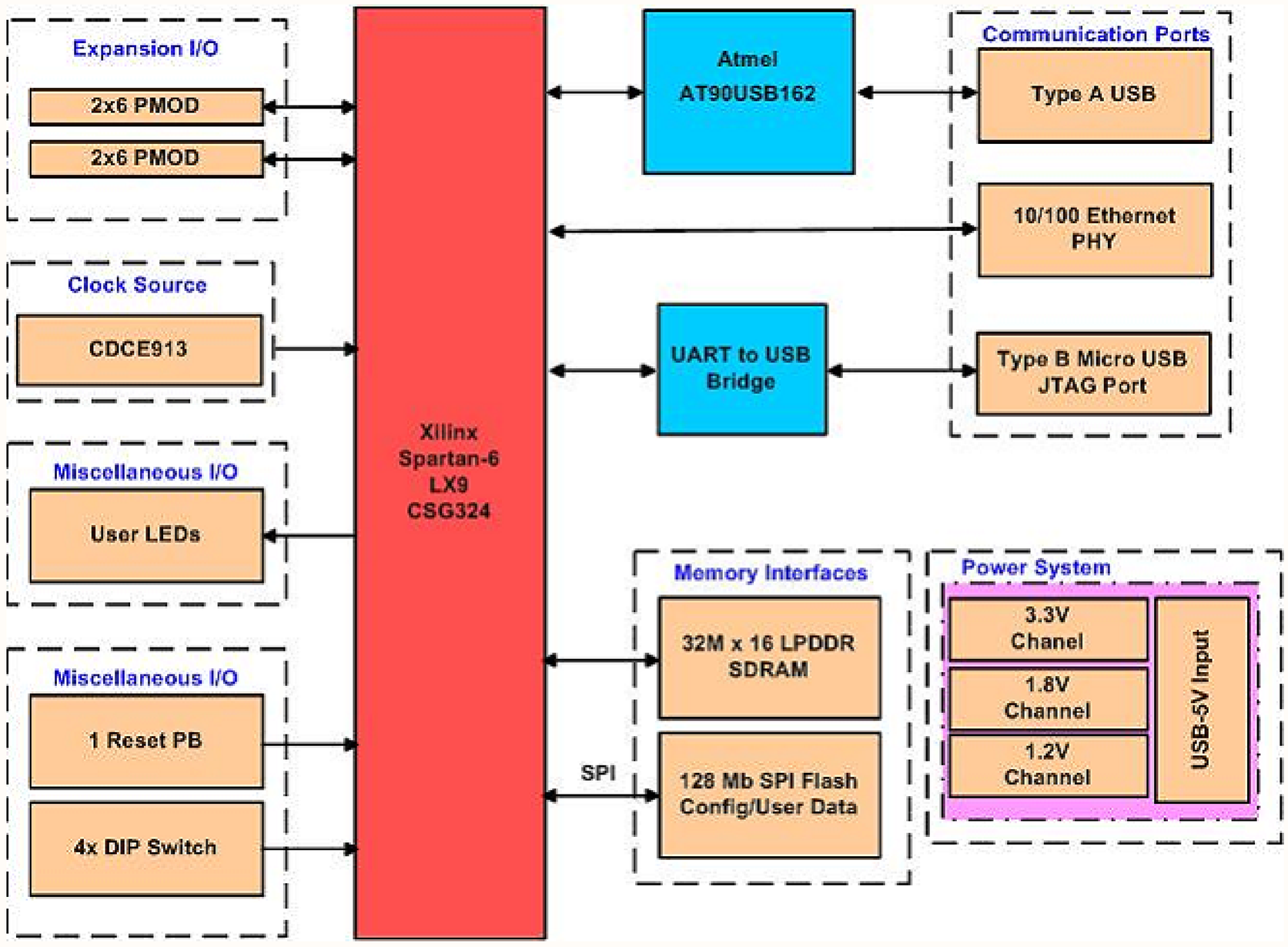
Spartan-6 LX9 MicroBoard Rev C
8/2/2012
2:45:45 PM

Modified Rev A Boards are Functionally Equivalent to Rev B Boards.

Modified Rev B Boards are Functionally Equivalent to Rev C Boards.

X's are a "No ERC" directive to the Design Rule Checker to ignore rule violations.

Avnet Engineering Services		
Title: Sheet 1 - Lead Sheet		
Size: B	Document Number: S6-LX9-SCH-C	Rev: C
Date: 8/2/2012	Sheet 1 of 10	



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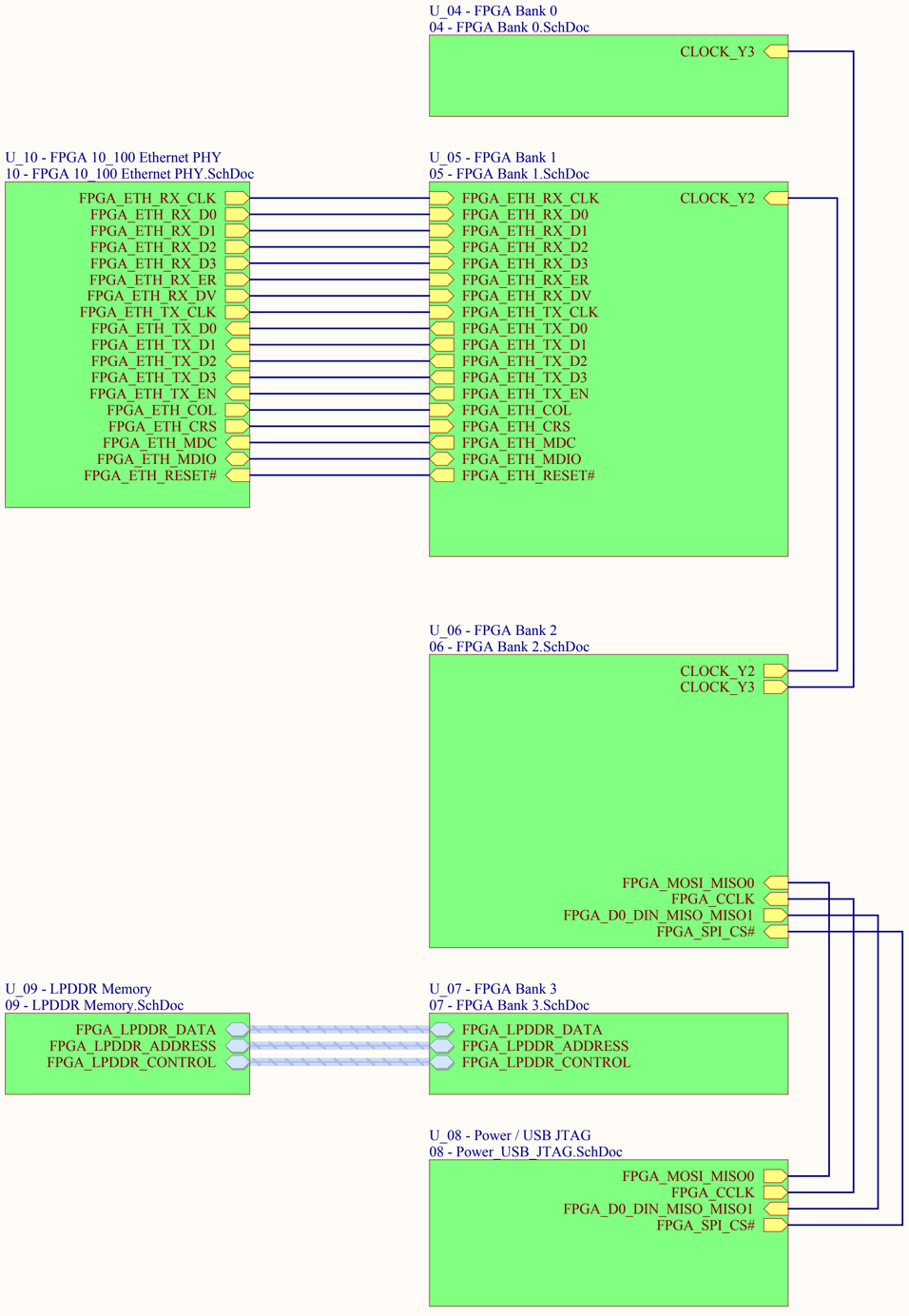
AVNET electronics marketing — Avnet Engineering Services		
Title: Sheet 2 - Block Diagram		
Size: B	Document Number: S6-LX9-SCH-C	Rev: C
Date: 8/2/2012	Sheet 2 of 10	



MTG2
MOUNTING HOLE 125mil

MTG3
MOUNTING HOLE 125mil

MTG1
MOUNTING HOLE 125mil

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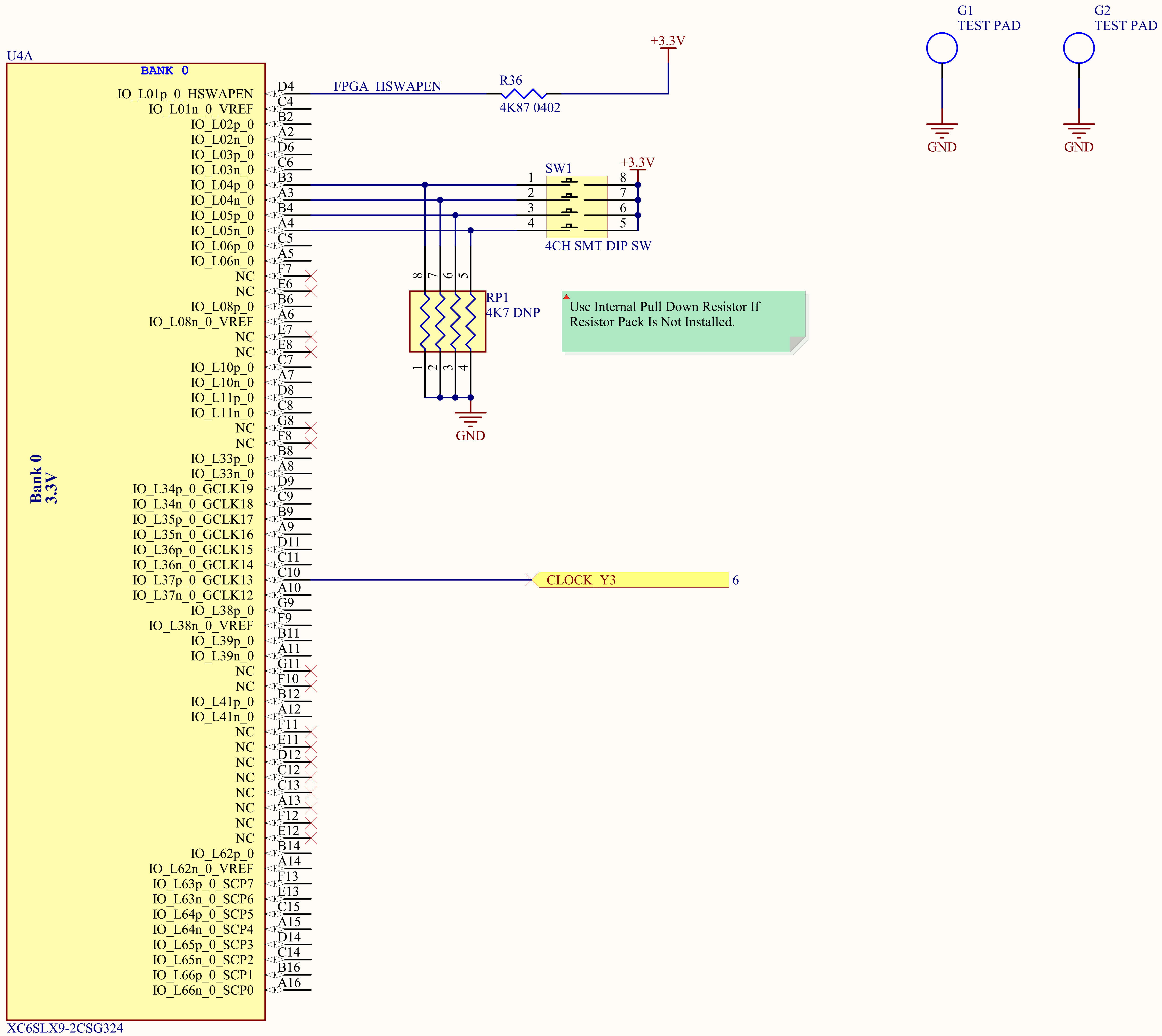
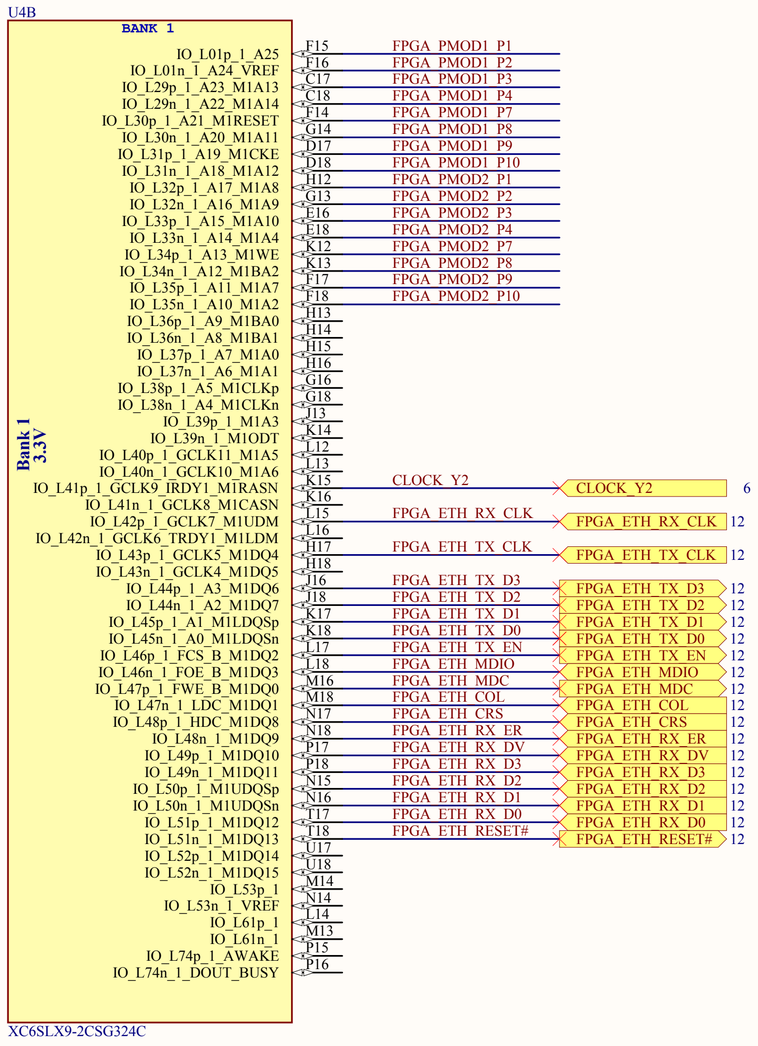
Avnet Engineering Services

Title: Sheet 3 - Architecture		
Size: C	Document Number: S6-LX9-SCH-C	Rev: C
Date: 8/2/2012	Sheet 3 of 10	

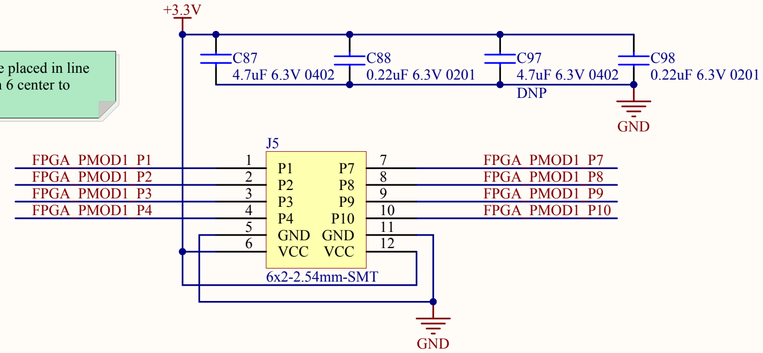


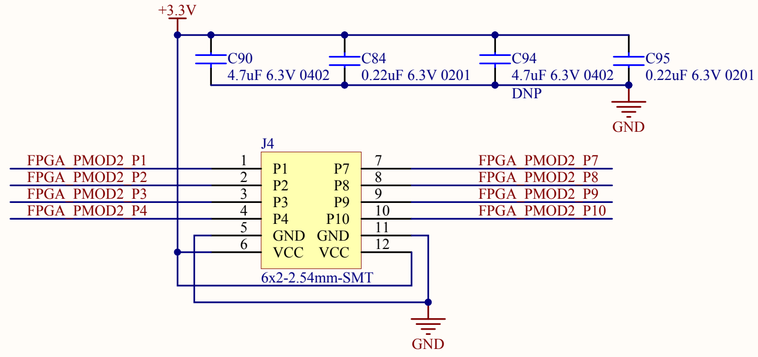
Avnet Engineering Services

Title: Sheet 4 - FPGA Bank 0		
Size: B	Document Number: S6-LX9-SCH-C	Rev: C
Date: 8/2/2012	Sheet 4 of 10	



PMOD Headers must be placed in line with 400mil spacing pin 6 center to following pin 1 center.





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AVNET electronics marketing — Avnet Engineering Services		
Title: Sheet 5 - FPGA Bank 1		
Size: B	Document Number: S6-LX9-SCH-C	Rev: C
Date: 8/2/2012	Sheet 5 of 10	

U4C

Bank 2
3.3V

XC6SLX9-2CSG324C

Place serial termination resistor close to the FPGA

Allow for trace cut
Mode1=0, Mode0=1

Use Internal Pull Up Resistor If Resistor Is Not Installed.

Do Not place power or ground planes under device crystal to reduce stray capacitance.

Place 22 ohm series termination resistors close to clock source.

Optional Switch 3 was removed for Rev B

Use Internal Pull Down If Resistor Is Not Installed.

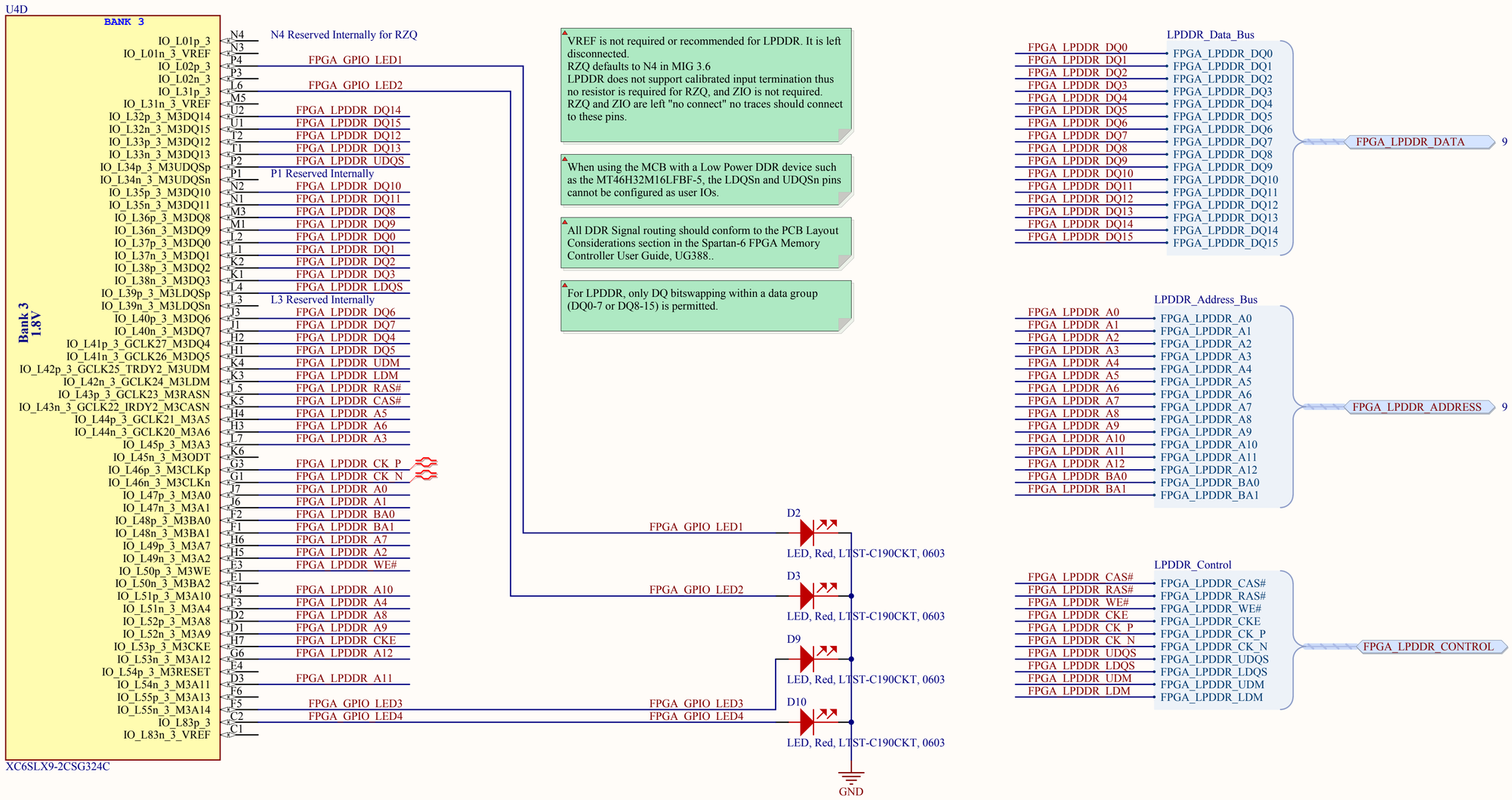
SPI Flash ROM Signal / Pin Equivalences
C = Clock = Input
DQ0 = Serial Data In = Input
DQ1 = Serial Data Out = Output
S_N = CS = Input

Route USB D+/- as 90 ohm differential pairs, 45 ohm to GND

Note: USB Micro AB pin definition corrected in RevC, added

X's are a "No ERC" directive to the Design Rule Checker to ignore rule violations.

Company	Avnet Engineering Services
Title	Sheet 6 - FPGA Bank 2
Size	B
Document Number	S6-LX9-SCH-C
Rev	C
Date	8/2/2012
Sheet	6 of 10


U4D
BANK 3
Bank 3
1.8V
IO_L01p_3
IO_L01n_3_VREF
IO_L02p_3
IO_L02n_3
IO_L31p_3
IO_L31n_3_VREF
IO_L32p_3_M3DQ14
IO_L32n_3_M3DQ15
IO_L33p_3_M3DQ12
IO_L33n_3_M3DQ13
IO_L34p_3_M3UDQSp
IO_L34n_3_M3UDQSn
IO_L35p_3_M3DQ10
IO_L35n_3_M3DQ11
IO_L36p_3_M3DQ8
IO_L36n_3_M3DQ9
IO_L37p_3_M3DQ0
IO_L37n_3_M3DQ1
IO_L38p_3_M3DQ2
IO_L38n_3_M3DQ3
IO_L39p_3_M3LDQSp
IO_L39n_3_M3LDQSn
IO_L40p_3_M3DQ6
IO_L40n_3_M3DQ7
IO_L41p_3_GCLK27_M3DQ4
IO_L41n_3_GCLK26_M3DQ5
IO_L42p_3_GCLK25_TRDY2_M3UDM
IO_L42n_3_GCLK24_M3LDM
IO_L43p_3_GCLK23_M3RASN
IO_L43n_3_GCLK22_IRDY2_M3CASN
IO_L44p_3_GCLK21_M3A5
IO_L44n_3_GCLK20_M3A6
IO_L45p_3_M3A3
IO_L45n_3_M3ODT
IO_L46p_3_M3CLKp
IO_L46n_3_M3CLKn
IO_L47p_3_M3A0
IO_L47n_3_M3A1
IO_L48p_3_M3BA0
IO_L48n_3_M3BA1
IO_L49p_3_M3A7
IO_L49n_3_M3A2
IO_L50p_3_M3WE
IO_L50n_3_M3BA2
IO_L51p_3_M3A10
IO_L51n_3_M3A4
IO_L52p_3_M3A8
IO_L52n_3_M3A9
IO_L53p_3_M3CKE
IO_L53n_3_M3A12
IO_L54p_3_M3RESET
IO_L54n_3_M3A11
IO_L55p_3_M3A13
IO_L55n_3_M3A14
IO_L83p_3
IO_L83n_3_VREF
N4
N3
P4
P3
L6
M5
U2
U1
T2
T1
P2
P1
N2
N1
M3
M1
L2
L1
K2
K1
L4
L3
J3
J1
H2
H1
K4
K3
L5
K5
H4
H3
L7
K6
G3
G1
J7
J6
F2
F1
H6
H5
E3
E1
F4
F3
D2
D1
H7
G6
E4
D3
F6
F5
C2
C1
N4 Reserved Internally for RZQ
FPGA_GPIO_LED1
FPGA_GPIO_LED2
FPGA_LPDDR_DQ14
FPGA_LPDDR_DQ15
FPGA_LPDDR_DQ12
FPGA_LPDDR_DQ13
FPGA_LPDDR_UDQS
P1 Reserved Internally
FPGA_LPDDR_DQ10
FPGA_LPDDR_DQ11
FPGA_LPDDR_DQ8
FPGA_LPDDR_DQ9
FPGA_LPDDR_DQ0
FPGA_LPDDR_DQ1
FPGA_LPDDR_DQ2
FPGA_LPDDR_DQ3
FPGA_LPDDR_LDQS
L3 Reserved Internally
FPGA_LPDDR_DQ6
FPGA_LPDDR_DQ7
FPGA_LPDDR_DQ4
FPGA_LPDDR_DQ5
FPGA_LPDDR_UDM
FPGA_LPDDR_LDM
FPGA_LPDDR_RAS#
FPGA_LPDDR_CAS#
FPGA_LPDDR_A5
FPGA_LPDDR_A6
FPGA_LPDDR_A3
FPGA_LPDDR_CK_P
FPGA_LPDDR_CK_N
FPGA_LPDDR_A0
FPGA_LPDDR_A1
FPGA_LPDDR_BA0
FPGA_LPDDR_BA1
FPGA_LPDDR_A7
FPGA_LPDDR_A2
FPGA_LPDDR_WE#
FPGA_LPDDR_A10
FPGA_LPDDR_A4
FPGA_LPDDR_A8
FPGA_LPDDR_A9
FPGA_LPDDR_CKE
FPGA_LPDDR_A12
FPGA_LPDDR_A11
FPGA_GPIO_LED3
FPGA_GPIO_LED4
XC6SLX9-2CSG324C
VREF is not required or recommended for LPDDR. It is left disconnected.
RZQ defaults to N4 in MIG 3.6
LPDDR does not support calibrated input termination thus no resistor is required for RZQ, and ZIO is not required.
RZQ and ZIO are left "no connect" no traces should connect to these pins.
When using the MCB with a Low Power DDR device such as the MT46H32M16LFBF-5, the LDQSn and UDQSn pins cannot be configured as user IOs.
All DDR Signal routing should conform to the PCB Layout Considerations section in the Spartan-6 FPGA Memory Controller User Guide, UG388..
For LPDDR, only DQ bitswapping within a data group (DQ0-7 or DQ8-15) is permitted.
D2
D3
D9
D10
LED, Red, LTST-C190CKT, 0603
GND
LPDDR_Data_Bus
FPGA_LPDDR_DATA
9
LPDDR_Address_Bus
FPGA_LPDDR_ADDRESS
LPDDR_Control
FPGA_LPDDR_CONTROL
X's are a "No ERC" directive to the Design Rule Checker to ignore rule violations.
Avnet Engineering Services
Title: Sheet 7 - FPGA Bank 3
Size: B
Document Number: S6-LX9-SCH-C
Rev: C
Date: 8/2/2012
Sheet 7 of 10

Route USB D+/- as 90 ohm differential pairs, 45 ohm to GND

Place 22 ohm series termination resistors close to USB XCVR.

P1
USBA RA SMT
VBUS
D-
D+
GND
SHD
SHD
USBA_n
USBA_p
R7 22R 0402
R9 22R 0402
USBA1_n
USBA1_p
D4 PESD0402-140
D5 PESD0402-140
GND

D11 ZEN056V130A24LS
Vin Vout Gnd
+5V_USB_A
C62 0.22uF 6.3V 0201
GND

+3V3_USB_A
C71 4.7uF 6.3V 0402
C47 0.22uF 6.3V 0201
C61 0.22uF 6.3V 0201
GND

Floating Avcc pin 32 was connected to +3V3_USB_A for Rev B

Footprint was fixed for Rev B

U3 AT90USB162-16MUR / ATMEGA162U2
XTAL1
XTAL2(PC0)
GND
VCC
PC2(PCINT11)
PD0(OC.0B/INT0)
PD1(AIN0/INT1)
PD2(RXD1/AIN1/INT2)
PD3(TXD1/INT3)
PD4(INT5)
PD5(XCK/PCINT12)
PD6(RTS/INT6)
PD7(CTS/HWB/T0/INT7)
PB0(SS/PCINT0)
PB1(SCLK/PCINT1)
PB2(PDI/MOSI/PCINT2)
PAD
AVCC
UVCC
D-/SDATA
D+/SCK
UGND
UCAP
(PCINT10)PC4
(PCINT9/OC.1B)PC5
(PC1/dW)Reset
(OC.1A/PCINT8)PC6
(INT4/ICP1/CLK0)PC7
(PCINT7/OC.0A/OC.1C)PB7
(PCINT6)PB6
(PCINT5)PB5
(T1PCINT4)PB4
(PDO/MISO/PCINT3)PB3

X2 NC NC NC NC 8MHz
C11 15pF 25V 0402
C10 15pF 25V 0402
GND

TP1 TEST PAD

J6 Xilinx Parallel IV Connector
GND NC NC TDO GND GND TCK GND TMS GND VREF

Diode is used to prevent any current backflow from a Parallel IV cable connection.

D8 BAS16
+3.3V
RP3 4K7

FPGA_D0_DIN_MISO_MISO1 R24 0R0 0402
FPGA_MOSI_MISO0 R25 0R0 0402
FPGA_CCLK R26 0R0 0402
FPGA_SPI_CS# R28 0R0 0402

J2 HEADER 2/SM
Boot Program En Not
GND

FRAGILE, USE SHUNTS ONLY

R38 0R0 0402
R39 0R0 0402
R8 0R0 0402
R37 0R0 0402
FPGA_TCK A17
FPGA_TMS B18
FPGA_TDO D16
FPGA_TDI D15
TCK
TMS
TDO
TDI

R30 0R0 0402
+3.3V
R41 4K87 0402
C93 4.7uF 6.3V 0402 DNP
GND

Program Start
SW4 SW_PB_SPST_4POS_SMT
Preferred Switch
GND GND

Optional Switch 2 was removed for Rev B

FPGA_PROG V2
PROGRAM_B_2
R35 0R0 0402
SUSPEND R16
SUSPEND
Suspend not used
FPGA_DONE V17
DONE_2
Reserved P13
CMPCS_B_2

+3.3V
R2 300R 0402
D1 LTST-C193TBKT-5A
GND

Two 0.22 0201 Ceramic Caps are substituted for each Xilinx recommended 0.47 0402 Ceramic Caps.

+1.2V
C21 100uF 6.3V 1206
C45 4.7uF 6.3V 0402
C58 4.7uF 6.3V 0402
C49 4.7uF 6.3V 0402 DNP
C48 0.22uF 6.3V 0201
C50 0.22uF 6.3V 0201
GND

+3.3V
C55 100uF 6.3V 1206
C42 4.7uF 6.3V 0402
C37 0.22uF 6.3V 0201
C43 0.22uF 6.3V 0201
C35 0.22uF 6.3V 0201
C36 0.22uF 6.3V 0201
C44 0.22uF 6.3V 0201
C39 0.22uF 6.3V 0201
GND

U4E XC6SLX9-2CSG324C
VCCINT
VCCAUX
VCCO_0
VCCO_1
VCCO_2
VCCO_3
GND

+3.3V
C23 100uF 6.3V 1206
C70 4.7uF 6.3V 0402
C67 0.22uF 6.3V 0201
C38 0.22uF 6.3V 0201
C40 0.22uF 6.3V 0201
C80 0.22uF 6.3V 0201
GND

+3.3V
C82 100uF 6.3V 1206
C68 4.7uF 6.3V 0402
C79 0.22uF 6.3V 0201
C77 0.22uF 6.3V 0201
C57 0.22uF 6.3V 0201
C78 0.22uF 6.3V 0201
GND

+3.3V
C6 100uF 6.3V 1206
C56 4.7uF 6.3V 0402
C69 0.22uF 6.3V 0201
C51 0.22uF 6.3V 0201
C81 0.22uF 6.3V 0201
C59 0.22uF 6.3V 0201
GND

+1.8V
C96 100uF 6.3V 1206
C1 4.7uF 6.3V 0402
C52 0.22uF 6.3V 0201
C46 0.22uF 6.3V 0201
C41 0.22uF 6.3V 0201
C60 0.22uF 6.3V 0201
GND

Route in a similar scheme to the example in the data sheet.

+5V_USB_A D13 DFLS130L-7 +5VUSB
+5V_USB_B D16 DFLS130L-7
C72 4.7uF 6.3V 0402
C73 4.7uF 6.3V 0402 DNP
C76 4.7uF 6.3V 0402
C74 4.7uF 6.3V 0402 DNP
GND

U7 TPS65708
VCC
VIN1
VIN2
VINLDO1
VINLDO2
PWM
MODE
L1
FB1
PGND1
L2
FB2
PGND2
VLDO1
VLDO2
ISINK

L2 2.2UH 600MA 0805
L1 2.2UH 600MA 0805
C86 4.7uF 6.3V 0402
C91 4.7uF 6.3V 0402 DNP
C85 4.7uF 6.3V 0402
C83 4.7uF 6.3V 0402 DNP
C65 4.7uF 6.3V 0402 DNP
C66 4.7uF 6.3V 0402
C24 4.7uF 6.3V 0402
+3.3V +1.8V +2.8V +1.2V
GND

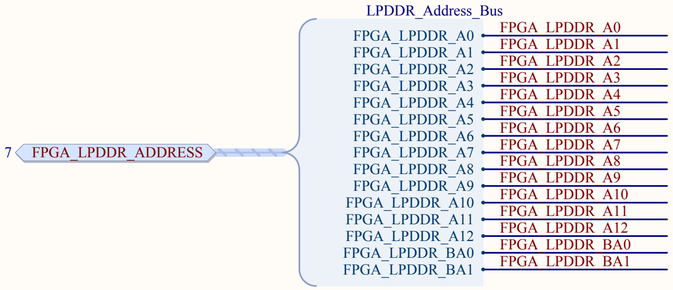
+3.3V
C54 4.7uF 6.3V 0402 DNP
+1.8V
C53 4.7uF 6.3V 0402
R33 0R0 DNP
R34 0R0
+1.2V
C75 4.7uF 6.3V 0402
GND

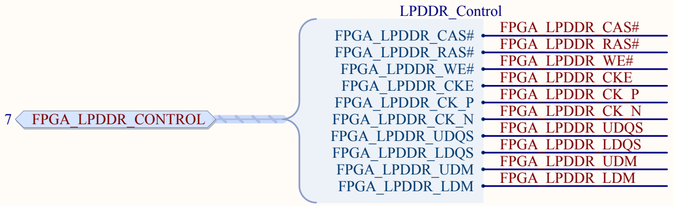
+5VUSB
R11 681R 0402
D7 LED_Green
POWER_GOOD_LED

+5VUSB
Allow for trace cut

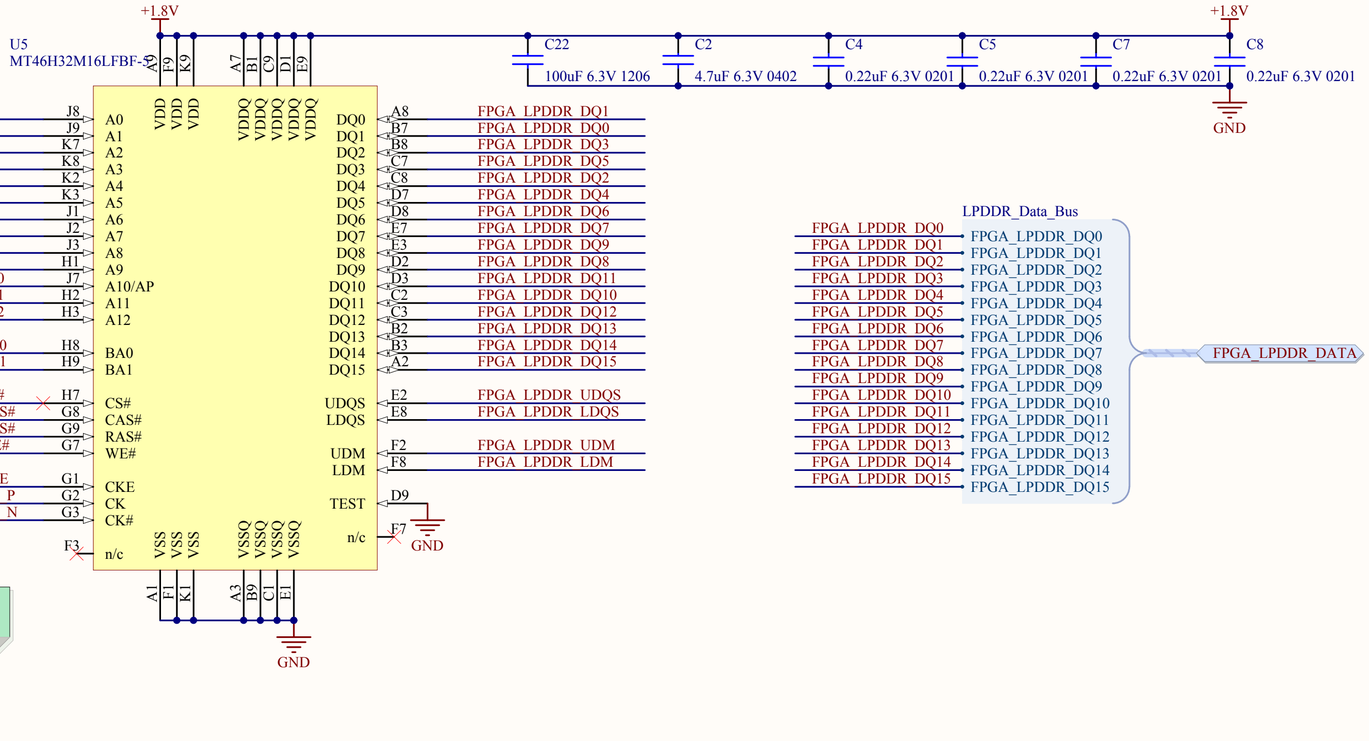
X's are a "No ERC" directive to the Design Rule Checker to ignore rule violations.

AVNET Avnet Engineering Services			
Title: Sheet 8 - Power / USB JTAG			
Size: C	Document Number: S6-LX9-SCH-C		Rev: C
Date: 8/2/2012	Sheet 8 of 10		



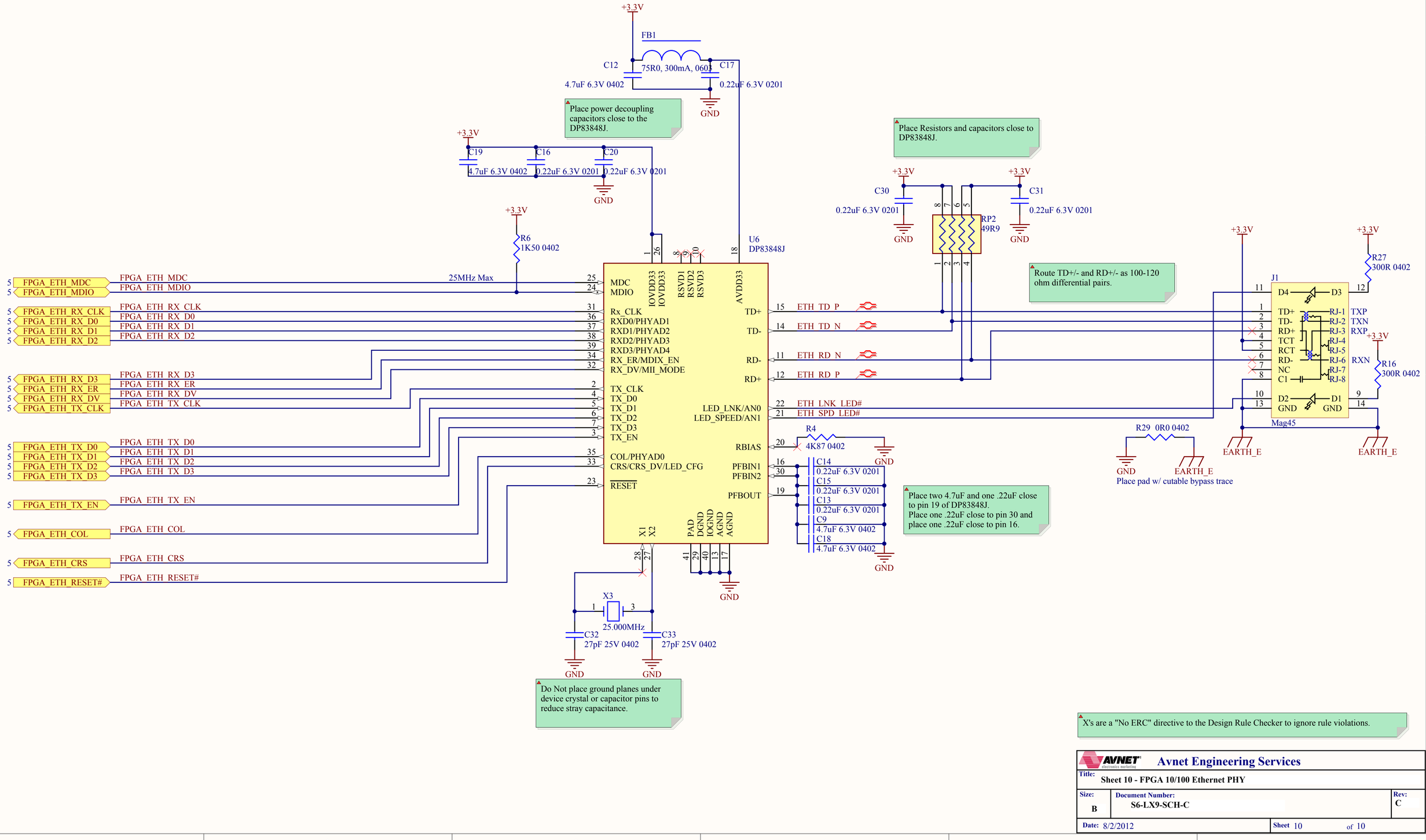


All DDR Signal routing should conform to the PCB Layout Considerations section in the Spartan-6 FPGA Memory Controller User Guide, UG388..



X's are a "No ERC" directive to the Design Rule Checker to ignore rule violations.

Avnet Engineering Services		
Title: Sheet 9 - LPDDR Memory		
Size: B	Document Number: S6-LX9-SCH-C	Rev: C
Date: 8/2/2012	Sheet 9 of 10	



Avnet Engineering Services	
Title:	Sheet 10 - FPGA 10/100 Ethernet PHY
Size: B	Document Number: S6-LX9-SCH-C
Rev:	C
Date: 8/2/2012	Sheet 10 of 10