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non linear parts of the MCP601, MCP6021 and MCP616 models on LT simulator

Issue

What changes are required to support non linear parts of the MCP601, MCP6021 and MCP616 models on LTspice?

Solution

There is a good link on a web site that we used to help troubleshoot the issue:
http://forums.cabling-design.com/Re-Wanted-LM709-(Spice-model)-National-OpAmp-article6652-45.htm

One suggestion in particular was most fruitful:

* Make sure that all semiconductor junctions (and other nonlinear elements) are modeled with realistic series resistances and junction capacitances as well. The importance and effect of something seemingly so mundane as this cannot be overemphasized, for this is what forces linear behavior during time step compression.

If you add the following lines to the model, the model runs correctly:

```
* Extra for LTspice
CD13 2 13 10P
CD16 16 1 10P
CD31 30 31 100P
CD32 30 32 100P
CD55 57 55 100P
CD56 57 56 100P
CD51 51 50 100P
CD52 52 50 100P
CD98 0 98 10P
*
```

If you have trouble with your circuit, I would suggest switching to the alternate analysis engine and increasing the rel tol. They proved fruitful while find good values for the above capacitors.

The model ran on Pspice (orcad v9 and v10) and other simulators with no modifications. If we continue to

see this problem with other simulators that we have not tried that have a large customer base, we may update the models. For now, I think the addition of these lines will get you up and running. You may find that you have to add similar statements with other highly non linear models. The structure of most of the Microchip op amp models are similar, so if you decide to try another op-amp the same statements should work. If you search on the word "table" you will find the locations where a small cap has to be added.

These changes are provided on an as is basis, and you should test the model with the changes in a small test circuit to verify that it still does perform correctly. There may be minor variations introduced, such as a small pole shift or a small slew rate reduction. We have not retested the model for more than basic operation with these changes.

The root cause of the problem is that LTspice does not like the non linear parts of the model that handle input voltage clamping, slew rate limiting, saturation recovery time, saturation voltage of the output and output current limiting.