data bus is stable so that it can be used directly as a R/W pulse to virtually any type of semiconductor memory. Furthermore, the $\overline{WR}$ signal goes inactive one-half T state before the address and data bus contents are changed so that the overlap requirements for almost any type of semiconductor memory type is met.

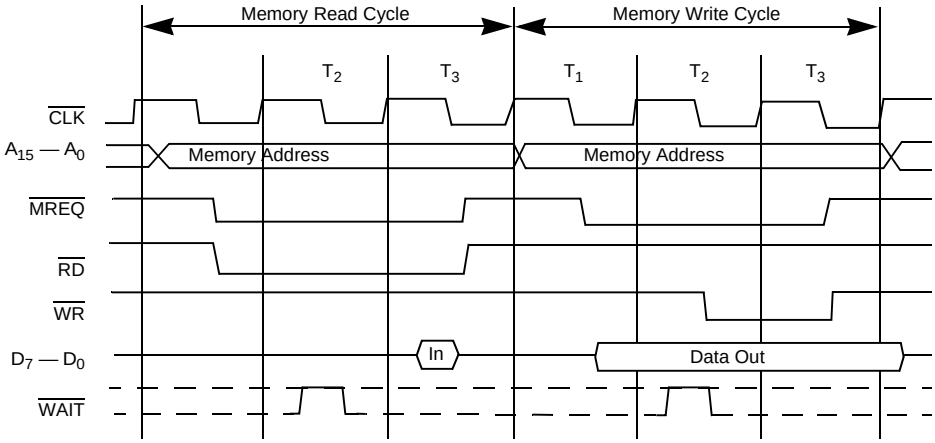

Figure 6. Memory Read or Write Cycle

Input or Output Cycles

Figure 7 illustrates an I/O read or I/O write operation. During I/O operations a single wait state is automatically inserted. The reason is that during I/O operations, the time from when the $\overline{IORQ}$ signal goes active until the CPU must sample the $\overline{WAIT}$ line is very short. Without this extra state, sufficient time does not exist for an I/O port to decode its address and activate the $\overline{WAIT}$ line if a wait is required. Also, without this wait state, it is difficult to design MOS I/O devices that can operate at full CPU speed. During this wait state time, the $\overline{WAIT}$ request signal is sampled.