DIS6531

5.0-Megapixel Camera Module with Autofocus, Shutter & Aperture

Product Data Sheet

General Description

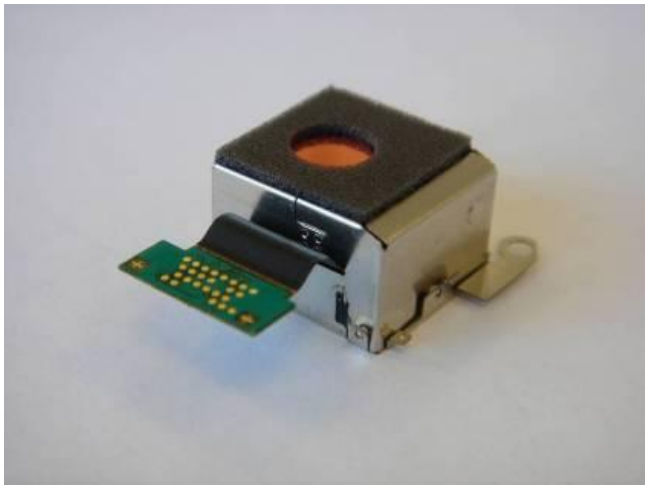
High quality photo imaging and video capability can now be easily embedded into next generation camera-equipped mobile devices such as mobile phones and personal digital assistants (PDA), with the new DIS6531. This full 5.0-Megapixel format digital camera module is a member of the new family of fully integrated camera modules specially targeted and optimized to support mobile applications which provides DSC-picture quality and functionality.

The DIS6531 module has been designed to be embedded in mobile phones experiencing rapid growing user demand to support high end picture quality and high resolution with the quality level delivered in current digital still cameras of the same resolution.

The module provides a complete camera solution comprising a CMOS SOC-camera, an auto-focus lens system, low current actuators, mechanical shutter, aperture and a flex connector.

The DIS6531 module outputs image data with a standard CCIR656 compatible interface. It simply requires two supply voltages and an external system clock of 36MHz (optional 48MHz); all other system clocks are generated internally.

The overall power consumption of the DIS6531 module has been greatly reduced compared to today's solutions to allow integration into mobile handheld devices.



Applications

- **Mobile Phones**
- **Digital Still Cameras**
- **Video Capturing Devices**
- **Handheld Games**
- **Portable Devices**
- **Consumer Products**

Key Features

- **1/2.5” optics with true maximal resolution of 2592x1944 pixels**
- **Frame rate of 30fps at VGA resolution**
- **Lens F# 2.8 (5.6 with aperture enabled)**
- **Focal length 5.56mm**
- **720p video at 30fps (with optional continuous autofocus)**
- **Macro function**
- **Object distance reporting**
- **Linear optics**
- **Low power consumption (<175mW) in viewfinder mode with active autofocus**
- **Module size 13.95x14.95x9.35mm (1.9cm^3)**
- **Two power supply inputs 1.8V and 2.8V**
- **34 pin system connector**
- **CMOS SOC-camera LSI with**
  - **Image DSP pipeline**
  - **Integrated power management**
  - **µController to support custom algorithms**
  - **Internal memory for calibration data**
  - **Command control through I2C**
  - **Parallel data output**
  - **Actuator drivers**
  - **Firmware for AF algorithms**
  - **Windowing features programmable**
  - **Xenon/LED flash trigger output**

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Absolute Maximum Ratings

Supply voltage:	3.6V
Storage temperature:	-40ºC to +85ºC
Input voltage:	-0.3V to VCC + 0.3V
ESD Susceptibility (Note 2)	2000V
Junction temperature:	150ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Conditions

Supply voltage:	1.80V ±5%
	2.85V ±5%
Temperature range:	-20ºC to +70ºC

All voltages are referenced to VSS unless otherwise stated.

Currents flowing into the device are deemed positive, currents flowing out are deemed negative.

All parameters are valid over the full operating temperature range and power supply range unless otherwise stated.

Electrical Characteristics (Note 1)

The following specification apply for T_A = -20ºC to +70ºC.

Symbol	Parameter	Min	Typ	Max	Unit
VCCA	Analog supply voltage	2.70	2.85	3.00	V
VCCD	Digital supply voltage	1.70	1.80	1.90	V
P_{ACT}	Active power consumption		250		mW
P_{STAND_BY}	Stand-by power consumption			300	uW
P_{OFF}	Power down power consumption			50	uW
Digital I/O					
V_{OH}	Output level [high]	VCCD-0.2		VCCD	V
V_{OL}	Output level [low]	0		0.2	V
V_{IH}	Input level [high]	VCCD*0.8		VCCD	V
V_{IL}	Input level [low]	0		VCCD*0.2	V
t_r, t_f	Rise / Fall time			10	ns
I_{DRIVE}	Output drive current			1	mA
I_{LOAD}	Input load current			100	uA
C_{IN}	Input capacitance			10	pF
System clock					
SYS_CLK	System clock frequency	10		50	MHz
	Duty cycle	45		55	%
	Tolerance	-1		1	ppm
t_r, t_f	Rise / Fall time		2	3	ns
T_{JITTER}	Jitter			2	ns
I_{LOAD}	Load current			100	uA
C_{IN}	Input capacitance		10		pF

Note 1:
Electrical Characteristics give DC and AC electrical specifications under certain test conditions with the specified performance parameters. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: Testing based on human body model - 100 pF discharged through a 1.5 kΩ resistor.

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5.0-Megapixel Camera Module with Autofocus, Shutter & Aperture

Product Data Sheet

Functional Description

The DIS6531 is a complete camera module including a 5.0-megapixel sensor with image DSP functionality, lens, housing and flex connector.

Camera features

- 1/2.5” autofocus optics with true maximal resolution of 2592x1944 pixels
- Frame rate of 30fps at VGA resolution
- 720p video at 30fps (with optional continuous autofocus)
- Lens F# 2.8 (5.6 with aperture enabled)
- Focal length 5.56mm
- Macro function
- Object distance reporting
- Linear optics
- Low power consumption (<175mW) in viewfinder mode with active autofocus
- Module size 13.95x14.95x9.35mm (1.9cm^3)
- Only 2 power supply inputs 1.8V and 2.8V
- 34 pin system connector
- CMOS SOC-camera LSI with:
    - Image DSP pipeline
    - Integrated power management
    - µController to support custom algorithms
    - Internal factory calibration
    - Command control through I2C
    - Parallel data output
    - Actuator drivers
    - Firmware for AF algorithms
    - Windowing features programmable
    - Xenon/LED flash trigger output
    - Active and low power stand-by modes supported
    - Vertical and horizontal flip
    - Defect pixel correction
    - Pixel binning for improved low light performance
    - Lens-shading compensation
    - Parallel picture interface support, RAW 10-bit Bayer output

General Specification

The core components in the camera module are a CMOS sensor circuit and an integrated image DSP circuit. The camera module also contains an autofocus lens system, a mechanical shutter, actuators and a flex connector. The camera module is a stand-alone solution that only requires supply voltage, clock and an interface to transfer the pictures.

Parameter	Specification	Remark
Scanning System	Progressive scan	
Optical Format	1/2.5”	
Resolution	2592 H x 1944 V	
Pixel Size	2.2 x 2.2 µm	
Array Diagonal	7.14 mm	
Lens System	1 glass / 2 plastic	
Shutter	1/1000s	Mechanical
Aperture	25% transmission	ND-filter
F Number	2.8	
Hyperfocal Distance	2.0m	
Horizontal Field of View	52.6º	
Normal focus range	30cm to infinity	
Macro focus range	10cm to 40cm	
Lag	<300ms with AF < 150ms for punch through	Focus set to 2m at punch through
Auto focus time	<170ms	Full seek
Dynamic Range (normal mode)	54 dB	
Signal/Noise ratio (max)	38.1dB	
Analog Gain	ISO50 to ISO800	
Exposure Time Control	64 µs to 32.7 ms (@ 30fps)	
Object Distance Reporting	Actual object distance +/- 10% Actual object distance +/-20%	Distance < 60cm Distance > 60cm
Frame Rate	up to 30 fps	
System & Pixel Clock	36 MHz	
Digital Video Output	10 bit parallel Bayer Raw	

Module Specification

Actuator Control

The module contains logic and output drivers to control the actuators for auto focus, for mechanical shutter and for aperture.

Auto Focus (AF)

The module incorporates an auto focus mechanism as an integral part of the system. The auto focus supports “Spot AF” with fully programmable window position and size for areas up to 5% of full image and “Multi-spot AF” with three and five predefined windows with fixed position, size and programmable weighting between those windows. The type of focus is programmable via the serial control interface. Focus tracking is also possible for focusing on moving objects when recording video.

It is possible to override to manual focus in 50 steps over the full focus range and switch specifically to the hyper focal position. The focus position is set via the serial control interface in manual focus mode.

Auto Focus Trigger

The auto focus in the application is triggered by a 2-position button. When the auto focus button is pressed half-ways the focusing starts. Once the auto focus algorithm has found the optimum focus, the focus is locked as long as the button stays half-

way down even if the camera is pointed towards another object. The image is taken when the button is fully pressed. The change of the operating mode between Viewfinder-, AF lock-, and Snapshot- mode is controlled via the serial control interface. The status of the 2-position button is transferred via the serial control interface to the camera module. The button is not part of the camera module.

The auto focus works down to 5lux and for lower light conditions than 5lux the user will have to switch to manual focusing.

Object Distance Reporting

After and autofocus operation, the distance to the object can be read out from the module. This can be used to set the trigger level for the Xenon-flash to be used in conjunction with the quench-circuit to achieve optimal flash performance. The module also supports moving the lens to a fixed object distance. This is for example used for punch through where the lens is moved to an object distance of 2m, for focus failure in low light where the lens also is moved to an object distance of 2m and a user defined landscape mode where the lens is moved to an object distance of infinity.

Position Calibration

The current position of the lens is unknown after reset. Therefore a calibration mechanism is implemented that allows setting the actual position of the lens; i.e. the actual position value of the motor control module.

Shutter Actuator

Due to the fact that the image sensor array has a rolling shutter, there will be motion artifacts in the images when photographing fast moving objects with a high resolution. To improve this and the picture quality for snapshots a mechanical shutter is integrated into the system. With the mechanical shutter the sensor array will no longer be exposed during read out after taking the image. Motion artifacts will be reduced with this mechanism.

There is a limitation for the shutter speed, which may not be fast enough for taking photos in very bright light conditions where the exposure time must be very low. It is proposed to use only the rolling shutter in these scenarios with the potential occurrence of motion artifacts. The following use cases are proposed:

Object Illumination	Use Mechanical Shutter
< 80000 Lux	Yes
> 80000 Lux	No, only imager rolling shutter

Note: 80000 Lux is an equivalent of a sunny day. A brighter illumination may occur in very sunny conditions with additional reflections from e.g. a snow covered surface.

Aperture Actuator

Additionally a controllable aperture using an ND-filter is integrated into the system in order to reduce the amount of light exposing the sensor for improving the image quality in very bright light conditions. The aperture has two states: without ND-filter and with ND-filter.

Sensor Array Specification

The following table outlines the key specifications of the sensor array:

Parameter	Value	Remark
Imager Technology	CMOS	
Active Array Size	5.7 mm x 4.3 mm	
Pixel Size	2.2 µm * 2.2 µm	Square Pixels
Optical Format	1/2.5”	
Active Array Resolution	2592 x 1944 = 5.0MP	Landscape orientation
Color Pattern	Bayer RGB	
Output Format	10 bit Raw Bayer	
Maximum Frame Rate	Full: 5 fps VGA: 30 fps	MCLK = 36MHz
Scan Modes	Progressive Scan with T/B flip and L/R mirror	
Region of Interest	Programmable	
Gain Range	16x analog 16x digital	
Quantum Efficiency	450nm: 42% 530nm: 47% 600nm: 36%	

The following features are associated with the sensor array:

- 4T pixel architecture
- Vertical charge domain binning and horizontal weighted averaging, available in sub sampled modes for lower noise, reduced aliasing, and higher sensitivity still and video capture
- Selectable binning or standard decimated sub sampling modes
- Pinned photodiode architecture; high blue QE, low dark current, lag free, high quantum efficiency
- Micro lenses for increased sensitivity and fill factor
- True correlated double sampling (CDS) for low read noise and pattern noise cancellation
- Anti-blooming control
- Automatic or manual black level clamp
- External sync output signal for use with strobe flash

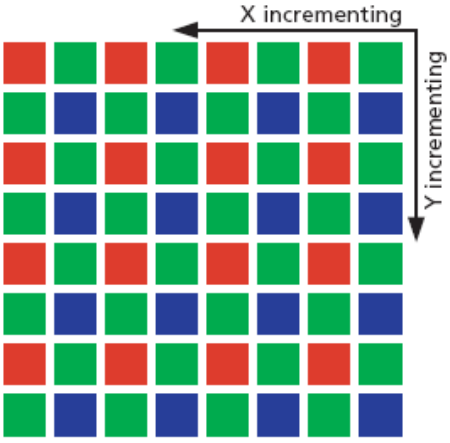
Binning Modes

By default, the resolution of the output image is the full width and height of the FOV as defined above. The output resolution can be reduced by two methods: Skipping and Binning.

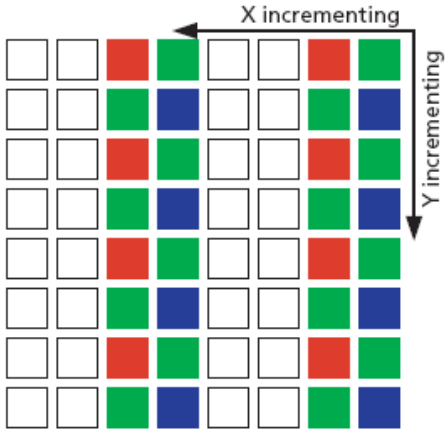
Row and column skip modes use subsampling to reduce the output resolution without reducing FOV. Row and column binning modes, which can reduce the impact of aliasing introduced by the use of skip modes, are also supported. This is achieved by averaging of 2 or 4 adjacent rows and columns (adjacent same-color pixels). Both 2X and 4X binning modes are supported. Rows and columns can be binned independently.

Skipping

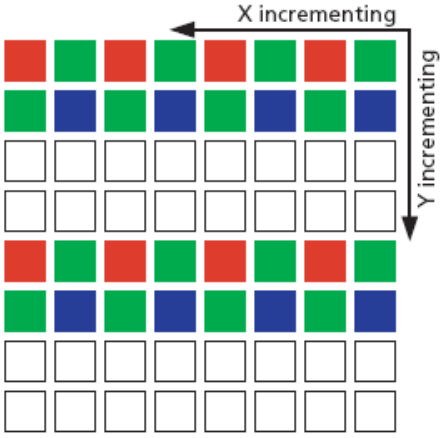
Skipping reduces resolution by using only selected pixels from the FOV in the output image. In skip mode, entire rows and columns of pixels are not sampled, resulting in a lower resolution output image. A skip 2X mode skips one Bayer pair of pixels for every pair output. Skip 4X skips three pairs for each one pair output. Rows and columns are always read out in pairs. If skip 2x mode is enabled with otherwise default sensor settings, the columns in the output image correspond to the pixel array columns 16, 17, 20, 21, 24, 25... Skipping can be enabled separately for rows and columns.



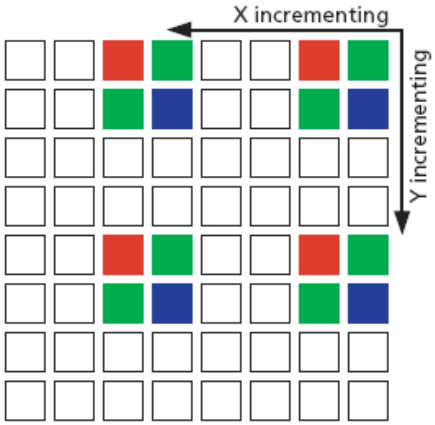
Pixel readout (no skipping)



Pixel readout (Column skip 2X)



Pixel readout (Row skip 2X)

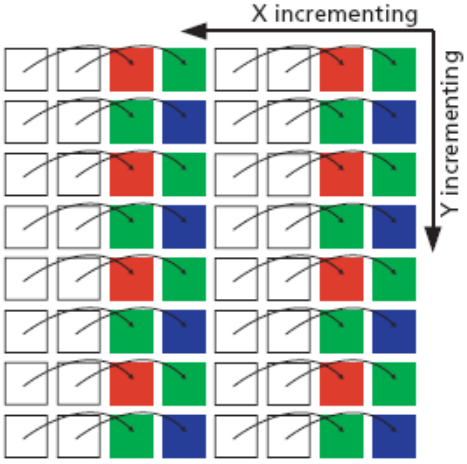


Pixel readout (Column skip 2X, Row skip 2X)

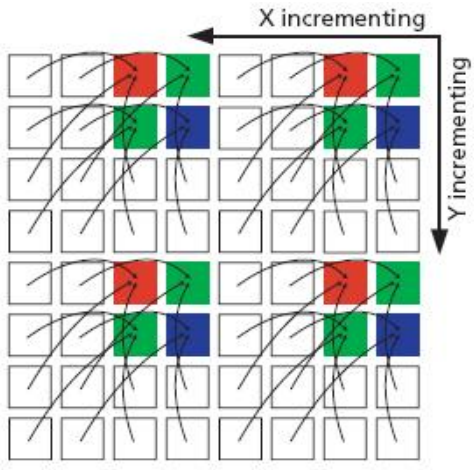
Binning

Binning reduces resolution by combining adjacent same-color imager pixels to produce one output pixel. All of the pixels in the FOV contribute to the output image in bin mode. This can result in a more pleasing output image with reduced subsampling artifacts. It also improves low-light performance. For columns, the combination step can be either an averaging or summing operation. Depending on lighting conditions, one or the other may be desirable. In low-light conditions, summing produces a gain roughly equivalent to the column bin factor.

Binning works in conjunction with skipping. Pixels that would be skipped because of the Column_Skip and Row_Skip settings can be averaged instead by setting Column_Bin and Row_Bin to the number of neighbor pixels to be averaged with each output pixel.



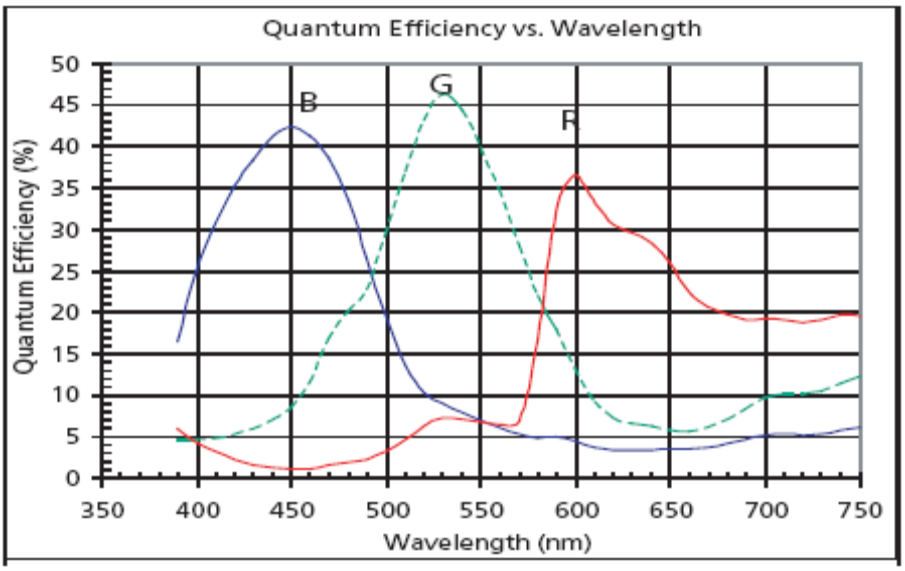
Pixel readout (Column bin 2X)



Pixel readout (Column bin 2X, Row bin 2X)

Quantum Efficiency Data

The following diagram shows the initial QE data. Optimization is ongoing.



Imaging Modes

The module supports different still image modes as described below. They can be run both with and without shutter as well as multiple images in a row for “best picture” functionality. The command interface supports this through an automatic function where only one command is sent to the camera module with an additional parameter stating how many frames to capture.

The module also supports video modes with up to 30 frames per second. The focus function can in this mode either be locked at a pre-defined position or continuous autofocus selected.

Mode	Pixels (Columns)	Pixels (Rows)	W/H Ratio	Frame Rate
5MP (Full frame)	2592	1944	4:3	5 fps
SXGA (2x binned)	1280	960	4:3	15 fps
VGA (4x binned)	648	486	4:3	30 fps
720p (2x skipped)	1280	720	16:9	30 fps

Optics Specification

The optics consists of 1 glass lens and 2 plastic lenses with autofocus capability.

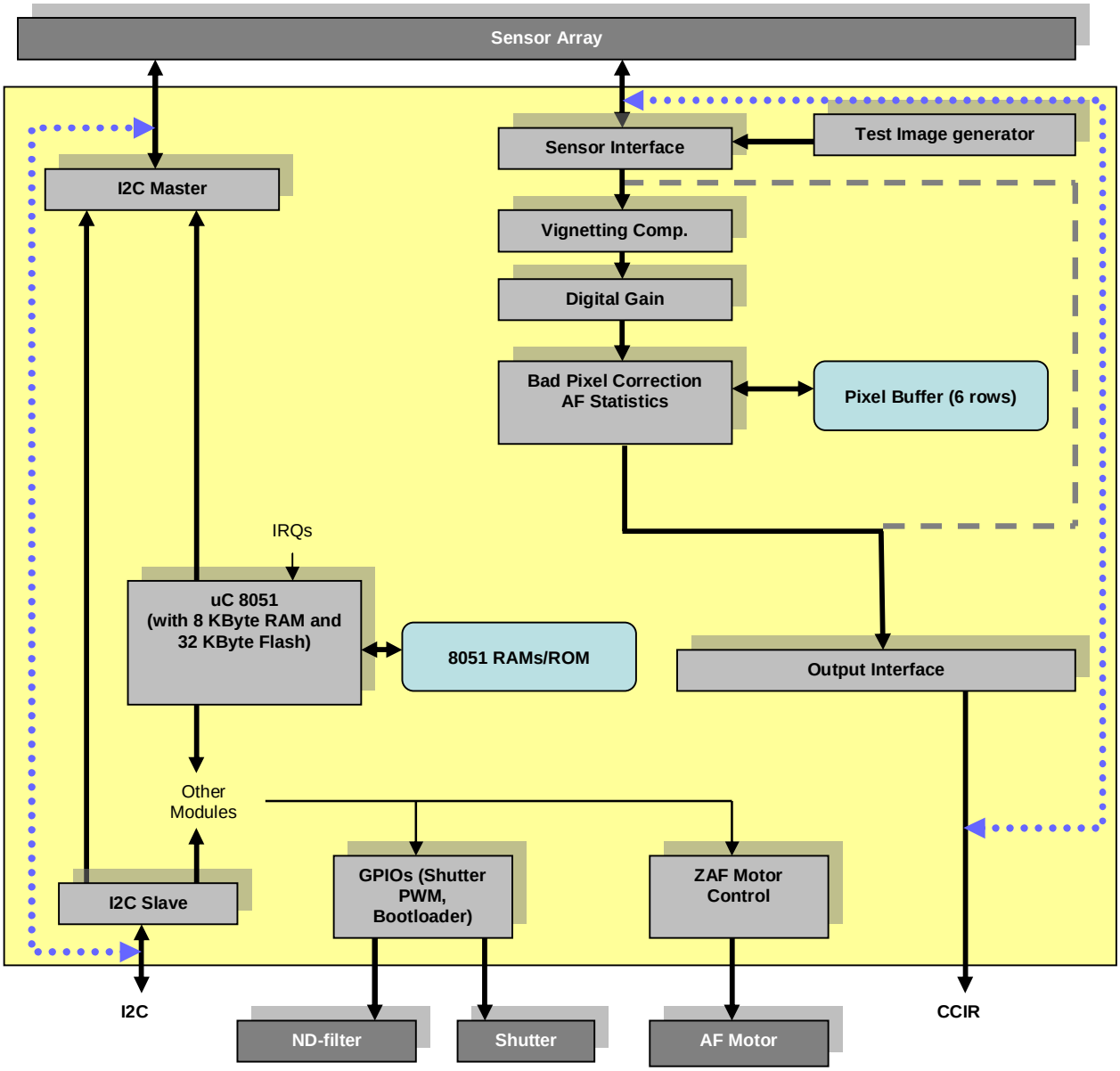
Parameter	Value
Resolution	2592 x 1944 (5.0 MP)
Dimension	5.702 mm x 4.277mm
Pixel pitch	2.2um
Nyquist frequency	228 $^{Lp}/_{mm}$
Image circle	∅ 7.14 mm
F/number	2.8
Effective focal length range	5.56 mm
Horizontal FOV	52.6°
Closest focusing distance	100mm
Straylight	< 2%
TV distortion	1.1%
Illumination relative to image center (independent on focus settings)	> 48%
Maximum illumination decrease over 10% of image height	<7%
IR cut off frequency	640nm

Imaging Performance

Parameter	Value	Remark
Center MTF @ 25lp/mm	0.86	60cm object distance
Center MTF @ 55lp/mm	0.50	60cm object distance
Center MTF @ 55lp/mm	0.50	4m object distance
Corner MTF (60% IH) @ 25lp/mm	0.76	60cm object distance
Corner MTF (60% IH) @ 55lp/mm	0.40	60cm object distance

Imaging DSP Flow Specification

The module supports different imaging DSP algorithms, such as image processing and statistic capturing. It has built-in hardware support for automatic exposure and autofocus control. The utilization of the image processor enables a more complex power saving scheme. This supports the active mode, stand-by mode, sensor-off mode and power-off.



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General

The pixel flow from the sensor will pass a number of processing steps as described in the figure above. Some of these steps gather statistical information about the read out frame that will be used in the processing of following frames, others transform the raw data.

Sensor Interface

The sensor interface handles the image data transfer from the sensor to the ISP part as well as also re-synchronization of the data is to the ISP clock.

Test Image Generator

The Test Image Generator allows to output test images and test image overlays as defined in the SMIA specification. The pre-defined test modes are: no test patterns, solid color, 100% color bars, fade to grey color bars and PN9. It is also possible to insert test cursors into the image using this block.

Vignetting Compensation

Due to limitations of the optical a lens shading effect might be visible and thus needs to be corrected. Because of the different wave length of the three colors, the position of the micro lenses and the geometry and layout of the pixels itself an individual compensation is provided for each pixel and for each direction (x,y). So even in optical zoom systems with changed optical paths and behavior a color shift can be eliminated.

Digital Gain

The digital gain module assists the exposure control by multiplying the pixel values with a provided factor. Thus a fine-grained regulation of the luminance of a picture is possible and allows easy compensation of bigger step widths for the other exposure control parameters (exposure time, analog gain, clock rate). The exposure control provides the digital gain value. The digital gain value is within a range of 0 and 8 and can be set in steps of 1/256.

Bad Pixel Correction

The defect pixel correction block detects bad pixels in an image based on a 5x5 window of pixels. Examination of the pixel in the middle of the window and comparing it with thresholds results in a decision whether the pixel is bad or good. If a pixel is bad it is corrected using the darkest/brightest pixel of the same color in the surrounding 5x5 window.

Auto-Focus Support

Auto focus lens systems vary the distance between the sensor and the lens system. To find the optimal focus normally the sharpness of a region of the image is observed while changing the distance between the sensor and the lens system. The distance will be changed until the maximal sharpness is found. The observation of the sharpness is normally done by searching for the maximal steepness of edges in the image. The Sobel algorithm helps to find a value for the sharpness of an image by summing up the gradients detected in a region of the image. The Sobel algorithm calculates the gradient of one pixel in x and y direction. This is done by applying two different matrixes to the pixel and its surrounding pixels with the same color. For this calculation a 5x5 pixel array is used.

Output Interface

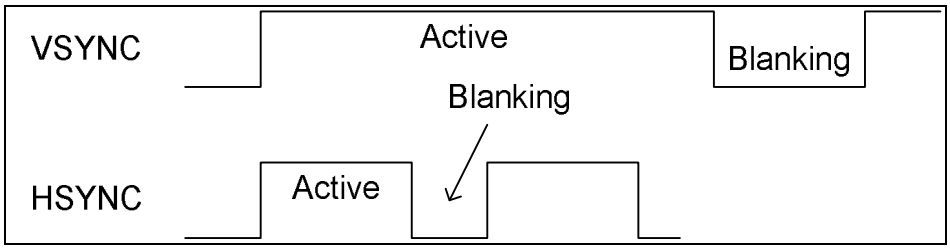
The output interface consists generates the signals to the external image processor. It consists of 10 data lines (PDATA0 - 9), HSYNC, VSYNC and PCLK. The output pixel rate is the same as the sensor pixel rate.

Processor

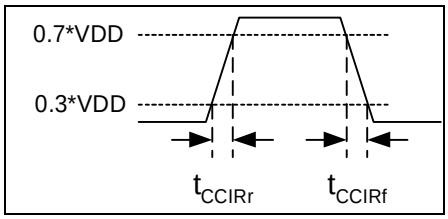
The DIS6531 includes a micro-processor of type 8051 to enhance the functionality and provide extensions to the functions already included in the device.

Parallel Data Output (CCIR601)

The module puts out RAW 10-bit Bayer data for a complete image through the parallel interface. The signals in the interface comprises of PCLK (pixel clock), VSYNC (vertical sync), HSYNC (horizontal sync) and Data[9-0]. PCLK varies with frame rate and can be programmed so that it is only available when HSYNC is high or always on.



Timing



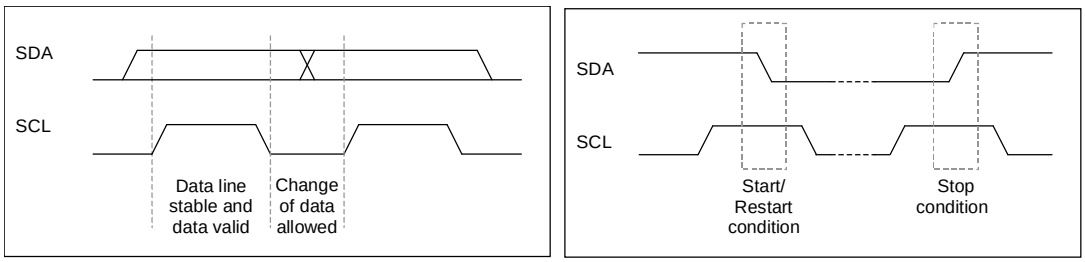
Symbol	Description	Reference	Min	Max
t_{CCIRr}	All data output signals rise time	30pF load	-	8 ns
t_{CCIRf}	All data output signals fall time	30pF load	-	8 ns
t_{VHs}	VSYNC & HSYNC setup time	Before PCLK rising edge	¼*PCLK	¾*PCLK
t_{Ds}	Data setup time	Before PCLK rising edge	¼*PLCK	¾*PCLK
t_{Dh}	Data hold time	After PCLK rising edge	¼*PCLK	¾*PCLK
t_{VHh}	HSYNC & VSYNC hold time	After PCLK rising edge	¼*PCLK	¾*PCLK

Control Interface

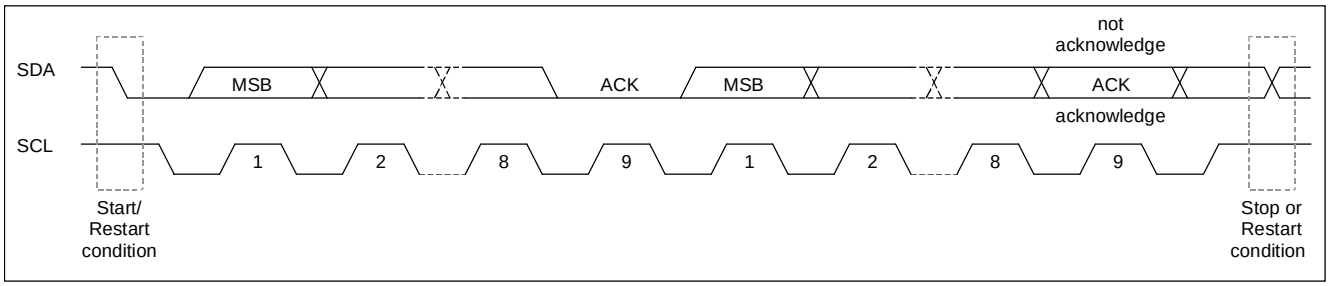
The hardware layer that is used for the control data is an I2C compatible interface. It is also possible to read back the content of the registers through this interface. The camera module is set up through this interface and the picture data is output through the parallel or serial interface.

Data Transfer

The data on the two serial lines of the control bus are transferred bit by bit. The data bit on the SDA line is valid during the SCL line is high. During this high period of the SCL line the SDA data line must be stable. If the SCL line is in a low state a change of the SDA data line is allowed. Additionally to the bit transfer the control bus defines special conditions called Start (S) and Stop (P). The Start condition signals a start of data transfer whereas the stop condition terminates the bus transfer. A start condition occurs when there is a transition of the SDA line from high to low while the SCL line is high. A stop condition occurs if the SDA line goes from low to high while the SCL line is asserted.



The master device generates the Start and Stop conditions, whereas data transfer can happen in both directions (read/write). Instead of termination a bus transfer with the stop command an immediate new transfer can be started by the master with a repeated Start (Sr) command. The repeated start command has the same characteristics as the normal Start condition.
The data transfer on the I2C bus is done in byte packets (8-bit). The number of bytes that can be transmitted in a transfer cycle is not restricted. Each byte is transmitted with the MSB first and each byte is followed by an Acknowledge bit (A). The device receiving the data bits sets the acknowledge bit (master sends data and the slave acknowledges or slave sends data and master acknowledges).

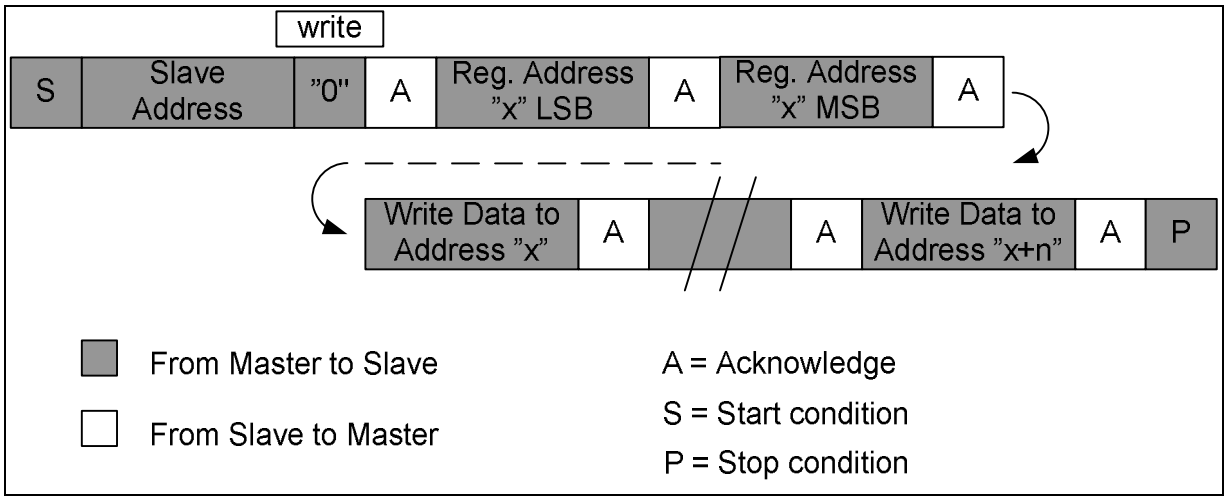


For the acknowledge clock cycle the receiver of the data byte must pull down the SDA line so that it is stable low during the high period of SCL. The acknowledge cycle occurs after each transmitted byte. If a slave is not able to process a transfer or additional bytes it leaves the SDA line in high state (not acknowledge). In case of a write access the master has to start a new transfer to write the data byte that was not acknowledged. If the slave transmits data to the master (read access) the master has to not acknowledge the last byte of the transfer to signal the slave to release the data line. This allows the master to set a Stop or Restart condition. Anyway a not acknowledged byte is followed by a stop or restart condition of the master device in any case. The data transfer follows the terminology mentioned as 7-bit addressing in the I2C specification. In this mode a 7-bit address is send by the master after the start/restart condition. This 7-bit address selects the slave to be accessed. The eighth bit of the first byte specifies the data transfer direction. A ‘0’ represent a write access whereas a ‘1’ indicates a read.

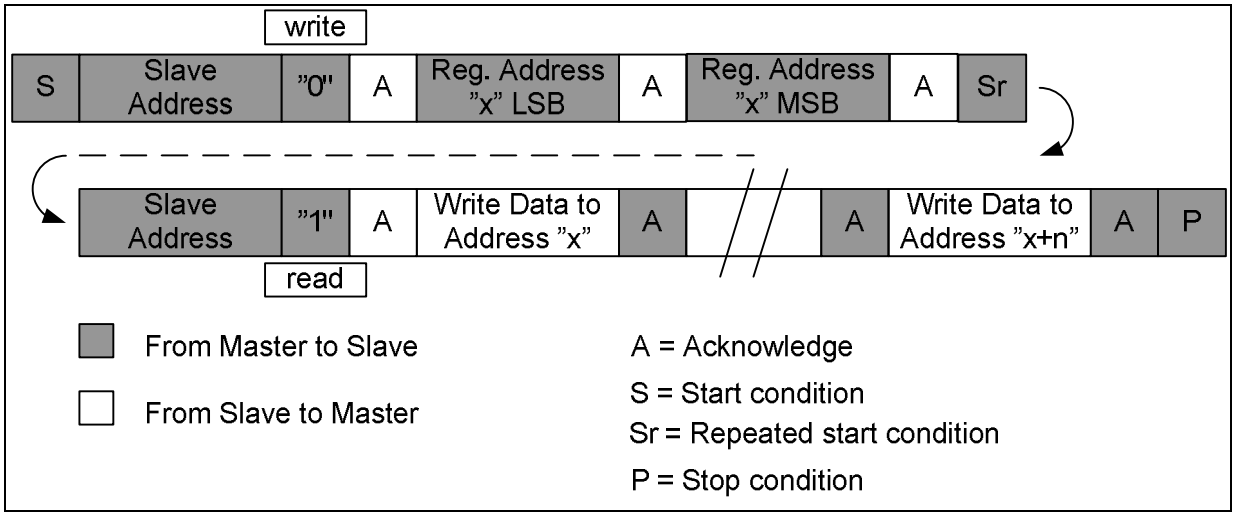
The DIS6531 has a fixed SLAVE address of:

- **60_{Hex}** $C0_{Hex}$ in case of write access and $C1_{Hex}$ in case of read access

Depending on the read/write indication the transmission direction of the next bytes is determined. A write access consists of at least four bytes. After the slave address byte, the LSB and MSB byte addresses of the addressed register is transmitted followed by at least one write byte. If the transfer contains more than one write byte the register address is internally incremented and the following bytes are written to the updated addresses. The addresses always increments with one so also unused addresses are included.



A read access is always done on the currently stored register address. This address is either the incremented byte address of the last access (read or write) or the address adjusted by a transfer just before the read access. The following figure shows a read access with preceding address adjustment transfer.



The Restart condition after the address adjustment cycle in the diagram above may also be replaced by a stop condition and a new start condition.

Processor Command Control

Access to the internal registers in DIS6531 is done through a command interface using the micro-processor in the device and an external API for high level control of the camera module. The internal registers used in the camera module are defined here.

The processor registers can always be accessed directly using a standard I2C compatible structure.

Processor Control

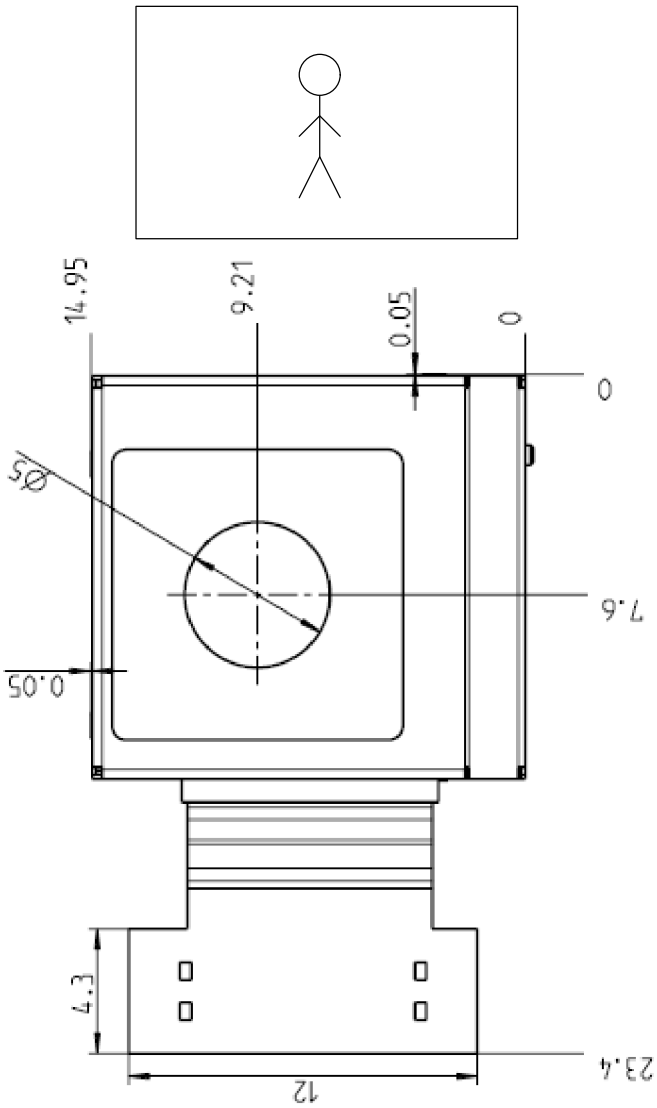
Address (Hex)	Data Width	Default (Hex)	R/W	Description
100B	8	00	R/W	Processor configuration Bit[7:2]: Reserved Bit[1]: Processor reset **0**: Enabled 1: Disabled (processor running) Bit[0]: Reserved
50C0	8	00	R/W	Start up mode 0x00: No initialization 0x01: Hard motor initialization 0x02: Hard motor initialization + viewfinder start 0x03: Soft motor initialization + viewfinder start
50C1	8	00	R/W	User defined data 1 byte
50C2	8	00	R/W	User defined data 2 byte
50C3	8	00	R/W	User defined data 3 byte
50C4	8	00	R/W	User defined data 4 byte
50C5	8	00	R/W	Processor command register

API – High Level Camera Control Interface

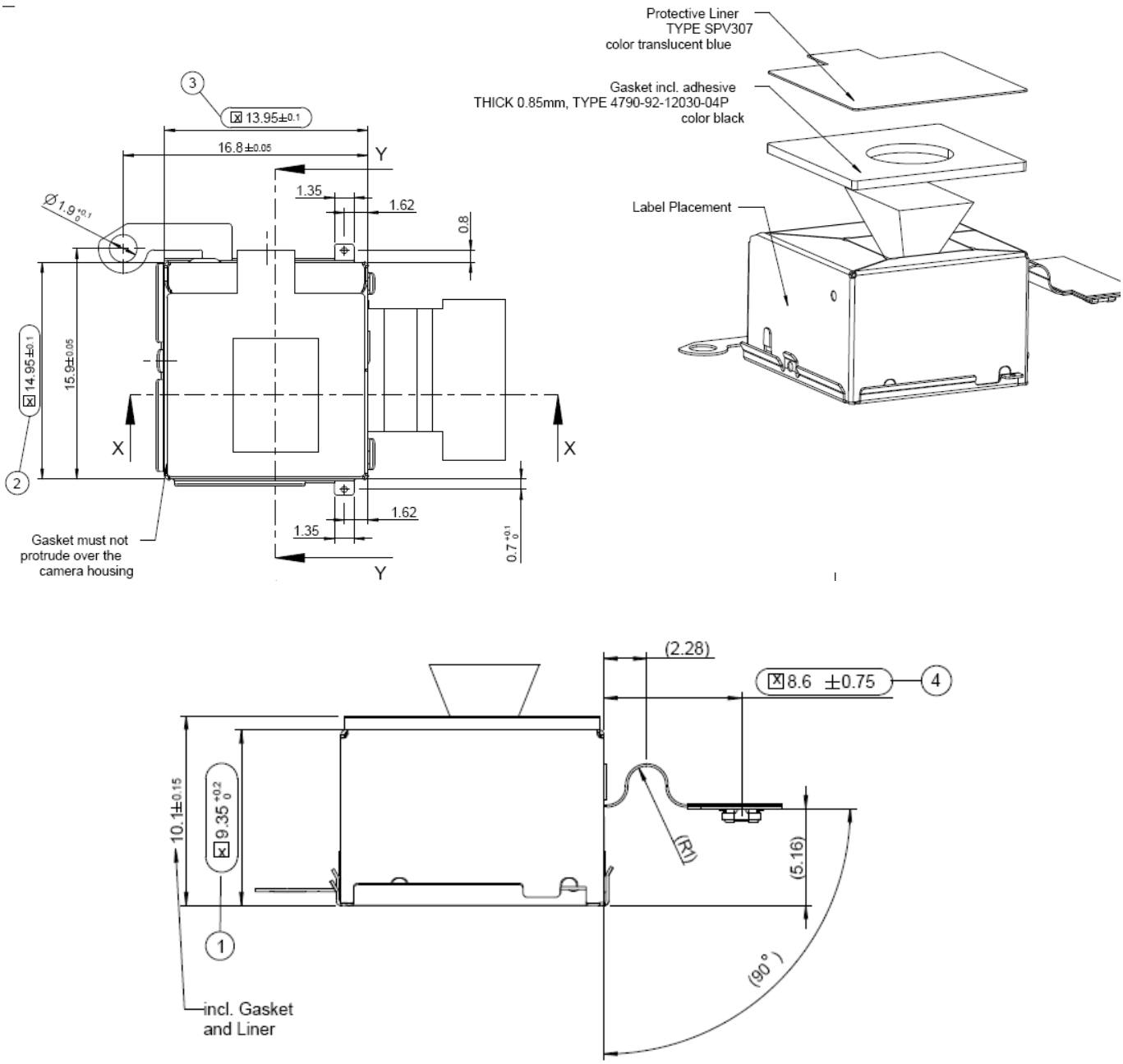
The camera module is supplied together with a high level control interface (API) that normally runs in the host processor. This interface enables easy and fast programming as well as upgrades between different modules in the same host system. Please refer to the application note, DIS-AN03, for more information about this control interface.

Image Orientation

The standard image orientation in the module is as follows. The image can be vertically and horizontally mirrored via the control interface.



Mechanical Module Information

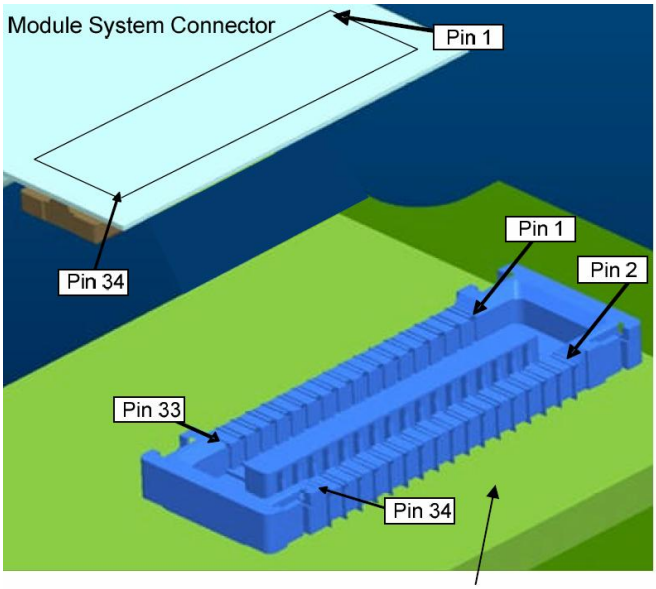


Pin Description

The following table shows the part numbers for the camera connector and the mating unit:

Name	Part number	Remark
Camera Connector	Molex 501594-3410	
Mating Connector	Molex 501591-3410	

The connector has the following pin 1 definition:



Customer PCB (use Molex 501-591-3410 Connector)

The pins on the module have the following functions:

Pin	Name	Type	Pin Description
1	**GND**	PS	**Ground**
2	**GND**	PS	**Ground**
3	**GND**	PS	**Ground**
4	AVDD	PS	Regulated voltage input 3.0V +/-10%
5	**GND**	PS	**Ground**
6	**GND**	PS	**Ground**
7	D8	DO	Data 8
8	D9	DO	Data 9
9	D6	DO	Data 6
10	D7	DO	Data 7
11	D4	DO	Data 4
12	D5	DO	Data 5
13	D2	DO	Data 2
14	D3	DO	Data 3
15	N.C.	-	Connect to ground in application
16	N.C.	-	Connect to ground in application
17	D0	DO	Data 0
18	D1	DO	Data 1
19	**GND**	PS	**Ground**
20	**GND**	PS	**Ground**
21	HSYNC	DO	Horizontal synchronization
22	VSYNC	DO	Vertical synchronization
23	N.C.	-	Connect to DVDD (1.8V) in application
24	DVDD	PS	Regulated voltage input 1.8V +/- 10%
25	VDD	PS	Regulated voltage input 3.0V +/- 10%
26	RSTn	DI	Module reset
27	MCLK	DI	System clock input (10 to 50MHz)
28	PCLK	DO	Pixel clock
29	STROBE	DO	Flash strobe control signal
30	DVDD	PS	Regulated voltage input 1.8V +/- 10%
31	SCL	DI	Serial control clock
32	SDA	DIO	Serial control data
33	**GND**	PS	**Ground**
34	**GND**	PS	**Ground**

Production & Reliability Testing

Volume Production Testing

A fully automated test system is used for testing each camera module before delivery. This test system verifies not only electrical parameters but also complete optical parameters such as focus accuracy, MTF, optical tilt, particles and bad pixels. It also captures a flat field image and calibrates the lens shading parameters used internally in the module and externally by the ISP (if applicable).

Additional data such as serial number, production date and bin class is also programmed into the non-volatile memory of the module.

A complete test specification is available upon request.

Reliability Testing

The camera module is verified during development according to a well defined flow. Normal procedure is to use this data as a starting point when qualifying the module for use in the end application. Additional tests might be necessary to fully qualify the module for use in a certain application. DIS can manage these tests as well based on an agreed specification.

A complete DIS reliability specification is available upon request.

Packaging and Shipping

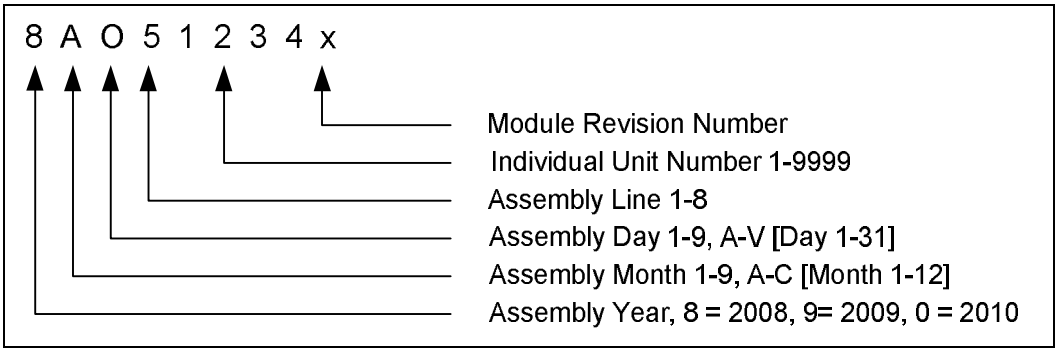
Camera Module Labelling

Each individual camera module is labelled. The label use a micro QR code as shown in the following figures:

The label also shows the following two items in human readable text:

1. D I S 6 5 3 1 (…or Customer Part Number)
2. Date code (in clear text as below)
2. DISh.h.ff.t (h.h = hardware version, ff = firmware version, t = test version)

The following figure shows the label.

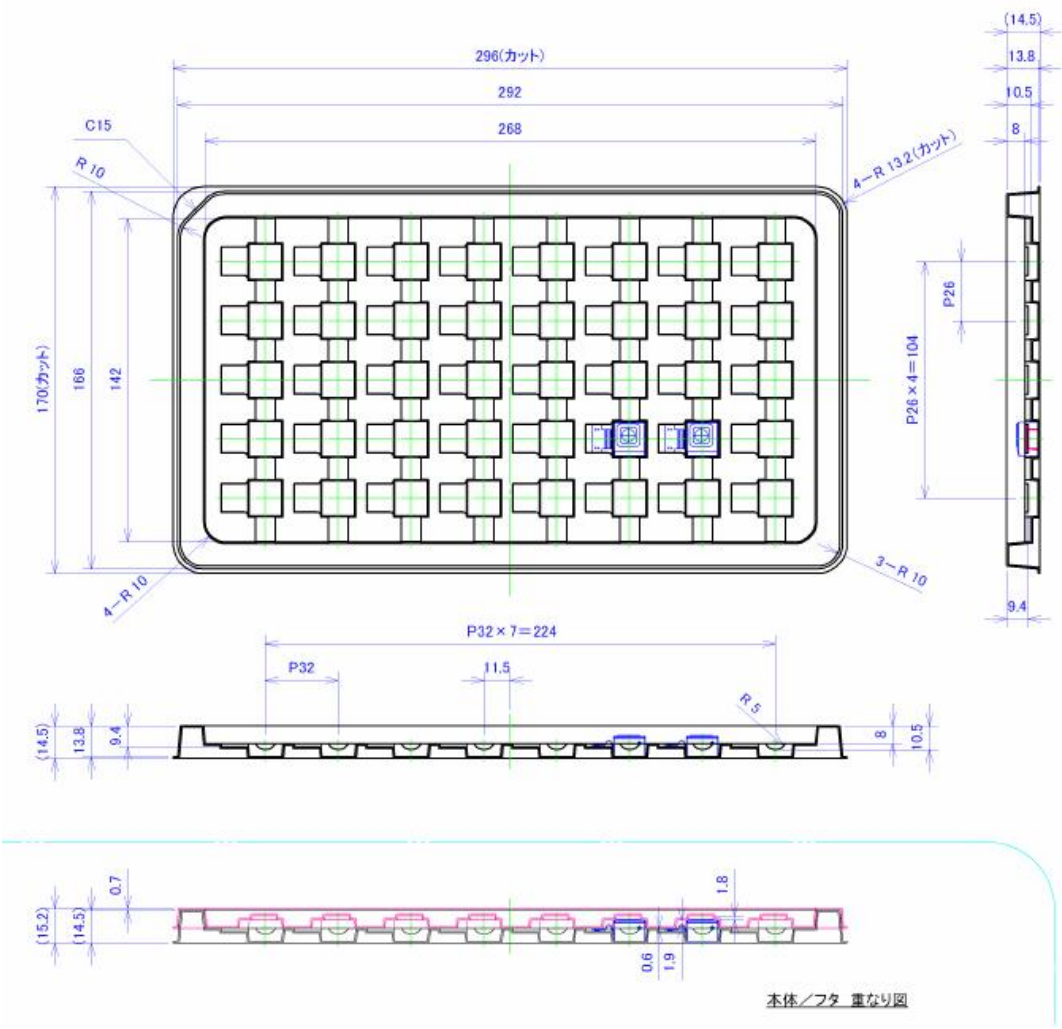


5.0-Megapixel Camera Module with Autofocus, Shutter & Aperture

Product Data Sheet

Trays

The camera module is shipped in trays with 40pcs each. The following figure shows the tray:



Ordering Information

Part Number	Size [mm]	Description
DIS6531	13.95x14.95x9.35	5.0Mpixel camera module with autofocus, shutter and aperture

Digital Imagng Systems Worldwide

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