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FIELD-STORE STANDARDS CONVERSION: a technical description of the C06/508 converter

No. 1972/22

Research Department, Engineering Division
THE BRITISH BROADCASTING CORPORATION

RESEARCH DEPARTMENT

FIELD-STORE STANDARDS CONVERSION: A TECHNICAL DESCRIPTION OF THE C06/508 CONVERTER

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Head of Research Department

(PH-86)

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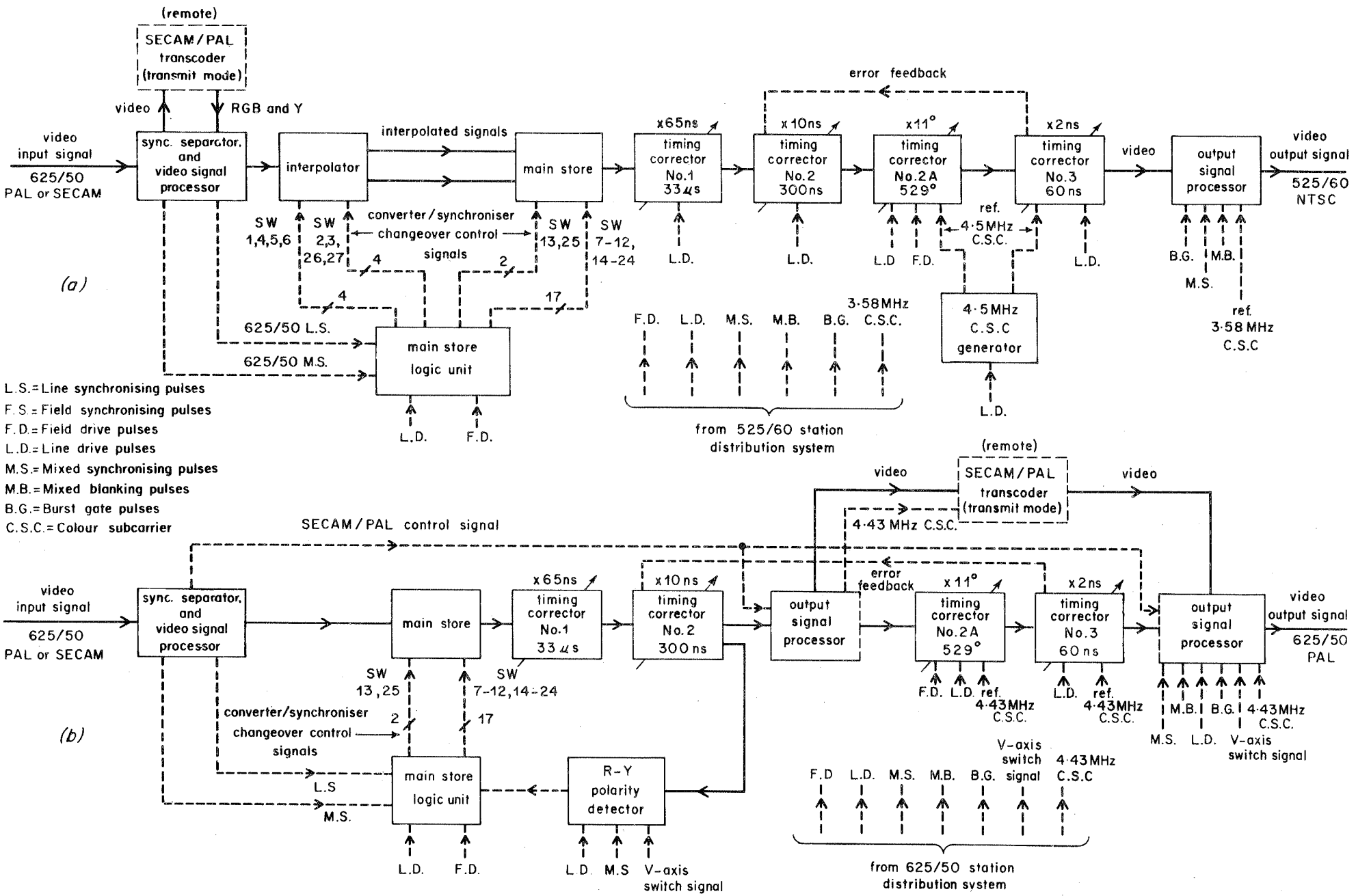

Fig. 1 - Converter/synchroniser basic block diagram

(*a*) Converter mode (*b*) Synchroniser mode

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FIELD-STORE STANDARDS CONVERSION: A TECHNICAL DESCRIPTION OF THE C06/508 CONVERTER

Summary

*This report describes points of technical interest in the design and development of the C06/508 field-store standards converter which converts in the direction 625/50 PAL/SECAM to 525/60 NTSC.**

*Many aspects of design in this converter are the same as, or similar to those used in the earlier C06/506** converter which converts 525/60 NTSC signals to the 625/50 PAL standard and is described in Research Department Report No. 1970/37. The present report does not describe common features, but rather compares the two converters pointing out any areas of special interest. Some items are of sufficient interest and complexity to merit reports of their own, and these are referred to where applicable. Reference is also made to the additional synchronising capability of the C06/508 converter, but only where the switchover from 'convert' mode to 'synchronise' mode is of interest. A comprehensive description of the equipment when used as a synchroniser can be found elsewhere.*[3]

* Sometimes described as the BBC Mk 2B Standards Converter.
** Sometimes described as the BBC Mk 2A Standards Converter.

1. Introduction

Following the successful development of the C06/508 converter which operates in the 525/60 NTSC to 625/50 PAL direction, the same principles have been used in achieving conversion in the opposite direction. The new machine differs from the earlier one in that a new facility has been added, namely the ability to synchronise any input PAL, SECAM or monochrome 625/50 'remote' source (within a certain specified frequency tolerance) to 'local' 625/50 signals. This facility was added in order to take advantage of the large, continuously-variable delay in the main store and timing corrector; this delay has a maximum duration of just over one input (50 Hz) field period, and is adjusted at the beginning of each line to preserve the synchronism between the remote and local sources.

2. Outline description of the converter/synchroniser

Fig. 1 is a block diagram of the equipment in its convert and synchronise modes respectively.

2.1. Sync separator and video signal processor[1]

In the convert mode, PAL signals are transcoded into an intermediate system of colour coding with a line-locked subcarrier of 4·5 MHz, the actual frequency being an integral multiple of line frequency, necessary to permit the interpolator to carry out inter-line averaging.[1,10] SECAM signals are routed to a remote SECAM-to-PAL transcoder which for this purpose operates only as a SECAM decoder, whose output R, G, B and Y signals are then coded into the intermediate system. The intermediate video signal is then modulated on a frequency-modulated carrier with a centre frequency of 30 MHz for passage through the delay units of the standards converter. Mixed syncs and line syncs are separated from the incoming composite signal and fed to the main store logic unit.

In the synchronise mode, there is no intermediate transcoder and the input PAL signals are subjected only to blanking and special burst and sync insertion[1] before entering the synchroniser. In the case of SECAM input signals, these are passed through the synchroniser before being transcoded to PAL at the output.

2.2. Interpolator

The interpolator is used only in the convert mode. Its function is to produce, from the input 625/50 line-signals,* a stream of line-signals which correspond closely in picture content with those which would have been obtained by scanning the original scene on the 525/60 standard. The field frequency is unchanged at this stage; thus a picture is formed by the interpolator in which 100 of the original 625 lines, spaced at roughly equal intervals are potentially redundant. It will be observed that there are two interpolator outputs. The extra output carries signals for the additional field which is inserted into the converted field sequence every 5 input fields. This subject is dealt with more fully under Section 3.

* In this report the term 'line-signal' is used to describe a signal carrying the picture information for one television scanning line.

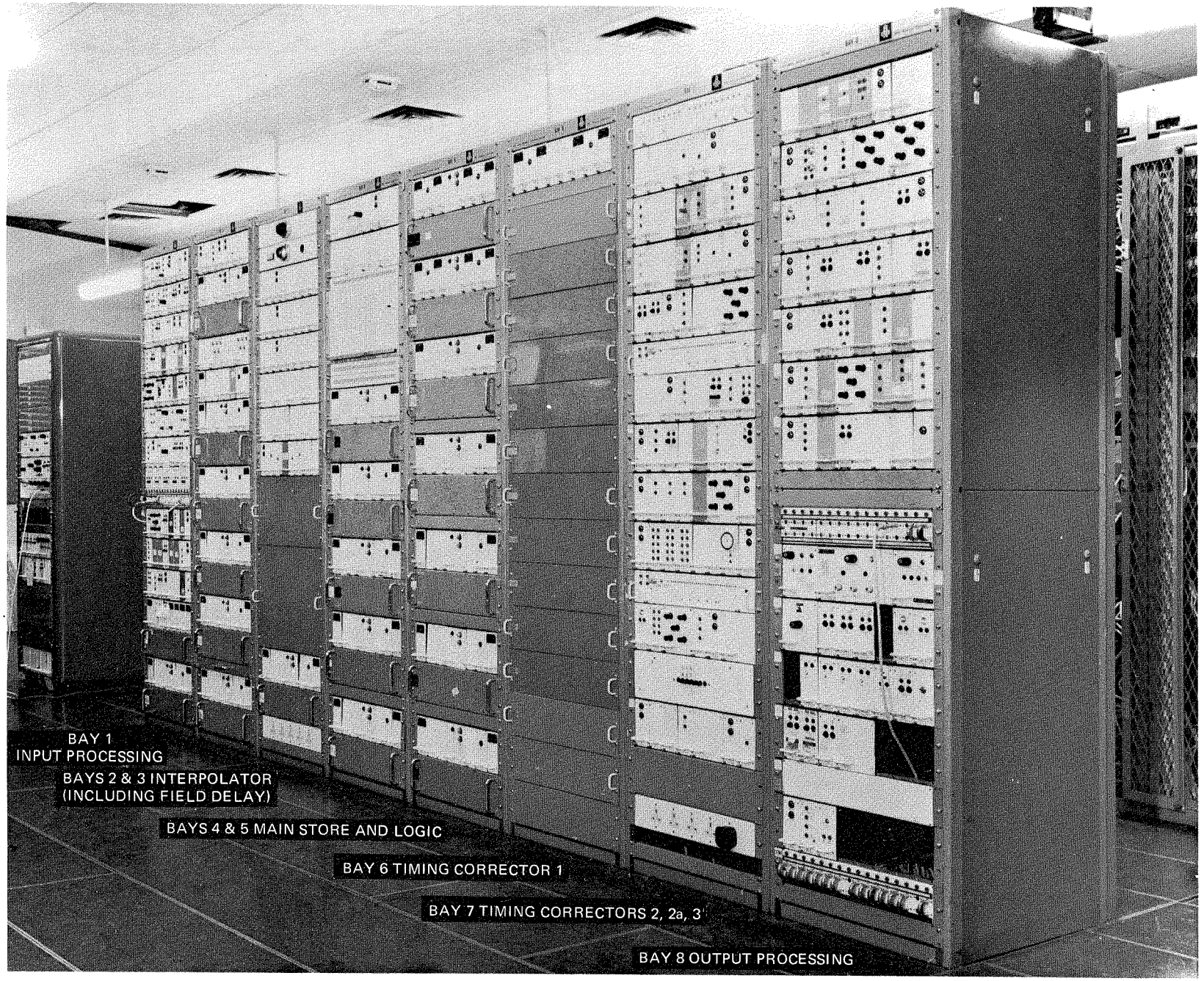


Fig. 2 - BBC Mk 2B converter in operational area at Television Centre

2.3. Main store

In the convert mode, the function of the main store is to remove the 100 lines per picture (50 lines per field) which are not required in the output picture. In doing this, the main store, which is an arrangement of switched delays, reduces the field duration from 1/50 sec to 1/59·94 sec. Approximately every 5 input fields, an extra field is inserted into the signal path; this occurs each time the main store is reset from zero delay to maximum delay and results in a 'field duplication'. The process is closely analogous to that which takes place in the earlier converter in which a 'field omission' takes place approximately every 6 input fields.

In the synchronise mode, the main store functions essentially as a variable delay placed in the path of the incoming signal, the delay being updated once per field to keep the output from the main store within range of the timing corrector.

2.4. Main store logic unit

The main store logic unit generates all the control waveforms for the delay-controlling switches in the interpolator and main store. It generates these waveforms from information obtained from the synchronising pulses of both the input and output standards.

Separate logic control circuits exist for the convert and synchronise modes and these come into operation automatically, depending upon which mode is selected.

2.5. Timing correctors 1, 2, 2A, 3[2]

Although the design of the timing corrector in the C06/508 converter differs fundamentally from that in the earlier C06/508 converter, its function is the same, namely, to produce from the very irregularly timed output lines of the main store precisely timed video signal which match the output synchronising pulses supplied to the converter, from the local station distribution system. Timing correction takes place in 4 stages; Timing Corrector 1 reduces errors in the timing of the signal from approximately 18 μs ($\pm$9 μs), to 65 ns. Timing Corrector 2 further reduces the errors to 10 ns, and Timing Corrector 3 further reduces the error to a theoretical minimum of 2 ns. In practice, because of spurious signals and noise, 5 ns is the best achieved; the timing correctors are more fully described in another report.[2] Timing Corrector 2A is necessary because, in the PAL system, the absolute phase of the colour subcarrier is not defined. Thus, two independent signals may be precisely synchronous as far as line synchronising pulses are concerned but their subcarriers may have any phase difference. In the convert mode, where the intermediate colour system is used, timing corrector 2A, is not necessary, but it remains in the circuit as a fixed delay.

2.6. Output signal processor[1]

In the convert mode, the output from timing corrector 3 is transcoded from the intermediate colour system to NTSC to form the output signal.

In the synchronise mode, no transcoding is necessary for PAL signals and signal processing consists simply of the re-insertion of burst and synchronisation signals. As mentioned earlier, SECAM signals are transcoded to PAL after passing through the synchroniser; in addition, because of the less critical timing requirements of SECAM signals, timing correctors 2A and 3 are not needed and are bypassed.

2.7. Physical layout

The converter/synchroniser is housed in eight bays, and is illustrated by the photograph shown in Fig. 2.

3. Interpolator

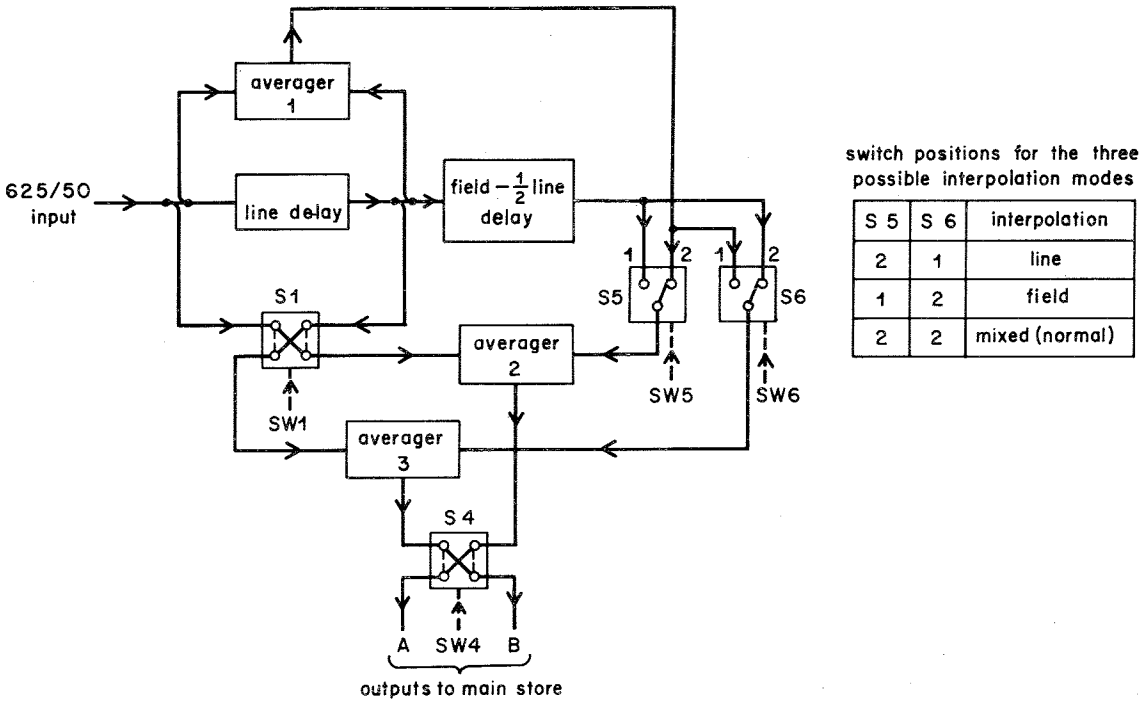
The interpolator, the main store, and the main store logic unit will be described more fully, since they are not the subject of separate reports. As in the case of the earlier (C06/508) converter, conversion without interpolation would result in two types of picture distortion, geometric distortion due to the relative shifts of picture information and line structure when changing the number of television lines, and movement portrayal distortion when changing the number of fields per second. Whereas geometric distortion in the converter being described is caused by the omission of roughly every 6th line, the equivalent distortion when converting in the other direction is due to the duplication of roughly every 5th line. The subjective impairments are very similar however.

Movement portrayal distortion is due to the increase in field frequency from 50 Hz to 60 Hz involving the duplication of roughly every 5th input field, as opposed to conversion in the opposite direction in which distortion is due to omitting every 6th input field. As might be expected, the interpolator block diagrams of the two forms of converter bear some resemblance to one another; Fig. 3(*a*) is a simplified schematic and Fig. 5 gives more detail. As in the earlier converter provision is made for three types of interpolation, 'Line' interpolation, 'Field' interpolation and 'Mixed' interpolation. The operation of the interpolator in all three modes will now be described with reference to Fig. 3.

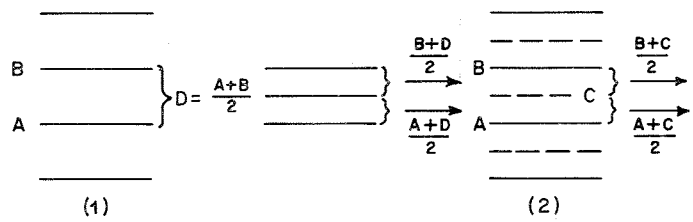
3.1. 'Line' interpolation

Consider the case where switches S5 and S6 are in the positions shown for 'line' interpolation.

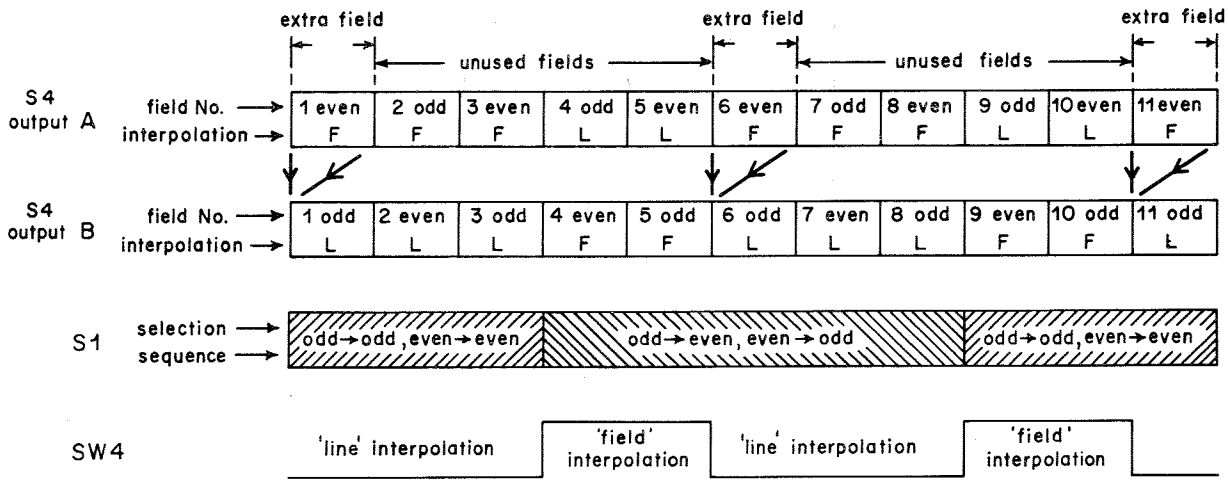
Fig. 3(*b*) (i) shows a magnified part of the raster containing four successive lines of a field. Consider two adjacent lines, say A and B. The output of Averager 1 in Fig. 3(*a*) will be (A + B)/2 which we shall call D. The outputs of Averagers 2 and 3 will then be represented by (B + D)/2 and (A + D)/2 or (A + D)/2 and (B + D)/2 respectively, depending on the state of switch S1. It is the function of S1 to select, for a given output, either (B + D)/2 or (A + D)/2, whichever corresponds most closely with the picture information expected at that position on the output raster. It is also a property of the system that if for example, the selection sequence on S1 is such as to produce an even field at the output of Averager 2, then the



(a)



(b)



(c)

Fig. 3 - Interpolator: simplified block diagram and output signal characteristics

(*a*) Block diagram and switch positions (*b*) Interpolation between raster lines
(*c*) Characteristics of signals emerging from the interpolator

same selection will produce an odd version of the same field at the output of Averager 3. This is because (B + D)/2 and (A + D)/2 represent picture information on adjacent picture lines. It will be seen in Section 4.1 that this ability to produce odd and even versions of the same field at the same time is an essential property of an interpolator operating in this direction of conversion. Line interpolation provides no compensation for impaired movement portrayal, and, as in the earlier converter, it is treated as an inferior mode of operation which nevertheless can be useful for maintenance purposes and under certain unusual operational conditions.

3.2. 'Field' interpolation

Consider S5 and S6 in the condition for 'Field' interpolation.

Fig. 3(*b*) (2) illustrates a magnified part of the input raster showing four successive lines of a field together with the positions occupied by the line of the previous field shown dotted. These lines from the previous field are available at the output of the (field – ½L) delay (Fig. 3(*a*)). The outputs of Averagers 2 and 3 will hence be (B + C)/2 and (A + C)/2 or (A + C)/2 and (B + C)/2 respectively, again depending on the selection sequence on S1, which is identical to that used for the line interpolation mode.

The advantage of field interpolation over line interpolation is that in field interpolation, the intermediate line C is available as directly scanned picture information whereas in line interpolation it has to be synthesised as (A + B)/2, with consequent loss in vertical resolution. As in line interpolation, field interpolation does not provide compensation for impaired movement portrayal.

3.3. 'Mixed' interpolation

The effect of mixed interpolation on movement portrayal is plotted in Fig. 4 which shows the error in the displayed or mean position of an object moving within the scene. The error is depicted in units of input field period as conveniently describing the distance moved. Field Interpolation and Line Interpolation each show similar effects, displaced by a distance equivalent to half of one input field-period. The error in position increases steadily up to a maximum when it is abruptly reduced to zero; this is when the duplication of a field occurs. If either field or line interpolation were used alone, severe 'movement judder' would result. Mixed interpolation, which is achieved by switching between line and field interpolation systematically, is shown in heavy lines on Fig. 4; it will be seen that its effect is to halve the maximum error and to double the rate of judder; the result is subjectively acceptable.

It is interesting to compare Fig. 4 with Fig. 3.4 in EL-47, which shows the equivalent movement portrayal for the converter operating in the opposite direction. The main difference between the graphs is in the number of fields constituting a complete cycle; this is five for the early converter (525/60-to-625/50) and six when converting from 625/50-to-525/60, which gives a slightly better movement portrayal.

4. Main store

4.1. Operation of the main store down to the 1T delay

With reference to Fig. 3 there are two interpolator outputs, A and B and these form the input to the main store. Although the signals appearing at each of these outputs are related to unchanged field durations (i.e. there are still 625 lines per picture and each field still has a duration of 1/50 second), the line-signals in each field are modified by the interpolation process to correspond closely in vertical information with the line positions which they are destined to occupy on the output standard. This means that in each field appearing at the output of the interpolator, there are 50 redundant lines spaced more or less regularly down the field.

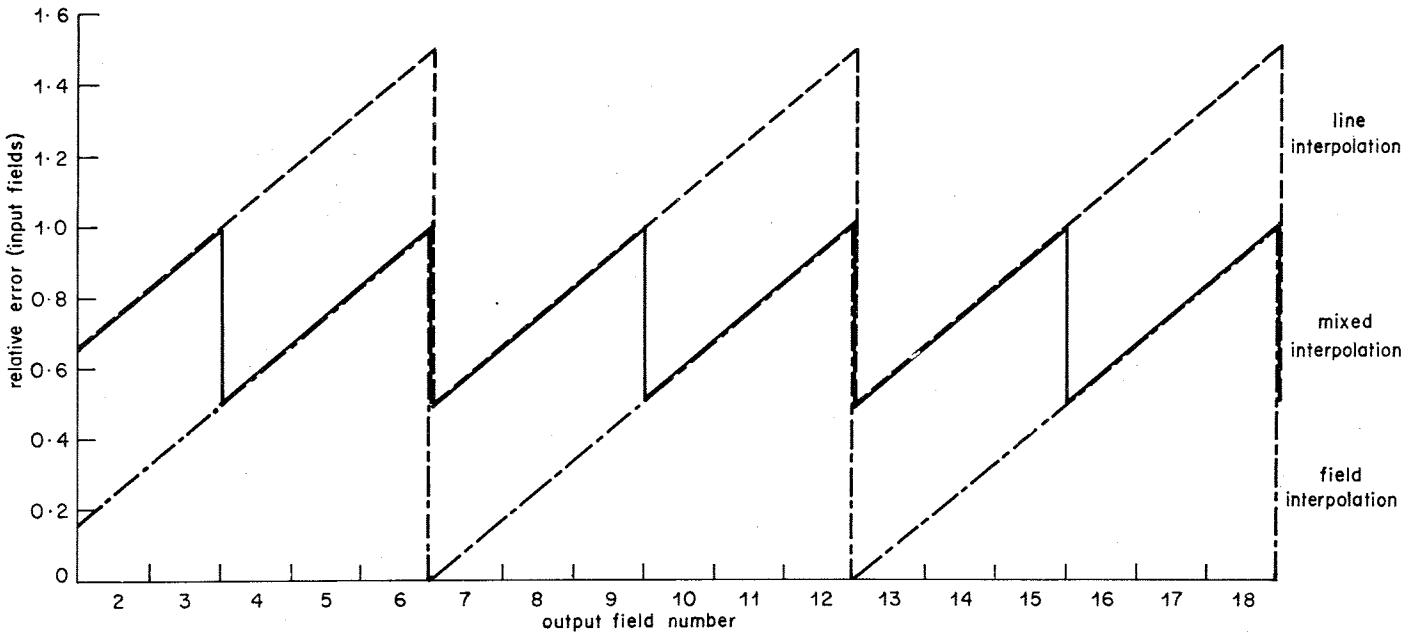


Fig. 4 - Movement interpolation: error in mean position of a moving object

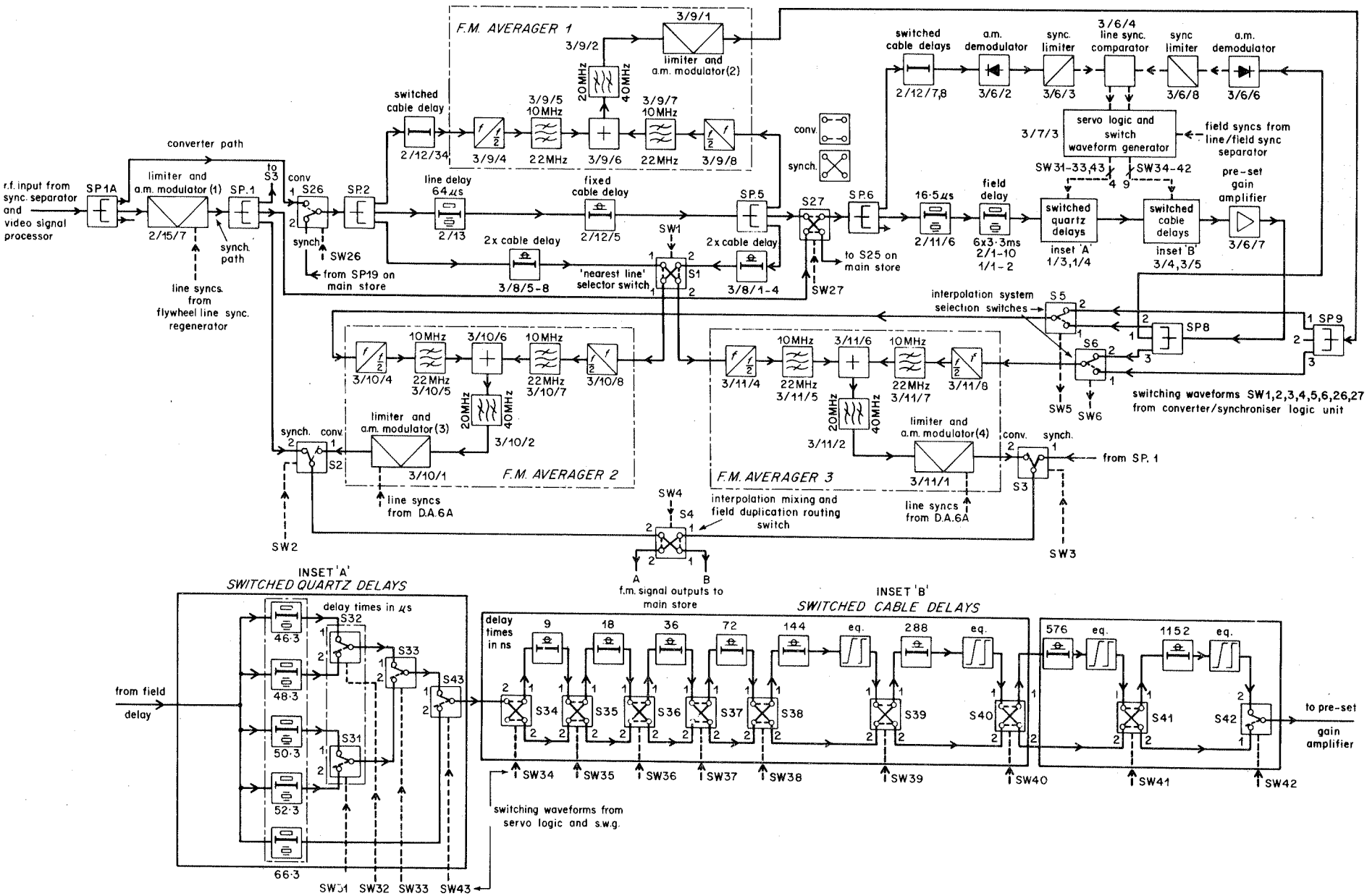


Fig. 5 - Interpolator and field delay: block diagram

It is necessary to convert every five input fields into six output fields and this is done by repeating every fifth input field. Those to be repeated are shown on output A and are each labelled 'Extra Field', see Fig. 3(*c*). The main store has to insert these extra fields into the sequence at output B as indicated by the arrows. This can be done by creating gaps between fields 0 and 1, 5 and 6, 10 and 11 etc. and by reducing the field durations from 1/50 sec. to 1/60 sec. (more precisely 1/59·94 sec.). The reduction in field duration is achieved by discarding the redundant lines; this is accomplished in the main store, but it is first necessary to understand more fully the nature of the signals emerging from the interpolator.

If the main store merely duplicated every fifth field, a one-line vertical hop would be seen on the output picture every time a duplicate field occurred. This is because the normal interlace sequence of odd field followed by even field etc. would be disturbed by two successive odd fields, or two successive even fields. Clearly, this disturbance can be anticipated, and it is possible to choose an interpolation selection sequence which will produce either an odd or even field at the output, whichever is required, and irrespective of whether the input field is odd or even. As was explained in Section 3 the interpolator can, in fact, simultaneously produce both odd and even versions of the same field at its two outputs. Hence for example, field number 5 is even at A and odd at B. Since field number 6 at A is eventually to be inserted between fields 5 and 6 at B, the interlace sequence after conversion is left uninterrupted.

It will also be seen that unlike the earlier C06/508 converter, it is possible with this design of interpolator to have both line and field interpolation available simultaneously at the two outputs. This is necessary because, for movement interpolation, the change from field interpolation to line interpolation should be phased to occur between the field to be repeated, and its repetition; this is seen in Fig. 4. Hence there are, for example, two differently interpolated fields number 6 (Fig. 3) which become two successive output fields, one of even interlace with field interpolation and one of odd interlace with line interpolation. The maintenance of correct interlace and interpolation is the function of switches S1 and S4.

Fig. 6 shows the 50T* section of the main store in the conversion mode, also the signals entering and leaving this section, and the waveforms controlling the switches. The 50T section may also be seen as part of the main store block diagram, shown in Fig. 7.

The inputs A and B are coupled to the outputs A and B of the interpolator. The signals at C and D are seen to have been converted into groups of lines of one field duration, overlapping one another on adjacent signal paths; the durations of the overlaps are all equal to 50T. It must be noted that although the beginnings and ends of these field groups do not normally correspond to the beginnings and ends of the fields, if these groups were to be arranged end to end, the fields would then be in the required sequence. It will be seen that each field is shown split into two regions, for example, 2 and 2′. The division between these regions marks the beginnings and ends of the overlapping field groups at the outputs C and D.

The remaining main store delays are arranged in the sequence 25T, 12T, 6T, 3T, 2T, 1T. Their function is to process the signals emerging from the 50T delay lines by distributing them among smaller-valued delay lines (arranged in order of decreasing magnitude) so that, ultimately, 50 redundant television lines appear at one (unwanted) output, and the required parts of the signal in correct order appear at another output. As illustrated in block diagram Fig. 7 the changes in signal routing are performed by transposing switches placed between the delay lines; each switch gives straight- or cross-connection from two inputs to two outputs whereby the signal is passed through the delay lines or via direct paths as required.

Fig. 8 shows in detail how a signal lasting for roughly one field period (produced by outputs C and D in Fig. 6 is compressed from 1/50 sec. to 1/59·94 sec. by time separation and subsequent omission of 50 lines. In this diagram, each switching waveform is drawn immediately above the two rows of signal-sequence blocks representing the alternative outputs from the switch it controls. Periods between the graduations dividing the blocks are of (about) one television line duration;* the numbered rectangles show the lines which are selected for omission (i.e. the redundant lines).

The diagram illustrates how the signal-overlaps at each pair of main store switch outputs decrease in duration, but increase in number during the field period. Thus, there is only one overlap from Switch 16 (shown at the top right-hand side of Fig. 8) which is 50T in duration; an overlap of this duration occurs because the signal comes from the switched 50T delay lines shown in Fig. 6. Similarly, after each stage in the signal partition process involving the smaller-value delays, the signal overlaps have individual durations equal to the delay value for that stage and a total duration for the whole field period equal to (about) 50T. Ultimately, as shown by the two bottom rows, the wanted output (the selected input to Switch 22) comprises a continuous sequence of signals describing a complete television field of reduced duration appropriate to the output standard, while the 50 'overlaps' appearing at the unselected input are each of 1T duration and represent redundant information.

* The 'T' unit is a unit of delay, in this context approximately 66·3 μs, which is used as a convenient increment of delay in field store standards converters. It is, in general defined as

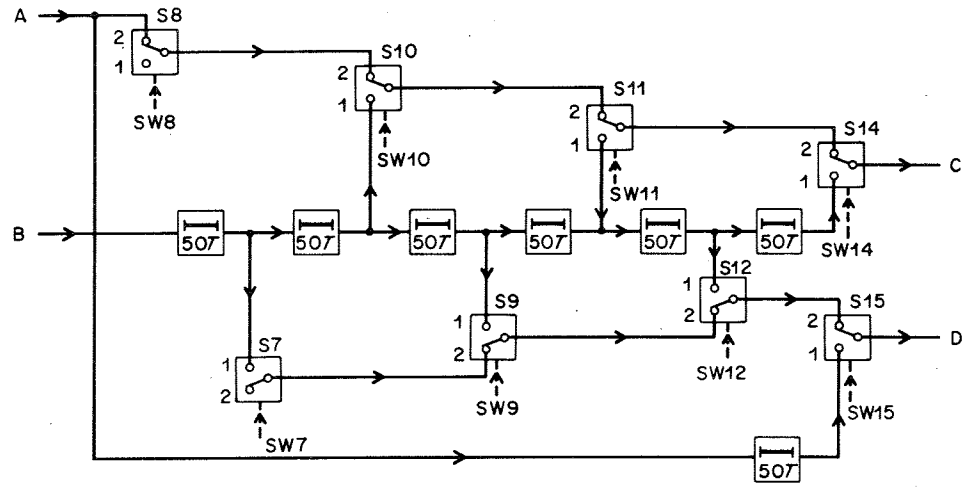
$$\left(\frac{F_1 - F_2}{N}\right), \text{ where:}$$

F_1 is the longer field duration of the two standards

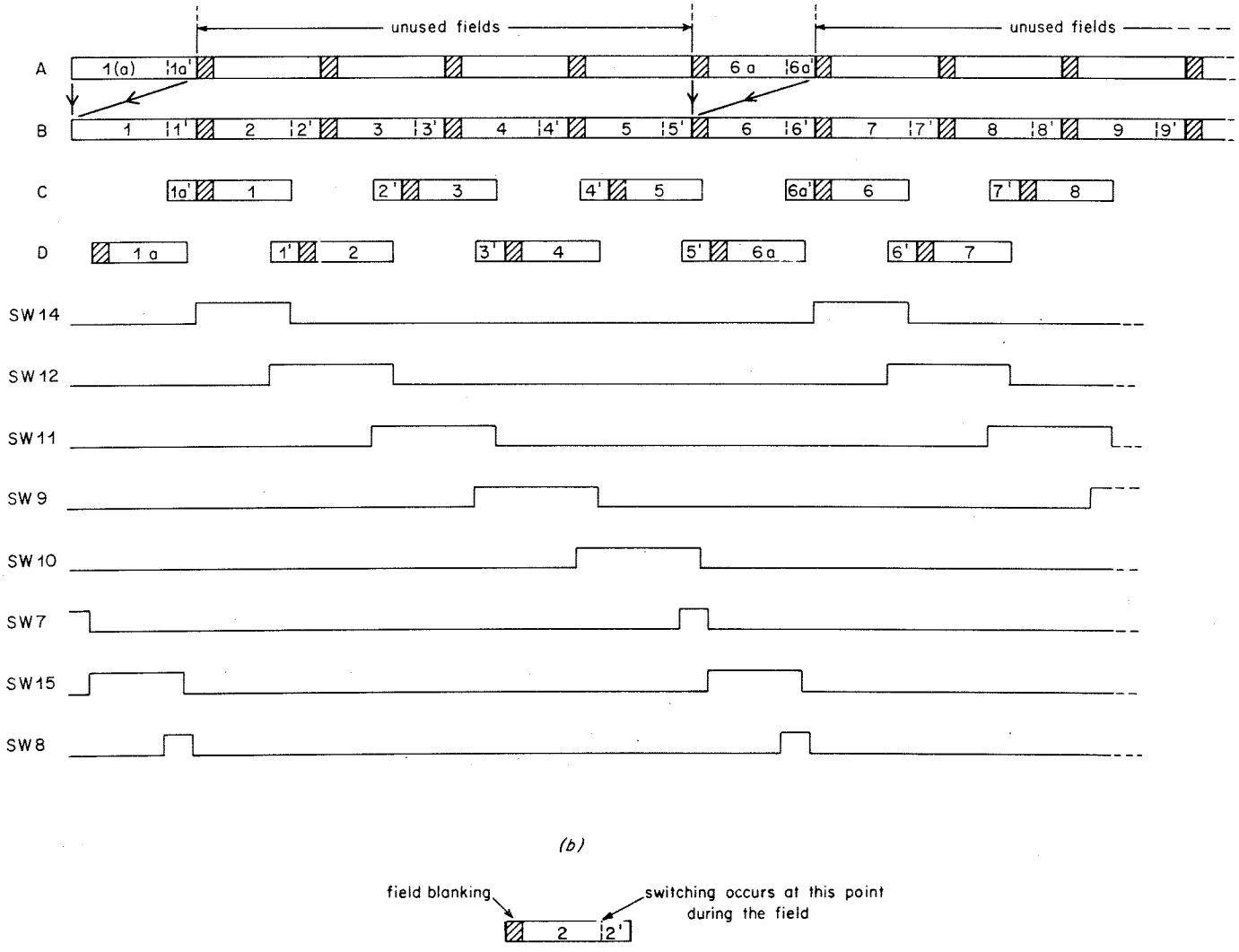
F_2 is the shorter field duration of the two standards

N is the difference between the number of lines per field of the two scanning standards.

* For simplicity, a slight approximation has been made in this drawing such that the durations of the T unit, the input-standard lines and the output-standard lines have been considered equal; in fact the durations are 66·3 μs, 64 μs and 63·5 μs, respectively. The differences are so small that it would not have been practicable to show them accurately with the scale used for this diagram. The validity of Fig. 8 is not affected by the approximation.

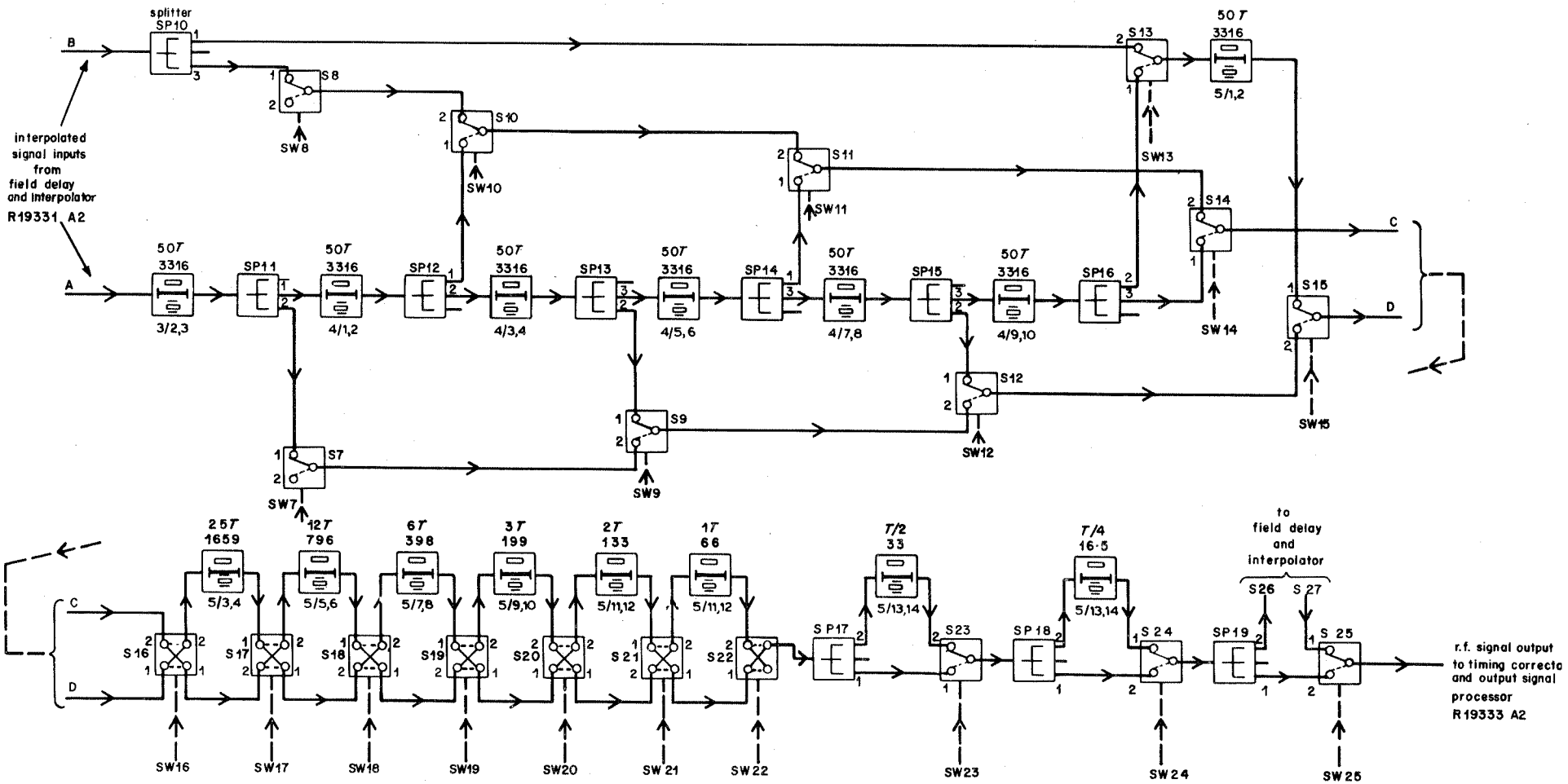


(a)



(b)

Fig. 6 - 50T section of main store, showing switching waveforms and resulting signals



Delay times in μs.

SW = switching waveform from converter/synchroniser logic unit

Fig. 7 - Main store block diagram

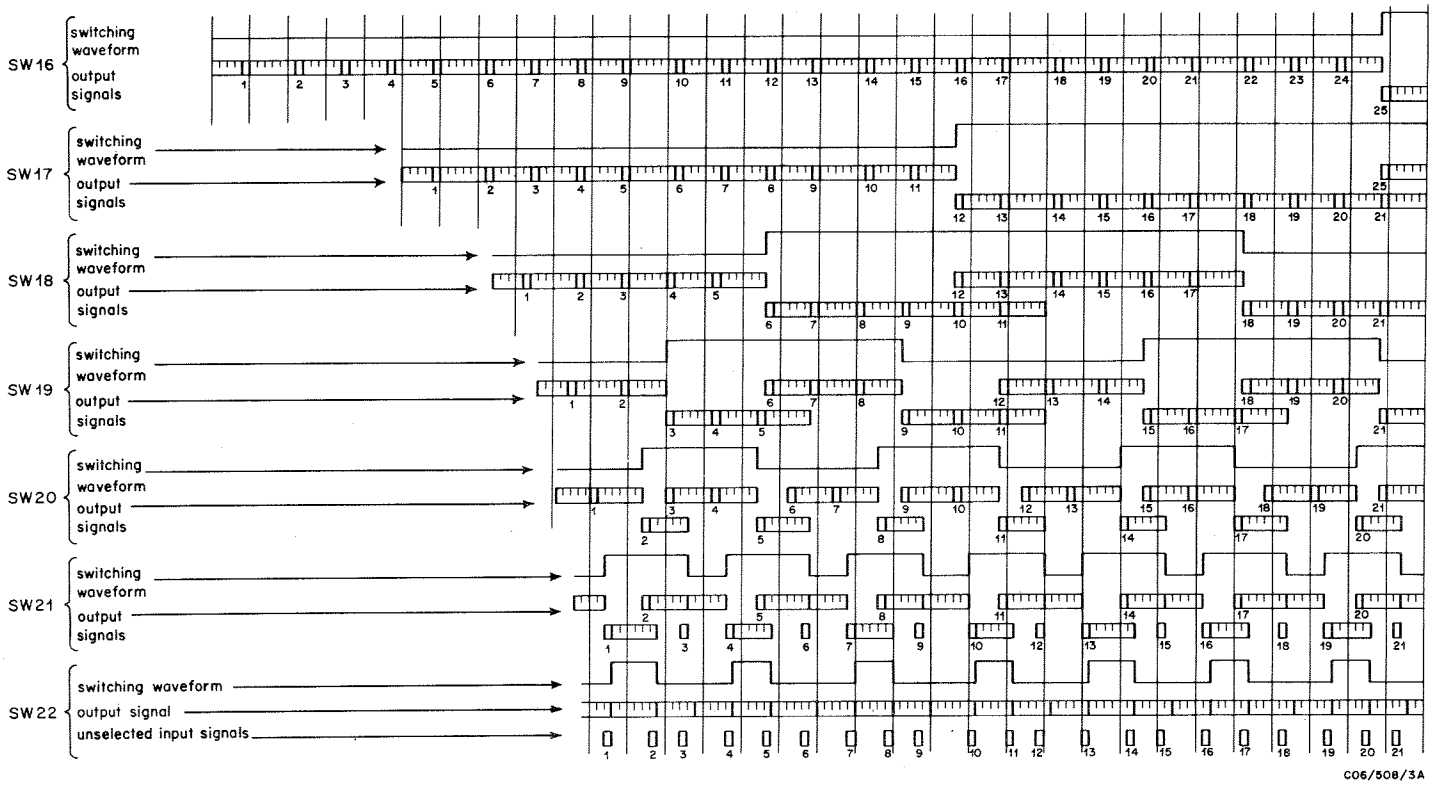


Fig. 8 - Signal partition process for approximately one field, with switching waveforms

4.2. The ½T and ¼T delays

These short delays, although shown on the main store block diagram Fig. 7 and although controlled by the main store logic play no part in the essential conversion process. It is usual to regard them as being a part of the timing corrector. Their function is to keep the timing of the signal which emerges from the main store in the middle of the range of Timing Corrector 1 (within a bracket of ¼T).

5. Main store logic

5.1. Design philosophy

Fig. 9 shows a possible relationship (one of an infinite number which can exist) between the converter input and output television fields. The frequency and phase of the output synchronising pulses are controlled by a local waveform generator which is in no way related to the input synchronising pulses. The relationship between the input and output synchronising pulses is therefore quite arbitrary.

Fig. 9 shows the input fields (of frequency 50 Hz) numbered 1 to 9 with arrows showing how they must be modified in timing and duration in order to fit into the framework provided by the output sync pulse generator.

From the diagram it will be seen that, in order to produce output fields numbered 1, 2, 3, 4 and 5, a variable signal delay is required. The derivation of output field number 6 is not so obvious, however, because the end of this field occurs before the end of input field number 6; in fact, output field number 6 must be derived from input field number 5. Most simply, this could be achieved by repeating the field number 5 after a suitable delay. In practice, interpolation is used in order to minimise the geometric picture distortion arising out of two successive identical fields. Conversion can be regarded as taking place in two stages.

Stage 1

At the beginning of each new field the delay in the main store is set to a value corresponding to the time lapse between the beginning of that field and the beginning of the output field which is to be constructed from it; i.e. in Fig. 9 this is represented by the time lapses such as AA′, BB′, CC′ etc.

Stage 2

During the course of a field, the total delay in the main store is systematically reduced in order to shrink the field duration from 1/50 sec. to 1/59·94 sec.

Since the logic unit controls the main store, it follows that the operation of the logic is similarly divided into two stages. First, the time lapses AA′, BB′, CC′, etc. have to be measured (by a device which we shall call the

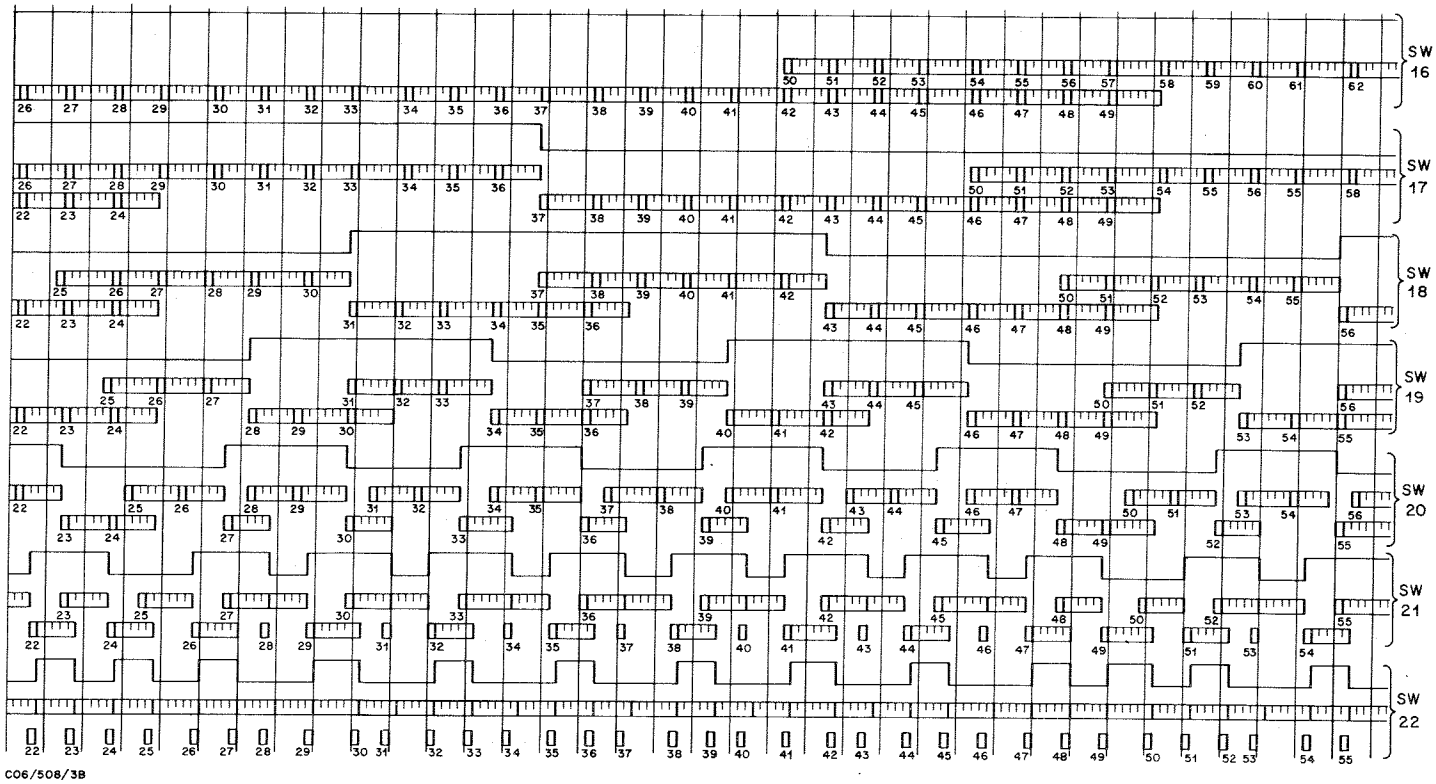


Fig. 8 (Cont'd)

'Field Sync Delay Clock') and the appropriate delay set up according to the results of the measurements, then the logic generates a family of waveforms designed to operate the switches controlling the main store delay. Since the values of the delays in the main store are multiples of a T unit (i.e. multiples of 66·3 μs), all the measurements made by the clock are obtained directly in multiples and binary sub-multiples of the T unit. This enables the logic to be directly coupled to the main store.

It would be of no practical use to make the measurements AA', BB', CC', etc. directly, since by the time the result were known, the signals would have to be just emerging from the delay whose value was being measured. In other words, the delay value is required to be known before the measurement can be made. This problem is surmounted by calculating the delay value in advance by measuring A'B, B'C, C'D etc. and the result subtracted from the known duration of the output field. This gives a prediction of the required delay in sufficient time to set up the main store to that value. This leads to some difficulty when field duplication becomes necessary. For example, the measurement D'E gives a prediction of the time lapse EE', and hence the correct delay for the beginning of output field No. 5, but the next measurement E'F gives a prediction for the time lapse FF', and not EF' as is required if field number 5 is to become field number 6 as well. Furthermore, the next measurement is F'G, or G'G, depending upon which field sync the logic unit uses to start its count. Neither of these measurements can give a prediction of FG', which is, of course, the delay needed to begin the conversion of input field number 6 into output field number 7. The problem is

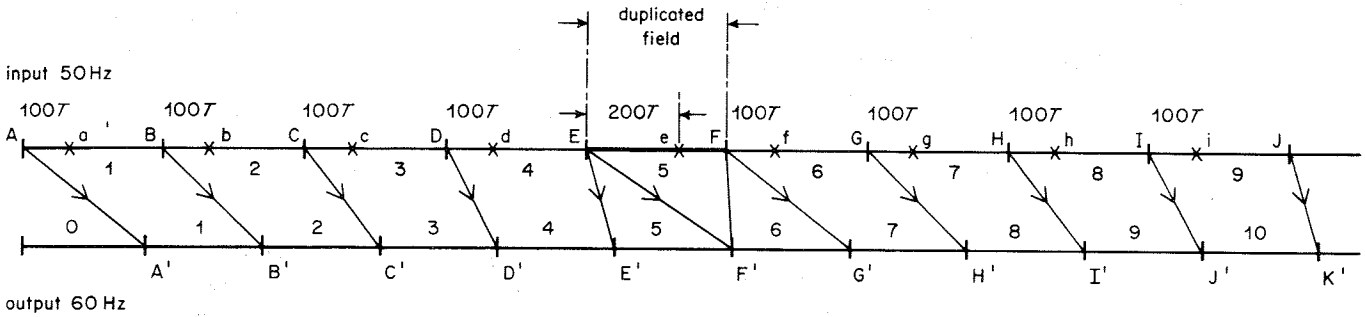


Fig. 9 - A possible relationship between converter input and output signals, showing the field which must be repeated

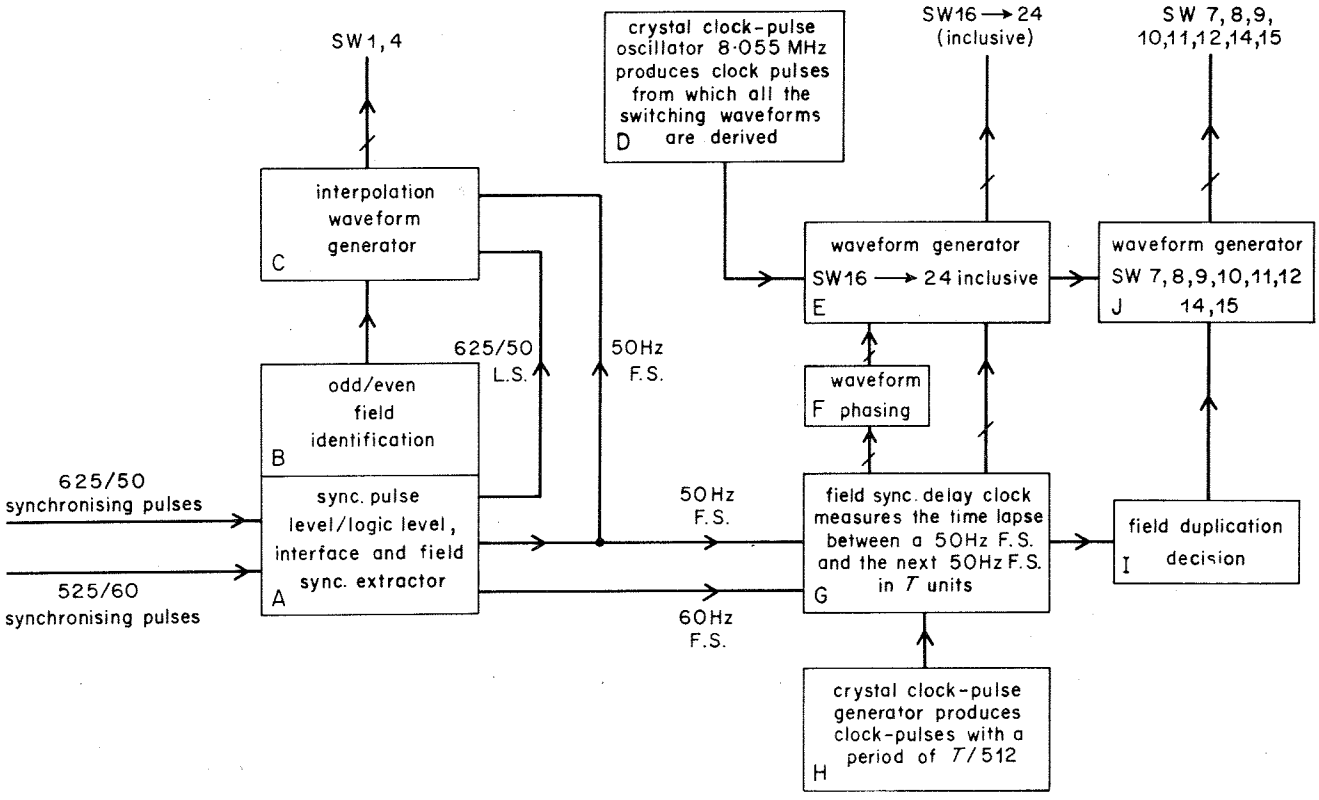


Fig. 10 - Main store logic: condensed block diagram

overcome by producing a pulse 100T units after every 50 Hz field sync, except for the one which precedes the duplicated field; in this special case the pulse occurs 200T after the field sync. The measurement of time lapse is then made either to the 50 Hz field sync or to the special pulse, whichever comes first. In this way, for example, D'E is measured quite normally as before, but E'F is never measured. E'e is measured instead of E'F, and likewise F'f is measured instead of F'G. This enables EF' and EG' to be deduced. The errors previously introduced by having measured to pulses delayed 100T and 200T from the field syncs can easily be compensated in the logic arithmetic circuits.

The criterion on which the decision to duplicate a field is based is whether or not the end of the converted field comes before the end of the field to be converted. For example, Field FG cannot be converted into field F'G' because G' is earlier than G. It therefore follows that output field F'G' must be formed by repeating field EF. The logic predicts from the measurements it makes when this condition is about to arise and generates a marker pulse which sets the field duplication process in operation.

5.2. Description of logic block diagram

With reference to Fig. 10, the main store switching waveforms SW7 to SW12 and SW14 to SW24, inclusive, are all derived by counters E and J from an 8·055 MHz crystal source D. The crystal provides an accurate clocking signal, the frequency* of which is made to follow variations in the input line frequency by means of a phase-locked loop.

Two conditions must be satisfied in waveform generators E and J at the beginning of every output field, these are:

1. The signals controlling switches should change state only during the line-blanking interval.
2. The delay value in the main store at the beginning of a new field, which is determined by the states of the field sync delay clock 'G' should be such as to position the beginning of the input field near enough to the beginning of the output field syncs to be within range of the Timing Corrector 1.

The first of these conditions is satisfied by the Waveform Phasing Circuit F, which ensures that the phase of waveform generator E is reset in such a way that logic transitions begin in the line blanking interval and continue

* The frequency of the crystal is defined by the formula

$$f_c = \frac{512 f_o \times f_i}{f_{ni}}$$

where f_c = crystal frequency
f_o = line frequency of output standard
f_i = actual line frequency of input standard
f_{ni} = nominal line frequency of input standard (i.e. 15,625 kHz)

to occur during line blanking throughout the field, subject to the stability of the 8·055 MHz crystal. The waveform phasing circuit F derives its information from measurements made by the field sync delay clock G. The second condition is satisfied by resetting waveform generator E to a value dictated by the Field Sync Delay Clock G. It will be recalled from Section 5.1 that the Field Sync delay clock measures the time lapse between input and output field sync pulses and hence determines the necessary delay required in the main store at the beginning of each field.

Waveform generator E produces the switching waveforms for the switches controlling the 25T, 12T, 6T, 3T, 2T, 1T, ½T and ¼T delays, whilst waveform generator J produces the switching waveforms for the tapped 50T section of the main store. It is locked by the output of waveform generator E, and is reset by the field duplication decision pulse produced by circuit I. (Field duplication is achieved by resetting the 50T delays from a delay of zero to a delay of one field period.)

The interpolation waveform generator C is responsible for generating SW1 and SW4, which it derives from input line and field synchronising pulses. Interlace is maintained at the field duplication point by using an odd/even field identification waveform generated by circuit B. Circuit A acts as an interface between the synchronising pulse circuits and logic circuits, and also extracts field synchronising pulses from the input synchronising pulse train.

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