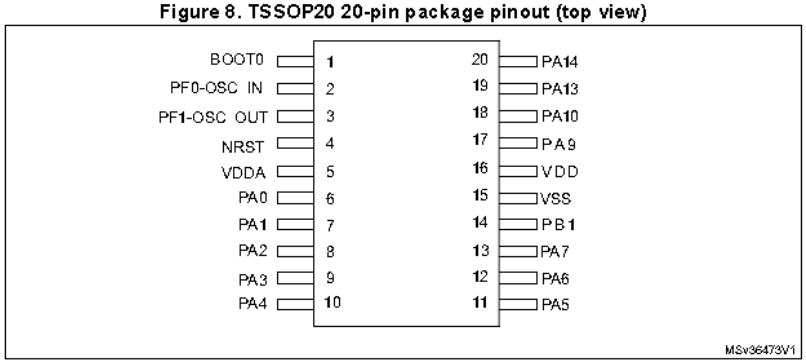
Figure 8. TSSOP20 20-pin package pinout (top view)



1 BOOT0	I	B	Boot memory selection
2 PF0-OSC_IN (PF0)	I/O	FT	I2C1_SDA[5] OSC_IN
3 PF1-OSC_OUT (PF1)	I/O	FT	I2C1_SCL[5] OSC_OUT
4 NRST	I/O	RST	Device reset input / internal reset output (active low)
5 VDDA	S		Analog power supply
6 PA0	I/O	TTa	USART1_CTS[2], USART2_CTS[3][5], USART4_TX[5] ADC_IN0, RTC_TAMP2, WKUP1
7 PA1	I/O	TTa	USART1_RTS[2], USART2_RTS[3][5], EVENTOUT, USART4_RX[5] ADC_IN1
8 PA2	I/O	TTa	USART1_TX[2], USART2_TX[3][5], TIM15_CH1[3][5] ADC_IN2
9 PA3	I/O	TTa	USART1_RX[2], USART2_RX[3][5], TIM15_CH2[3][5] ADC_IN3
10 PA4	I/O	TTa	SPI1_NSS, USART1_CK[2] USART2_CK[3][5], TIM14_CH1, USART6_TX[5] ADC_IN4
11 PA5	I/O	TTa	SPI1_SCK, USART6_RX[5] ADC_IN5
12 PA6	I/O	TTa	SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT USART3_CTS[5] ADC_IN6
13 PA7	I/O	TTa	SPI1_MOSI, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT ADC_IN7
14 PB1	I/O	TTa	TIM3_CH4, TIM14_CH1, TIM1_CH3N, USART3_RTS[5] ADC_IN9
15 VSS	S		Ground
16 VDD	S		Digital power supply
17 PA9	I/O	FT	USART1_TX, TIM1_CH2, TIM15_BKIN[3][5] I2C1_SCL[2][5]
18 PA10	I/O	FT	USART1_RX, TIM1_CH3, TIM17_BKIN I2C1_SDA[2][5]
19 PA13 (SWDIO)		I/O	FT [7] IR_OUT, SWDIO
20 PA14 (SWCLK)		I/O	FT [7] USART1_TX[2], USART2_TX[3][5], SWCLK

Pin type

S Supply pin, I Input only pin, I/O Input / output pin Functions selected through GPIOx_AFR registers

I/O structure

FT 5 V tolerant I/O, FTf 5 V tolerant I/O, FM+ capable, TTa 3.3 V tolerant I/O directly connected to ADC, TC Standard 3.3 V I/O, B Dedicated BOOT0 pin, RST Bidirectional reset pin with embedded weak pull-up resistor

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: - The speed should not exceed 2 MHz with a maximum load of 30 pF. - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. This feature is available on STM32F030x6 and STM32F030x4 devices only.
3. This feature is available on STM32F030x8 devices only.
4. For STM32F030x4/6/8 devices only.
5. For STM32F030xC devices only.
6. On LQFP32 package, PB2 and PB8 should be treated as unconnected pins (even when they are not available on the package, they are not forced to a defined level by hardware).
7. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on SWDIO pin and internal pull-down on SWCLK pin are activated.