

VACUUM FLUORESCENT DISPLAY  
MODULE  
SPECIFICATION

MODEL : GU120X32-300

SPECIFICATION NO. : DS-417-0000-02

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This specification is subject to change without prior notice.

**1. General Description**

Application : Data terminal, multi-purpose information system, etc.

Construction : Single board display module with a Vacuum Fluorescent Display consist of 120X32 dot matrix, refresh memories, control logics, and DC/DC convertor.

**2. Absolute Maximum Ratings**

Power Supply Voltage (V<sub>CC</sub>) : +7.0 V<sub>DC</sub>

Logic Input Voltage (V<sub>IH</sub>) : V<sub>CC</sub> + 0.3 V<sub>DC</sub>

**3. Electrical Ratings**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V <sub>CC</sub>	4.75	5.00	5.25	V <sub>DC</sub>

**4. Electrical Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	
Logic Input Voltage	H	V <sub>IH</sub>	2.2		V <sub>CC</sub>	V <sub>DC</sub>	V <sub>CC</sub> = 5.0 V
	L	V <sub>IL</sub>	0		0.8	V <sub>DC</sub>	V <sub>CC</sub> = 5.0 V
Power supply current	I <sub>CC</sub>		700	1000	mA <sub>DC</sub>	V <sub>CC</sub> = 5.0 V All dots ON	

Power rising time must be less than 50ms.

Power supply current might be double of the above value at power on rush time.

**5. Optical Characteristics**

Dot formation : 120 x 32 dot  
 Dot Size : 0.45 mm x 0.50 mm (X x Y)  
 Dot Pitch : 0.60 mm x 0.65 mm (X x Y)  
 Active Display Area : 71.85 mm x 20.65 mm (X x Y)  
 Luminance : Min. 350 cd/m (100fL)  
 Color : Blue green

**6. Environmental Condition**

Operating Temperature : -10 ~ +65°C

Storage Temperature : -40 ~ +85°C

Operating Humidity : 20 ~ 80% ( no condensation )

**7. Mechanical Test Condition**

- Vibration : Frequency 10 → 55 → 10 Hz
- : Sweep time 1/2 Octave/Minute
- : Amplitude 2mm
- : Direction X, Y, Z, (3 directions)
- : Duration 30 minutes per each directions.
  
- Shock : Acceleration 40 G
- : Duration 9.0 msec.
- : Direction X, Y, Z, (3 directions)
- : No. of times 3 times per each directions.

No failure shall be found after the above test.

**8. Functions**

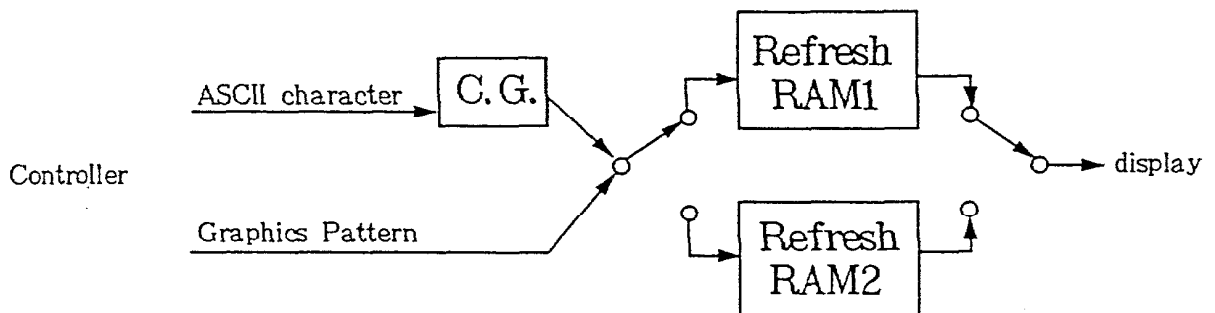
This module provides the functions of 8 bit parallel Data Write. Available character fonts are listed on the page 8 and 9. A data write is done during Busy line is low.

$\overline{WR}$	Function	Bus Direction
↓	Data Write	Host → Module

**8.1 Software module**

This display module has two set of refresh RAM. Each refresh RAM maintain one screen size display image. Either RAM is selected to send a image to the display.

This display module accepts blocks of data to control module and write characters or graphics image into the refresh RAM.



C.G. character Generator

**8.2 Structure of data block**

A data block consists of "Header", "Op code" and "Data".

"Header" + "Op code" + "Data"

01 Hex      1 Byte

"Header"    : 01 Hex

"Op Code" : Operation code which specify a type of "Data" such as Graphics, character and command.

"Data"     : Data block

**8.3 Op Code**

8.3.1 character write    Op Code : "C"

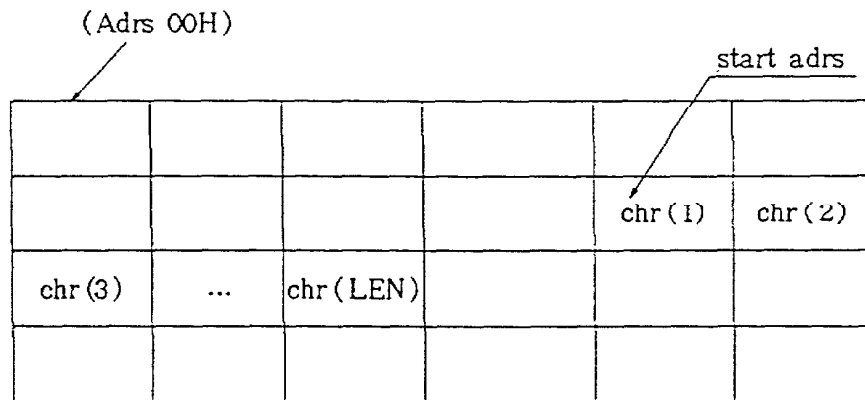
Format

(01 Hex) + ("C" 43 Hex) + Start ADRS + LEN + Write Mode  
   1 Byte     1 Byte     1 Byte  
 + chr(1) + chr(2) + ... + chr(LEN)

Description

Write ASCII characters into refresh RAM which is selected by command.

"Chr (1) is stored at "start ADRS".  
 "Chr (2) is stored at "start ADRS + 4"  
 In case the location over the refresh RAM size, next position is a left end of next lower line.



Write Mode

Display image (character font pattern) can be combined with Data in refresh RAM before stored into refresh RAM.

- "A" : RAM ← RAM .And. Chr Font
- "O" : RAM ← RAM .Or. Chr Font
- "E" : RAM ← RAM .Exor. Chr Font
- "S" : RAM ← Chr Font (Just Store)

8.3.2 Graphic Write Vertical Op Code : "G" 47Hex

Format

01 Hex + ("G" 47 Hex) + Start ADRS + LEN + Write Mode  
   2 Byte    2 Byte    1 Byte  
 + PT(1) + PT(2) + ... + PT(LEN)  
    Graphic pattern

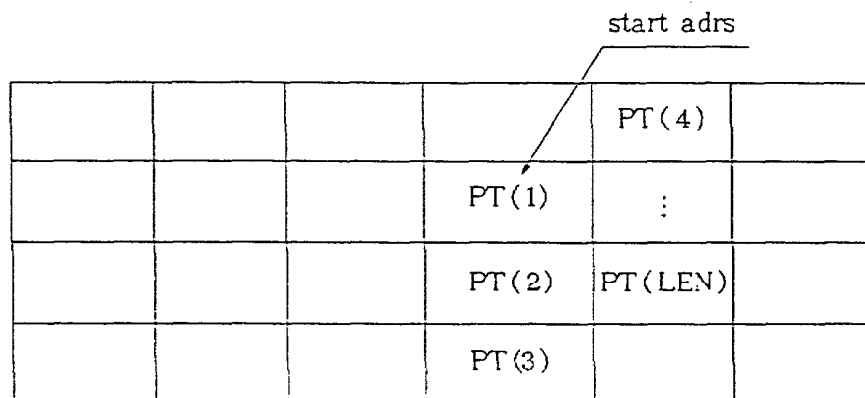
Description

Write Bit map pattern into refresh RAM which is selected by command.

PT(1) is stored at "start Adrs".

PT(2) is stored at "start Adrs + 1".

{ In case the location over the refresh RAM size,  
 next position is Address "00 Hex". }



Write Mode

Display image (Bit map Pattern) can be combined with Data in refresh RAM before stored into refresh RAM.

- "A" : RAM ← RAM .And. PT
- "O" : RAM ← RAM .Or. PT
- "E" : RAM ← RAM .Exor. PT
- "S" : RAM ← PT (Just Store)

8.3.3 Graphic Write Horizontal Op Code : "H" 48 Hex

Format

01 Hex + ("H" 48 Hex) + Start AdRS + LEN + Write Mode  
   2 Byte      2 Byte   1 Byte  
 + PT(1) + PT(2) + ... + PT(LEN)  
   Graphic pattern

Description

Write Bit map pattern into refresh RAM which is selected by command.

PT(1) is stored at "start Adrs".

PT(2) is stored at "start Adrs + 4".

{ In case the location over tehe refresh RAM size,  
 next position is left end of next lower Row. }

	PT(1)	PT(2)	—————> PT(N)
PT(NH) —————>			PT(LEN)

Write Mode

Display image (Bit map Pattern) can be combined with Data in refresh RAM before stored into the RAM.

- "A" : RAM ← RAM .And. PT
- "O" : RAM ← RAM .Or. PT
- "E" : RAM ← RAM .Exor. PT
- "S" : RAM ← PT (Just Store)

8.3.4 Control Code

Format

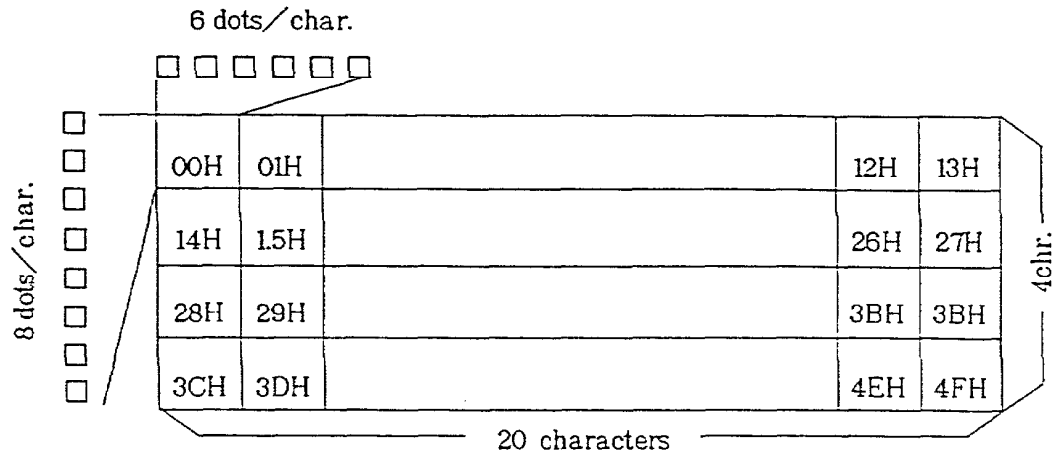
01 Hex + "O" 4F Hex + "command code"  
1 Byte

Description

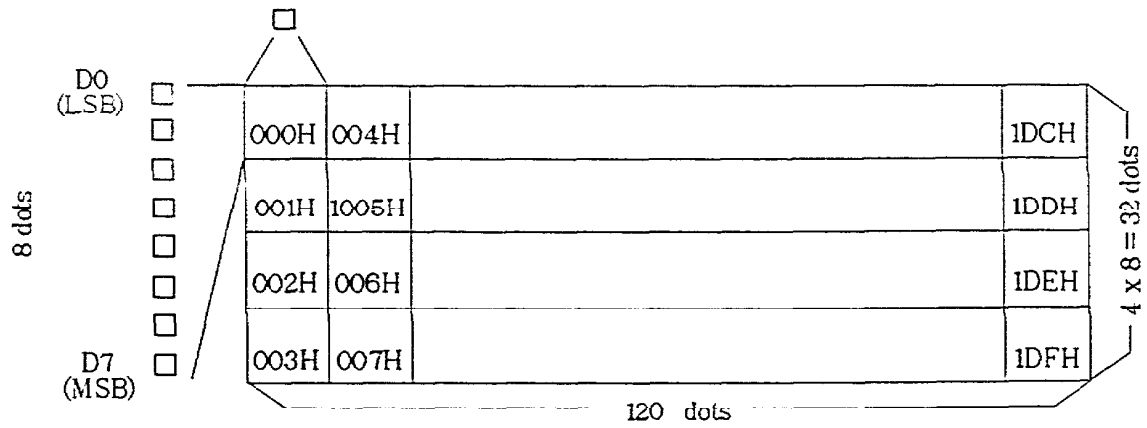
Command Code	
"D"	Display refresh RAM 1 (Default)
"E"	Display refresh RAM 2
"H"	Write refresh RAM 1 (Default)
"K"	Write refresh RAM 2
"L"	Clear refresh RAM 1
"M"	Clear refresh RAM 2
"P"	Clear refresh RAM 1 and 2
"Q"	Quick write
"R"	Flicker Less
"S"	Display off
"T"	Display ON (Default)
"a"	Luminance Control Maximun (Default)
⋮	⋮
"o"	Minimum
"0"	Select Character Table 0 (Default)
"1"	Select Character Table 1

8.4 Writing Position

A) Character Data Writing Position



B) Graphic Data Writing Position



1 : Turn on  
0 : Turn off



8.5 Character Table

The following 2 character tables are selected by command(see para 8.3.4).

8.5.1. International character

				D7 D6 D5 D4	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
D3	D2	D1	D0		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	0	1	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	0	1	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	1	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	1	0	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	1	1	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	1	1	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
1	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
1	0	0	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
1	0	0	1	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	0	1	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
1	0	1	0	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	0	1	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
1	0	1	1	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	1	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
1	1	0	0	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	1	0	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
1	1	0	1	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	1	1	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
1	1	1	0	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	1	1	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
1	1	1	1	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

Character Table 0(G68002)

8.5.2. Japanese(KATAKANA) character

		D7	D6	D5	D4	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111				
D3	D2	D1	D0																		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Character Table 0(G68003)

8.6 Data processing and Command Execution Time

Op Code & Function	Quick Write Mode			Flickerless Mode
	1st Byte	2nd~5th Byte	6th Byte~	
C Char. Write	30 $\mu$ s	35 $\mu$ s	75 $\mu$ s	See Note 1

Op Code & Function	Quick Write Mode			Flickerless Mode
	1st Byte	2nd~7th Byte	8th Byte~	
G H Graphic Write	30 $\mu$ s	35 $\mu$ s	50 $\mu$ s	See Note 1

Op Code & Function	Quick Write Mode		Flickerless Mode
	1st & 2nd Byte	3rd Byte	
D Disp. RAM 1	30 $\mu$ s	30 $\mu$ s	See Note 1
E Disp. RAM 2	30 $\mu$ s	30 $\mu$ s	
H WRI. RAM 1	30 $\mu$ s	30 $\mu$ s	
K WRI. RAM 2	30 $\mu$ s	30 $\mu$ s	
L CLR. RAM 1	30 $\mu$ s	500 $\mu$ s	
M CLR. RAM 2	30 $\mu$ s	500 $\mu$ s	
P CLR. RAM 1,2	30 $\mu$ s	1000 $\mu$ s	
Q Quick WR	30 $\mu$ s	35 $\mu$ s	
R Flickerless	30 $\mu$ s	35 $\mu$ s	
S Disp. OFF	30 $\mu$ s	40 $\mu$ s	
T Disp. ON	30 $\mu$ s	40 $\mu$ s	
a s o Lumi. Control	30 $\mu$ s	45 $\mu$ s	
0 Select. Chr. 0	30 $\mu$ s	30 $\mu$ s	
1 Select. Chr. 1	30 $\mu$ s	30 $\mu$ s	

Note 1 Under the "Flickerless Mode", Execution Time may be 2 to 4 Times longer than Quick Write mode.

It is recommended to check the BUSY Line under Flickerless Mode.

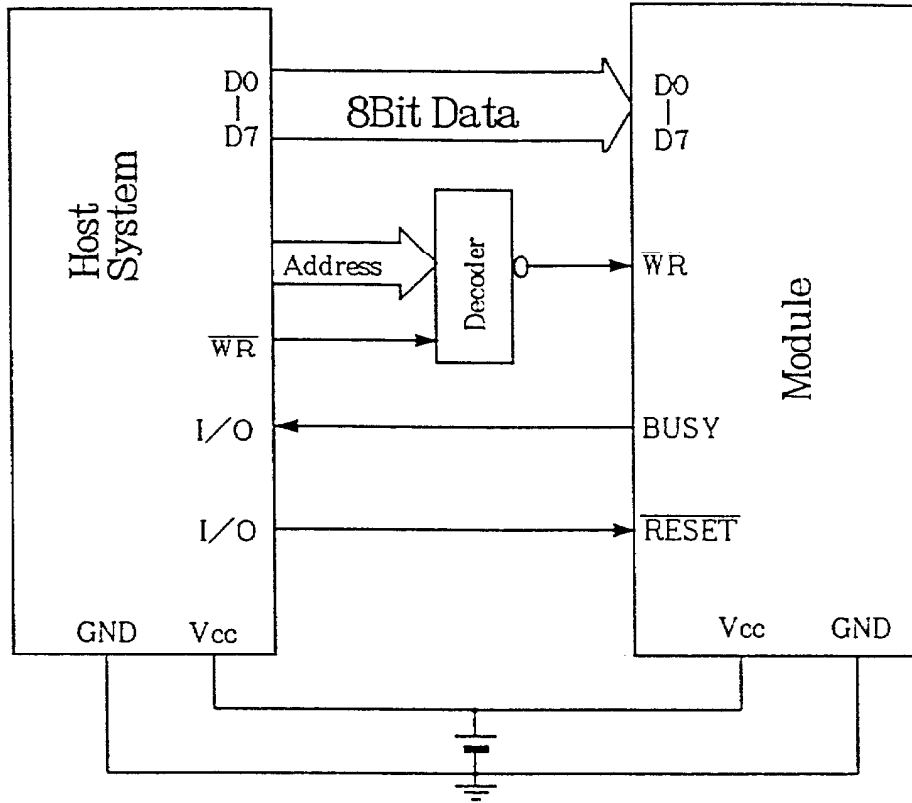
Note 2 Execution time is same as maximum of Tw (Busy Width).

9. Test Mode

Test Mode function is started when "To" is held at Low more than 100mSec. at power on.

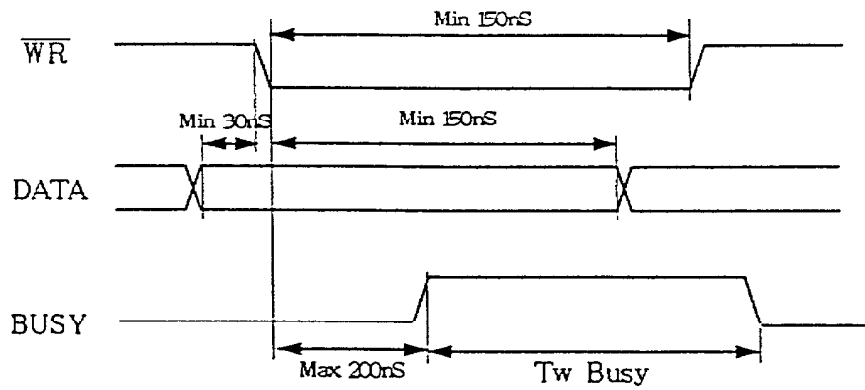
During Test Mode, all characters are displayed automatically and no any datas are accepted.

10 . Interfacing example



11. Timing

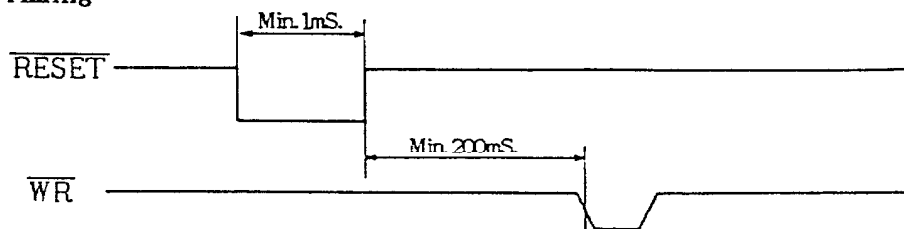
11.1 Write Timing



$T_w$  Busy : About 100 $\mu$ s with most data or Commands.

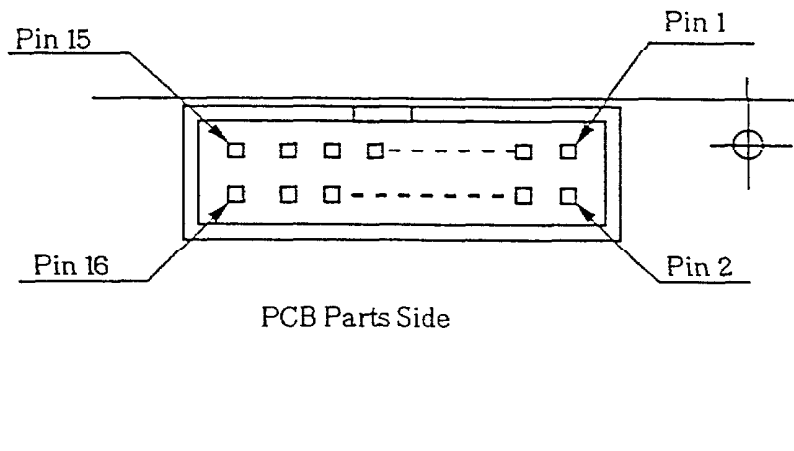
This figure will be confirmed on the specification.

11.2 Reset Timing



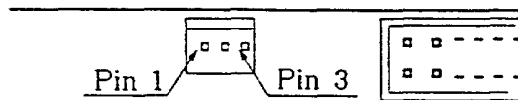
12. Pin Assignment

12.1 16 pin data connector



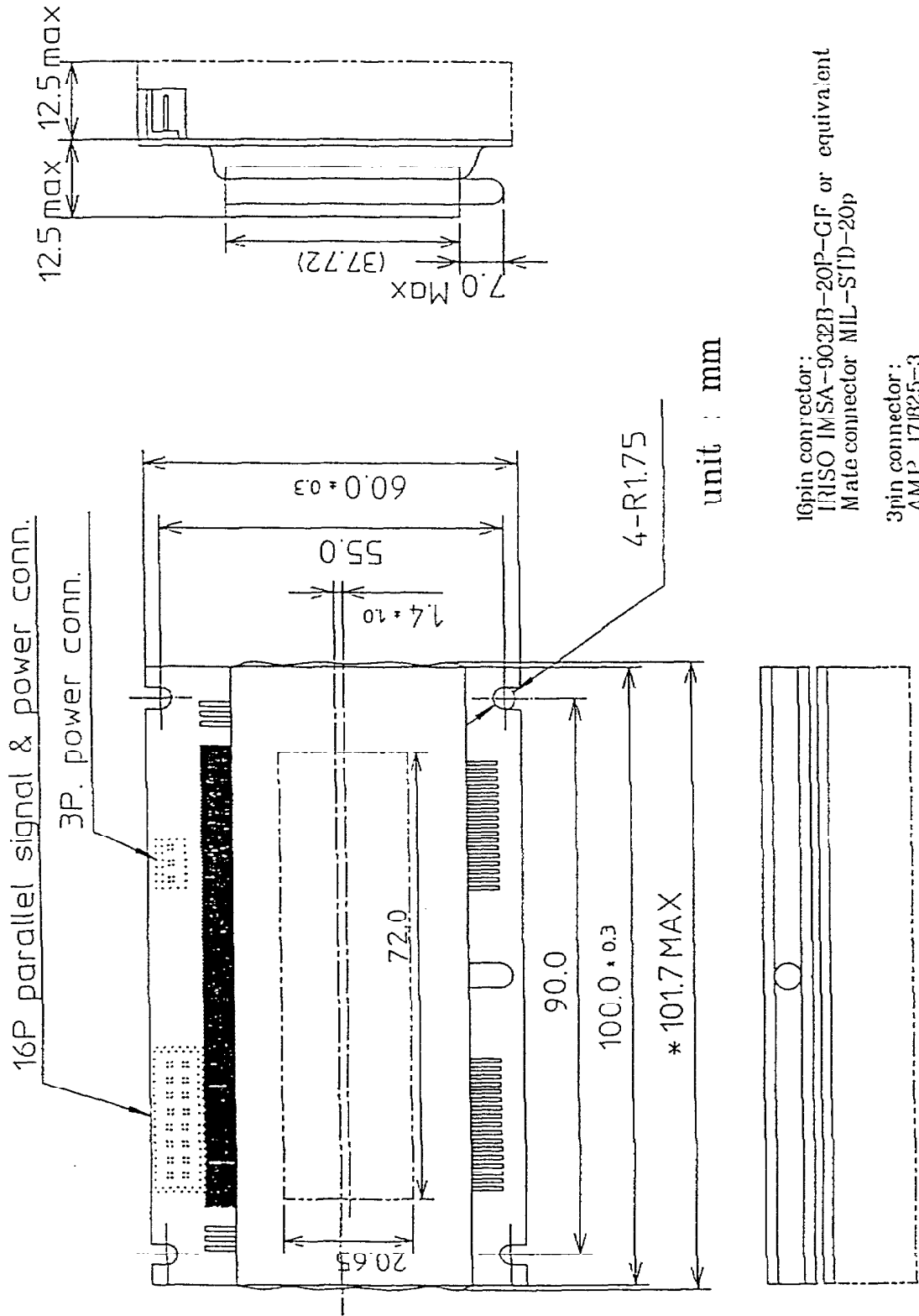
Pin No.	Signal	Pin No.	Signal
1	D7	2	D6
3	D5	4	D4
5	D3	6	D2
7	D1	8	D0
9	$\overline{WR}$	10	$\overline{RESET}$
11	To	12	BUSY
13	GND	14	GND
15	V <sub>cc</sub> (+5)	16	V <sub>cc</sub> (+5)

12.2 3 pin power connector



Pin No.	Description
1	+5V (V <sub>cc</sub> )
2	To
3	GND

13. Outline dimension



## IMPORTANT PRECAUTIONS

- \* All VFD Module contain MOS LSIs or ICs. Anti-Static handling procedures are always required.
- \* VF Display consists of Soda-lime glass. Heavy shock more than 40G, thermal shock greater than 10 °C/minute, direct hit with hard material to the glass surface -- especially to the EXHAUST PIPE -- may CRACK the glass.
- \* Do not PUSH the display strongly. At mounting to the system frame, slight gap between display glass face and front panel is necessary to avoid to contact failure of lead pins of display. Twist or warp mounting will make a glass CRACK around the lead pin of display.
- \* Neither DATA CONNECTOR nor POWER CONNECTOR should be connected or disconnected while power is applied.  
As is often the case with most subsystems, caution should be exercised in selectively disconnecting power within a computer based system. The modules receive high logic on strobe lines as random signals on all data ports. Removal of primary power with logic signals applied may damage input circuit.
- \* Stresses more than specification listed under the Absolute Maximum Ratings may cause PERMANENT DAMAGE of the modules.
- \* +5 volts power line must be regulated completely since all control logics are dependent on this line.  
Do not apply slow-start power. Provide sufficient output current power source to avoid trouble of RUSH CURRENT at power on. ( At least output current of double figure of  $I_{cc}$ , listed on the specification of each modules is required. )
- \* Do not place the module on the conductive plate just after the power off.  
Due to big capacitors on the module, more than 1 min. of discharging time is required to avoid the failure caused by shorting of power line.