General Description

FS6830 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications in sub 40W range. PWM switching frequency at normal operation is externally programmable and trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

The internal slope compensation improves system large signal stability and reduces the possible sub-harmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense(CS) input removes the signal glitch due to snubber circuit diode reverse recovery and thus greatly reduces the external component count and system cost in the design.

FS6830 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VDD over voltage clamp and under voltage lockout (UVLO). The Gate-drive output is clamped to maximum 18V to protect the power MOSFET. Excellent EMI performance is achieved with frequency shuffling technique together with soft switching control at the totem pole gate drive output. FS6830 is offered in SOT23-6 package.

Applications

- Battery Charger
- Power Adaptor for PDA and Digital Camera
- Set-Top Box Power Supplies
- Open-frame SMPS

Features

- Optimized for Sub 40W Applications
- Frequency Shuffling for Improved EMI
- Extended Burst Mode for Improved Efficiency and Low Standby Power
- Audio Noise Free Operation
- External Programmable PWM Switching Frequency
- Internal Synchronized Slope Compensation
- Low VDD Startup Current and Low Operating Current
- Leading Edge Blanking on Current Sense Input
- Over Load Protection(OLP) and Cycle-by-Cycle Current Limiting Protection(OCP)
- VDD Over Voltage Protection(OVP),Under Voltage Lockout Protection(UVLO) and Over Voltage Clamp
- Gate Output Maximum Voltage Clamp (18V)
- Pb-free SOT23-6 Package

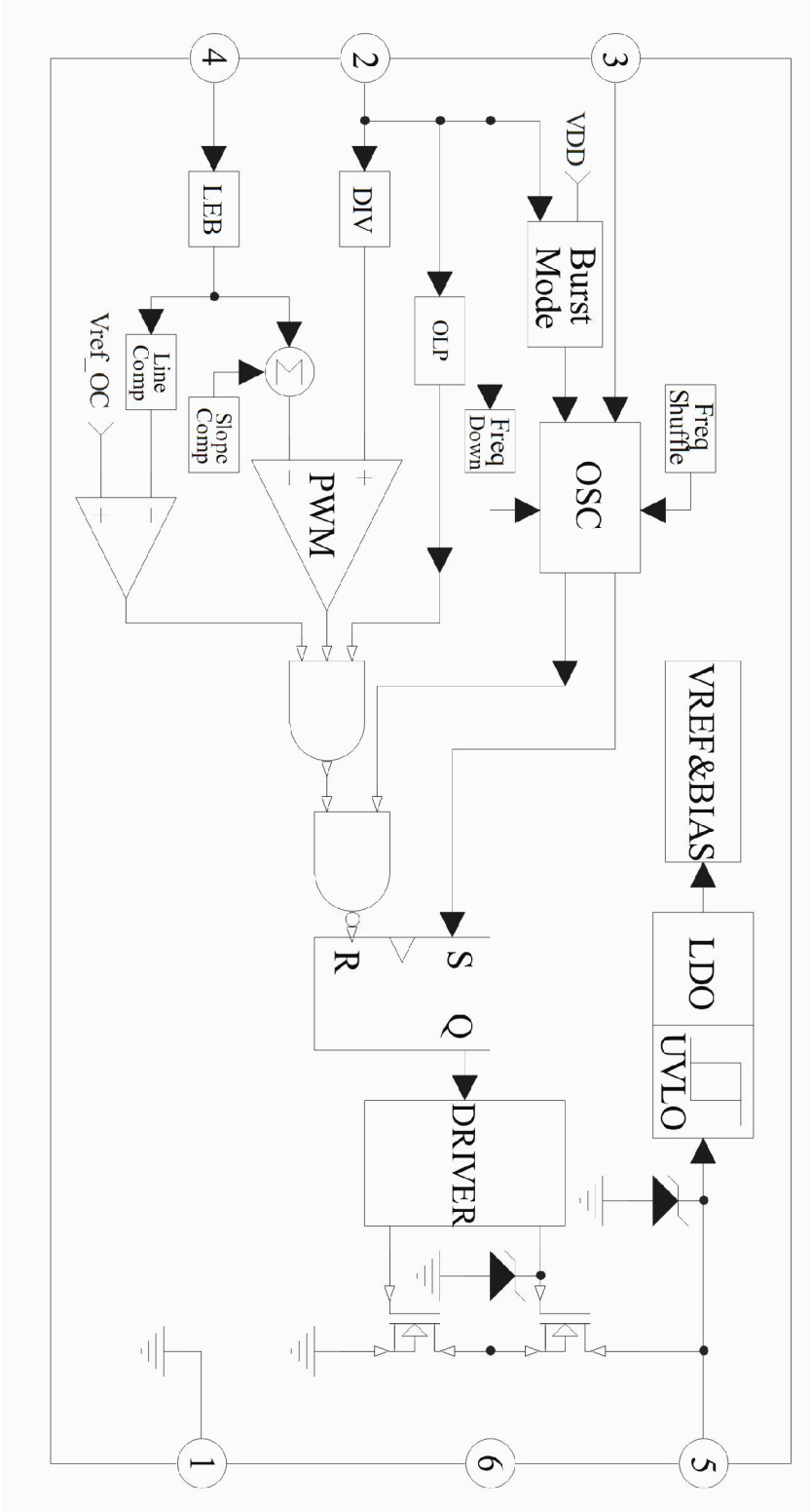
Absolute Maximum Ratings

Symbol	Description	Value	Unit
V_{DD}	VDD DC Supply Voltage	30	V
$V_{DD\_Clamp\_V}$	VDD Zener Clamp Voltage	34	V
$V_{DD\_Clamp\_I}$	VDD DC Clamp Current	10	mA
V_{FB}	VFB Input Voltage	-0.3~7	V
V_{RI}	VRI Input Voltage to RI Pin	-0.3~7	V
$T_{STORAGE}$	Storage Temperature	-55 to 160	℃

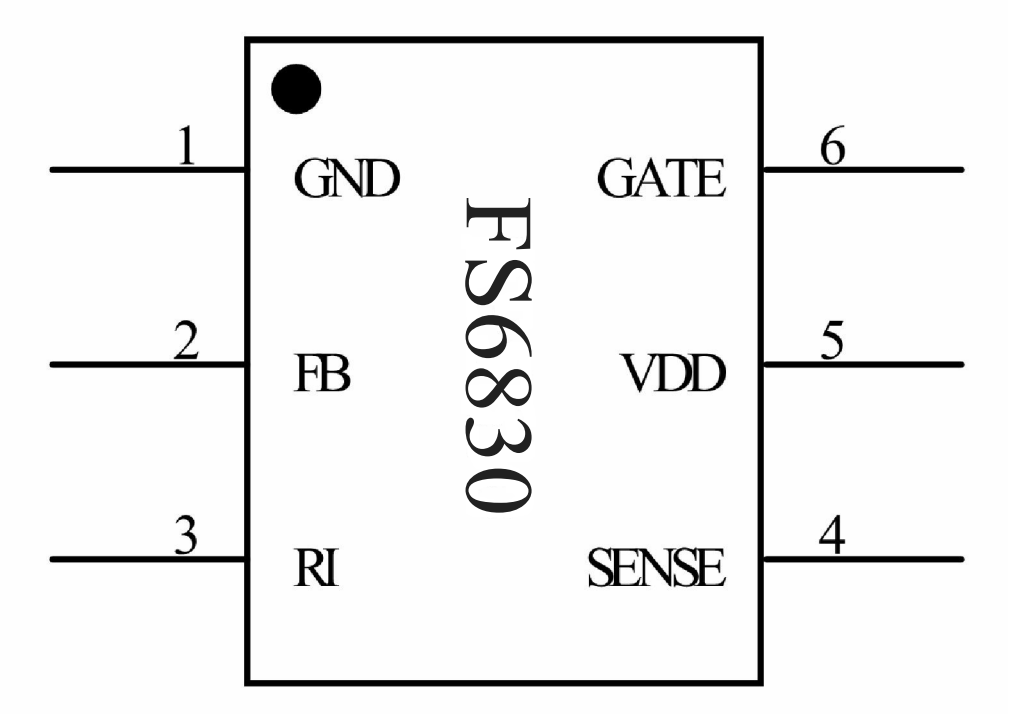
Recommended Operating Conditions

Symbol	Description	Value	Unit
V_{DD}	VDD DC Supply Voltage	10~25	V
T_A	Operating Ambient Temperature	-20~85	℃

Block Diagram



Pin Function Description



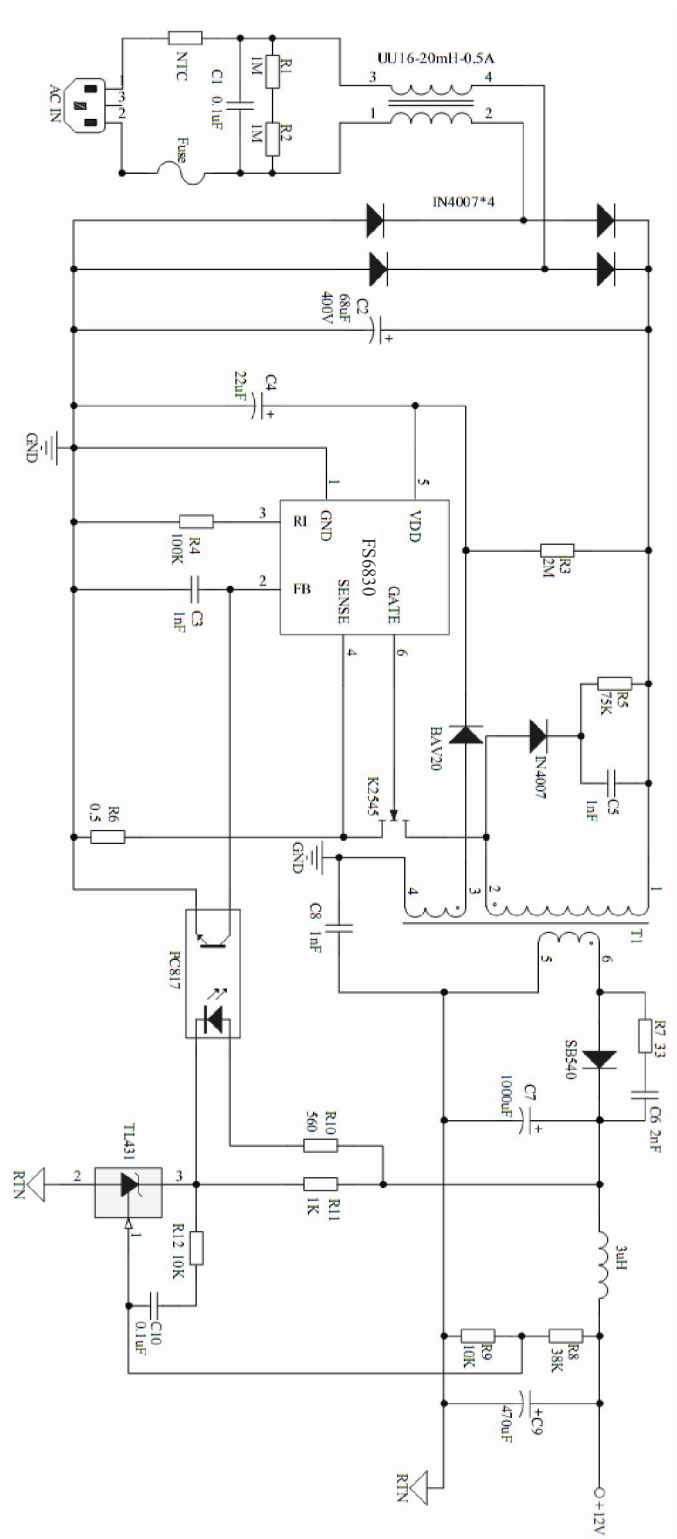
Pin No.	Pin Name	Function Description
1	GND	Ground
2	FB	Feedback input pin.
3	RI	Internal Oscillator frequency setting pin.
4	SENSE	Current sense input pin. Connected to MOSFET current sensing resistor node.
5	VDD	DC power supply pin
6	GATE	Totem-pole gate drive output for the power MOSFET.

Electrical Characteristics

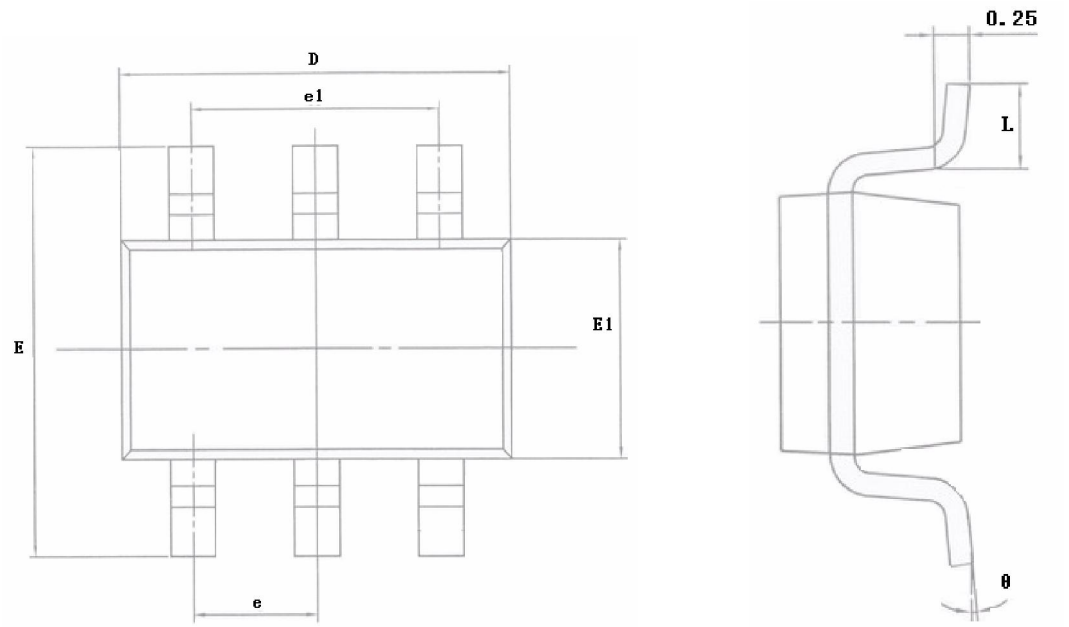
T_A=25℃,V_{DD}=16V, unless otherwise noted.

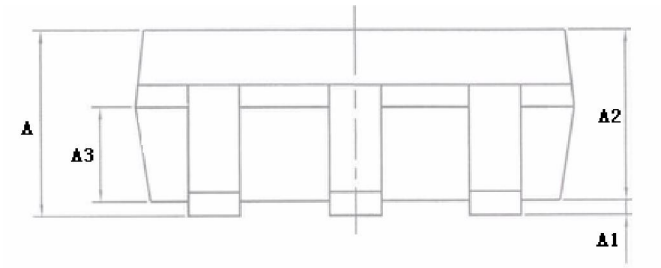
Symbol	Description	Test Conditions	Value			Units
			MIN	TYP	MAX	
I_{DD_ST}	VDD Start up Current	VDD=12.5V，RI=100KΩ，Measure current into VDD		3	20	uA
I_{OP}	Operation Current	VDD=16V,V_{FB}=3V，RI=100KΩ		1.4		mA
V_{DD_ST}	VDD Under Voltage Lockout Enter	VDD Rise	13	14	15	V
V_{UVLO}	VDD Under Voltage Lockout Exit	VDD Fall	7.8	8.8	9.8	V
V_{DD_CLAMP}	VDD Zener Clamp Voltage	I_{DD}=10mA		34		V
V_{FB_OPEN}	VFB Open Loop Voltage	V_{DD}=16V		4.8		V
I_{FB_SHORT}	FB pin short circuit current	V_{DD}=16V，Short FB to GND		1.2		mA
V_{TH_0D}	Zero Duty Cycle FB Threshold Voltage	V_{DD}=16V，RI=100KΩ，FB Fall until gate off			0.75	V
V_{TH_PL}	Power Limiting FB Threshold Voltage	V_{DD}=16V，RI=100KΩ，FB Fall until gate off		3.7		V
T_{LEB}	Leading edge blanking time	V_{DD}=16V，RI=100KΩ，FB Rise until gate off		300		nS
Z_{SENSE_IN}	Input Impedance			40		KΩ
V_{TH_OC}	Over Current Threshold Voltage at zero Duty Cycle	V_{DD}=16V ，RI=100KΩ，SENSE Rise until gate off	0.70	0.75	0.80	V
T_{D_OC}	Over Current Detection and Control Delay	V_{DD}=16V ，V_{FB}=3.0V，V_{CS}> V_{TH_OC}，RI=100KΩ		75		nS
F_{OSC}	Normal Oscillation Frequency	V_{DD}=16V ，V_{FB}=3.0V，V_{CS}=0V，RI=100KΩ	60	65	70	KHz
D_{MAX}	Maximum Duty Cycle	V_{DD}=16V ，V_{FB}=3.0V，V_{CS}=0V，RI=100KΩ		75		%
F_{BURST}	Burst Mode Base Frequency			22		KHz
ΔF_{OSC}	Frequency Modulation range	RI=100KΩ	-3		3	%
RI_{RANGE}	Operating RI Range		50	100	150	KΩ
V_{RI_OPEN}	RI open load voltage			2		V
V_{OL}	Output Low Level	V_{DD}=16V，I_O=-20mA			0.8	V
V_{OH}	Output High Level	V_{DD}=16V，I_O=20mA	10			V
Tr	Output Rising Time	VDD=16V，C_{LOAD}=1nF		220		nS
Tf	Output Falling Time	VDD=16V，C_{LOAD}=1nF		70		nS

Typical Application



Package Information（Unit:mm）





SYMBOL	MILLIMETER		
	MIN	NOR	MAX
A	-	-	1.35
A1	0.04	-	0.15
A2	1.00	1.10	1.20
A3	0.55	0.65	0.75
D	2.72	2.92	3.12
E	2.60	2.80	3.0
E1	1.40	1.60	1.80
e	0.95BSC		
e1	1.90BSC		
L	0.30	-	0.60
θ	0	-	8°

Operation Description

The FS6830 is a highly integrated PWM controller IC optimized for offline flyback converter applications in sub 40W power range. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

- **Startup Current and Start up Control**

Startup current of FS6830 is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet provides reliable startup in application. For AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and low power.
dissipation solution.

- **Operating Current**

The Operating current of FS6830 is low at 1.4mA. Good efficiency is achieved with FS6830 low operating current together with extended burst mode control features.

- **Frequency shuffling for EMI improvement**

The frequency Shuffling/jittering (switching frequency modulation) is implemented in FS6830. The oscillation frequency is modulated with a random source so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore reduces system design challenge.

- **Extended Burst Mode Operation**

At zero load or light load condition, majority of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. FS6830 self adjusts the switching mode according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level. Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend. The frequency control also eliminates the audio noise at any loading conditions.

- **Oscillator Operation**

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$F_{OSC} = \frac{6500}{RI(K\Omega)}(KHz)$$

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in FS6830 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to Snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

- **Internal Synchronized Slope Compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Gate Drive**

FS6830 Gate is connected to an external MOSFET gate for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI. A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

- **Protection**

Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO). The OCP threshold tracks PWM Duty cycles and is line voltage compensated to achieve constant output power limit over the universal input voltage range with recommended reference design. At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the output power MOSFET. Device restarts when VDD voltage drops below UVLO limit. VDD is supplied by transformer auxiliary winding output. It is clamped when VDD is higher than threshold value. The power MOSFET is shut down when VDD drops below UVLO limit and device enters power on start-up sequence thereafter.