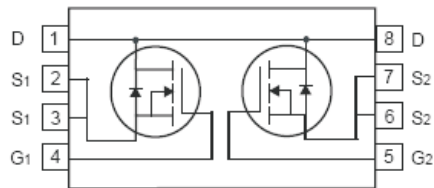


Dual N-Channel Enhancement Mode MOSFET

FEATURES

 $5A, 20V, r_{DS(on)} = 0.025 \Omega @ V_{GS} = 4.5V$
 $r_{DS(on)} = 0.040 \Omega @ V_{GS} = 2.5V.$

8205A
N-Channel MOSFET


Absolute Maximum Ratings (TA=25°C, unless otherwise noted)

Parameter	Symbol	Rating	Unit	
Drain-Source Voltage	V _{DS}	20	V	
Gate-Source Voltage	V _{GS}	±8	V	
Continuous Drain Current	I _D	5	A	
Pulsed Drain Current	I _{DM}	20	A	
Maximum Power Dissipation	P _D	TA = 25°C	2.0	W
		TA = 70°C	1.6	W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	78	°C/W	
Thermal Resistance, Junction-to-Case	R _{θJC}	40	°C/W	
Junction temperature and Storage temperature	T _j , T _{stg}	-55 to +150	°C	

8205A Electrical Characteristics (TA=25°C, unless otherwise noted)

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{DSS}	V _{GS} = 0 V, I _D = 250 μA	20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20V, V _{GS} = 0V			1	μA
		V _{DS} = 20V, V _{GS} = 0V, T _J = 55°C			5	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±8V			±50	nA
Gate Threshold Voltage	V _{GS(th)V}	V _{DS} = V _{GS} , I _D = 250μA	0.5		1.0	V
Drain-Source On-State Resistance *	r _{DS(on)}	V _{GS} = 4.5V, I _D = 5A		0.020	0.025	Ω
		V _{GS} = 2.5V, I _D = 4A		0.035	0.040	
On-State Drain Current *	I _{D(on)}	V _{DS} = 5V, V _{GS} = 4.5V	15			A
Forward Transconductance *	g _{fs}	V _{DS} = 5V, I _D = 3A		11		S
Input Capacitance	C _{iss}	V _{DS} = 10V, V _{GS} = 0V, f = 1.0 MHz		700		pF
Output Capacitance	C _{oss}			175		pF
Reverse Transfer Capacitance	C _{rss}			85		pF
Total Gate Charge	Q _g	V _{DS} = 10V, V _{GS} = 4.5V, I _D = 3A		7	10	nC
Gate-Source Charge	Q _{gs}			1.2		
Gate-Drain Charge	Q _{gd}			1.9		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10V I _D = 1A, V _{GS} = 4.5V, R _G = 6 Ω		8	16	ns
Rise Time	t _r			10	18	
Turn-Off Delay Time	t _{d(off)}			18	29	
Fall Time	t _f			5	10	
Maximum Continuous Drain-Source Diode Forward Current	I _S				1.3	A
Diode Forward Voltage *	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V		0.65	1.2	V

* Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.