9.2.3 Resistive Bridge Measurement

The device offers several features to ease the implementation of ratiometric bridge measurements (such as a PGA with gains up to 128, buffered, differential reference inputs, and a low-side power switch).

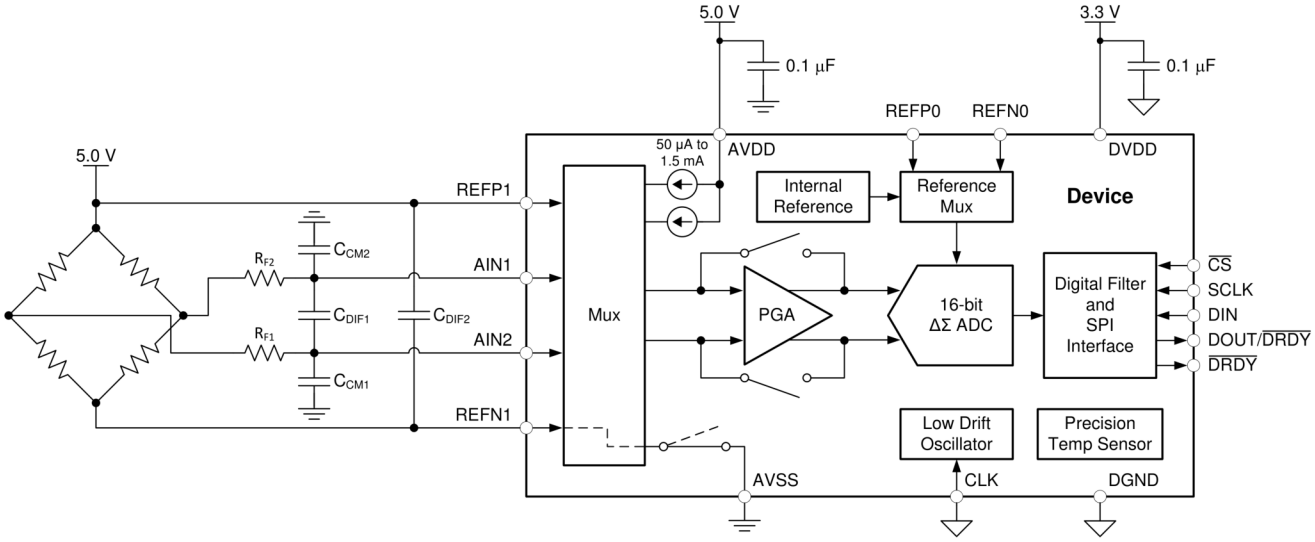

Figure 82. Resistive Bridge Measurement

9.2.3.1 Design Requirements

Table 25. Design Requirements

DESIGN PARAMETER	VALUE
Analog supply voltage	5.0 V
Digital supply voltage	3.3 V
Load cell type	4-wire load cell
Load cell sensitivity	2 mV/V
Excitation voltage	5 V
Noise-free counts	8000

9.2.3.2 Detailed Design Procedure

To implement a ratiometric bridge measurement, the bridge excitation voltage is simultaneously used as the reference voltage for the ADC; see Figure 82. With this configuration, any drift in excitation voltage also shows up on the reference voltage, consequently canceling out drift error. Either of the two device reference input pairs can be connected to the bridge excitation voltage. However, only the negative reference input (REFN1) can be internally routed to a low-side power switch. By connecting the low side of the bridge to REFN1, the device can automatically power-down the bridge by opening the low-side power switch. When the PSW bit in the configuration register is set to 1, the device opens the switch every time a POWERDOWN command is issued and closes the switch again when a START/SYNC command is sent.

The PGA offers gains up to 128, which helps amplify the small differential bridge output signal to make optimal use of the ADC full-scale range. Using a symmetrical bridge with the excitation voltage equal to the supply voltage of the device ensures that the output signal of the bridge meets the common-mode voltage requirement of the PGA.

Note that the maximum input voltage of ADS1120 is limited to $V_{IN\ (MAX)}$ = ±[(AVDD – AVSS) – 0.4 V] / Gain, which means the entire full-scale range, FSR = ±(AVDD – AVSS) / Gain, cannot be used in this configuration. This limitation is a result of the output drive capability of the PGA amplifiers (A1 and A2); see Figure 39. The output of each amplifier must stay 200 mV away from the rails (AVDD and AVSS), otherwise the PGA becomes nonlinear. Consequently, the maximum output swing of the PGA is limited to V_{OUT} = ±[(AVDD – AVSS) – 0.4 V].

Using a 2-mV/V load cell with a 5-V excitation yields a maximum differential output voltage of $V_{IN\ (MAX)}$ = ±10 mV, which meets Equation 42 when using a gain of 128.

$$V_{IN\ (MAX)} \le \pm[(AVDD - AVSS) - 0.4\ V] / Gain = \pm(5\ V - 0.4\ V) / 128 = \pm 36\ mV \quad (42)$$

A first-order differential and common-mode RC filter (R_{F1}, R_{F2}, C_{DIF1}, C_{CM1}, and C_{CM2}) is placed on the ADC inputs. The reference has an additional capacitor C_{DIF2} to limit reference noise. Care must be taken to maintain a limited amount of filtering or the measurement will no longer be ratiometric.

The device is capable of 16-bit, noise-free resolution using a gain of 128 at 20 SPS for the specified reference voltage. Accordingly the device is able to resolve signals as small as one LSB. The LSB size is calculated using Equation 43:

$$1\ LSB = (2 \cdot V_{ref} / Gain) / 2^{16} = (2 \cdot 5.0\ V / 128) / 2^{16} = 1.192\ \mu V \quad (43)$$

To find the total number of counts available for the bridge measurement, the maximum output voltage is divided by the LSB value. Dividing 10 mV by 1.192 µV equates to 8389 total counts available, which meets the design parameter of 8000 counts.

The register settings for this design are shown in Table 26.

Table 26. Register Settings

REGISTER	SETTING	DESCRIPTION
00h	3Eh	AIN_P = AIN1, AIN_N = AIN2, gain = 128, PGA enabled
01h	04h	DR = 20 SPS, normal mode, continuous conversion mode
02h	98h	External reference (REFP1, REFN1), simultaneous 50-Hz and 60-Hz rejection, PSW = 1
03h	00h	No IDACs used