SpyBiWire

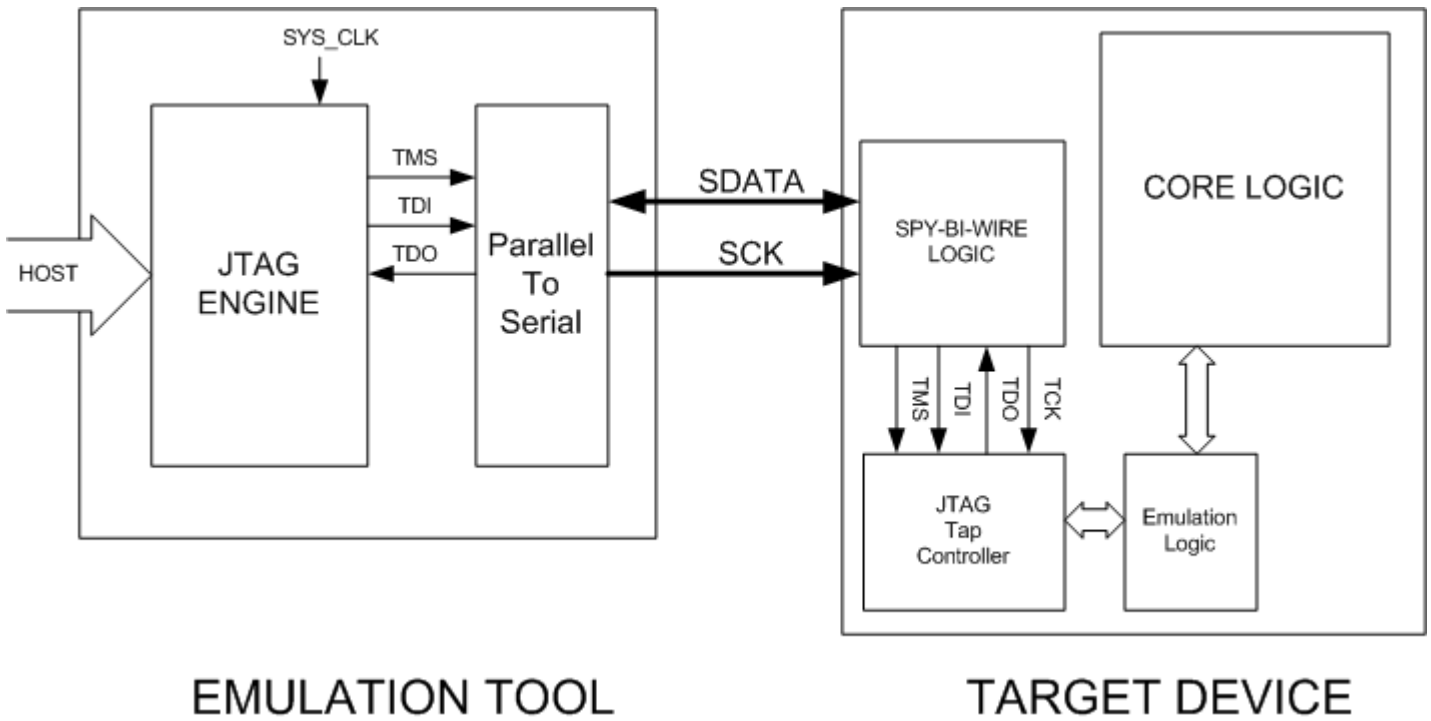
A new Emulation interface ?

JTAG versus SpyBiWire

SpyBiWire…

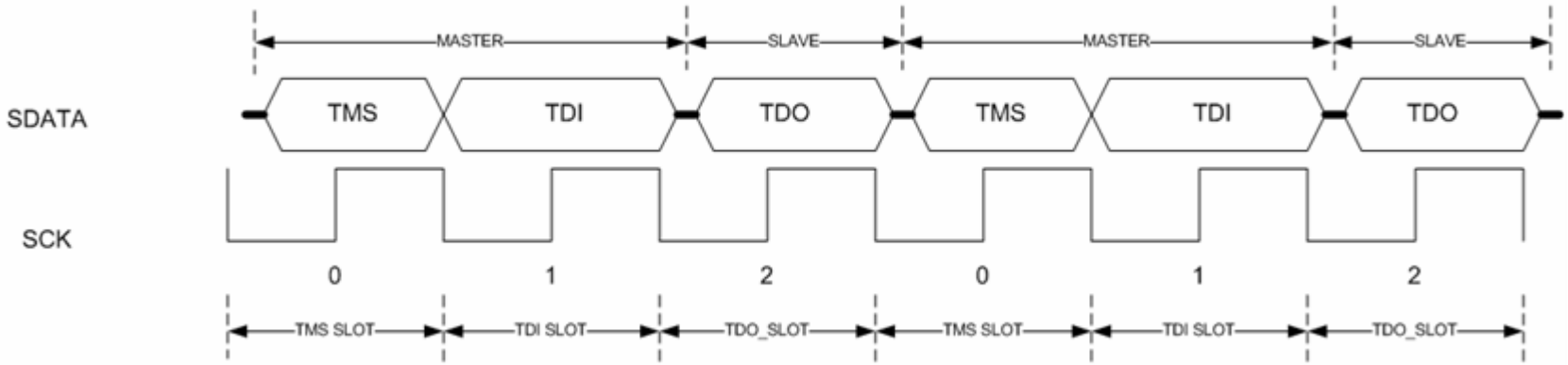
- does use the same protocol as JTAG just the way to transmit is different
- does need two pins – Jtag requires 4
- needs Entry Sequence to switch either to SpyBiWire or JTAG mode
- does not work with the Parallel Port FET due to timing issues
- is slower then JTAG because 3 lines are multiplexed on one

Block Diagram



SpyBiWire Protocol

- Clock signal SBWTCK is identical to TCK
- TDI / TMS and TDO are multiplexed on the data line SBWTDIO
- This means that the SBWTDIO is a bidirectional data line
- Timing limitation for SBWTCK: max low time: 15us
  -> Parallel FET could not support SpyBiWire



Connections

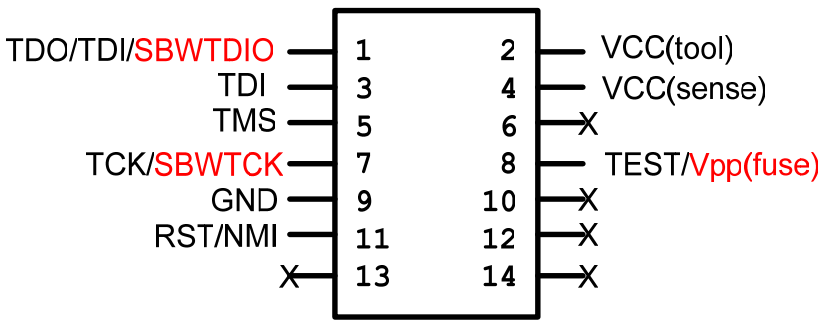
JTAG

- 4 / (5) Pins:
  TDI / TMS / TCK / TDO
  (TEST)

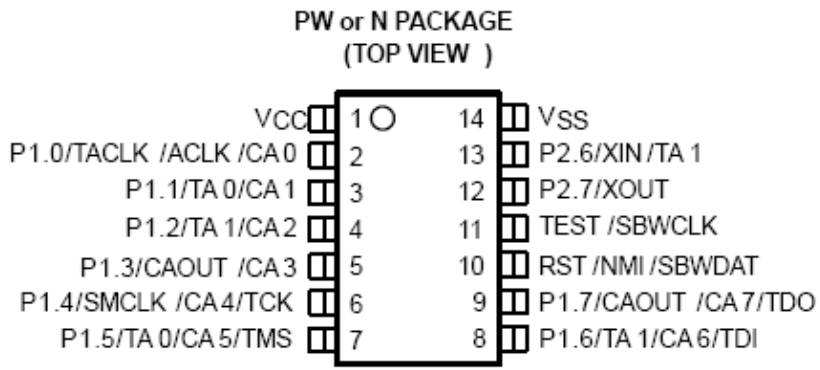
SpyByWire

- 2 Pins:
  RST/NMI and TEST

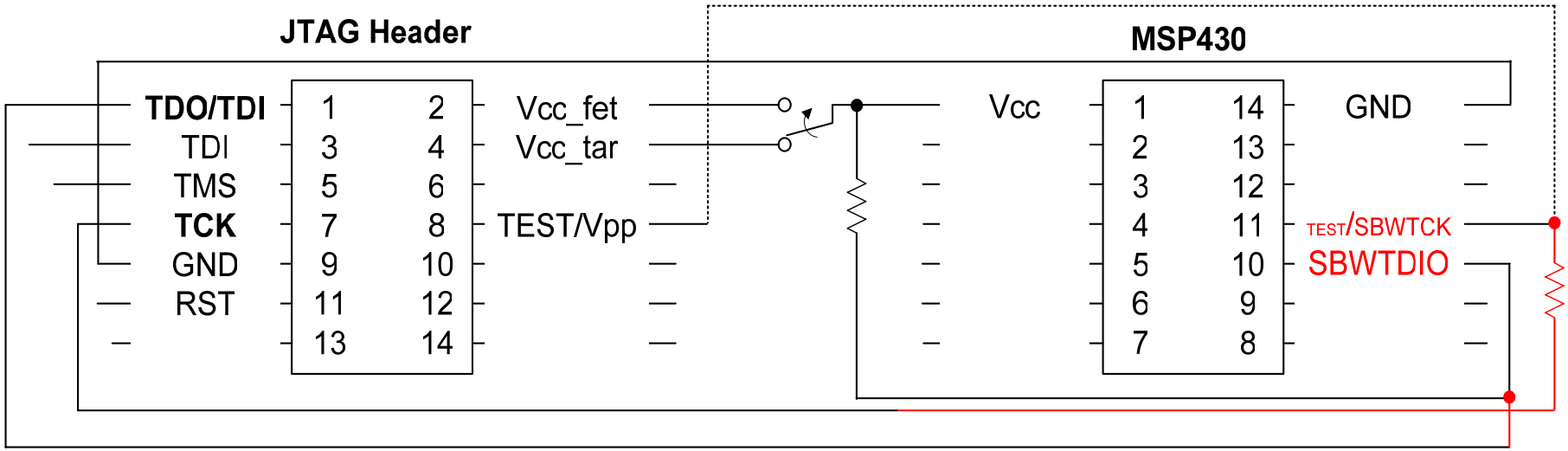
Header for Tools



Foot print of 14 pin Device



14-pin Header 2-wire connections



- TEST Connection & SBWTCK resistor optional for fuse blow

14-pin Header 4-wire connections

- old JTAG communication still could be used with following connections
- May be interesting for production programming to enhance speed