Section 17 ROM

17.1 Overview

The H8/532 includes 32K bytes of high-speed, on-chip ROM. The on-chip ROM is connected to the CPU via a 16-bit data bus and is accessed in two states.

Users wishing to program the chip themselves can request electrically programmable ROM (PROM). The PROM version of the H8/532 has a PROM mode in which the chip can be programmed with a standard, external PROM writer. The chip is also available with masked ROM.

The on-chip ROM is enabled or disabled depending on the MCU operating mode, which is determined by the inputs at the mode pins when the chip comes out of the reset state.
See table 17-1.

Table 17-1 ROM Usage in Each MCU Mode

	Mode Pins			
Mode	**MD_2**	**MD_1**	**MD_0**	**ROM**
Mode 1 (expanded minimum mode)	0	0	1	Disabled (external addresses)
Mode 2 (expanded minimum mode)	0	1	0	Enabled
Mode 3 (expanded maximum mode)	0	1	1	Disabled (external addresses)
Mode 4 (expanded maximum mode)	1	0	0	Enabled
Mode 7 (single-chip mode)	1	1	1	Enabled

17.1.1 Block Diagram

Figure 17-1 shows the block diagram of the on-chip ROM.

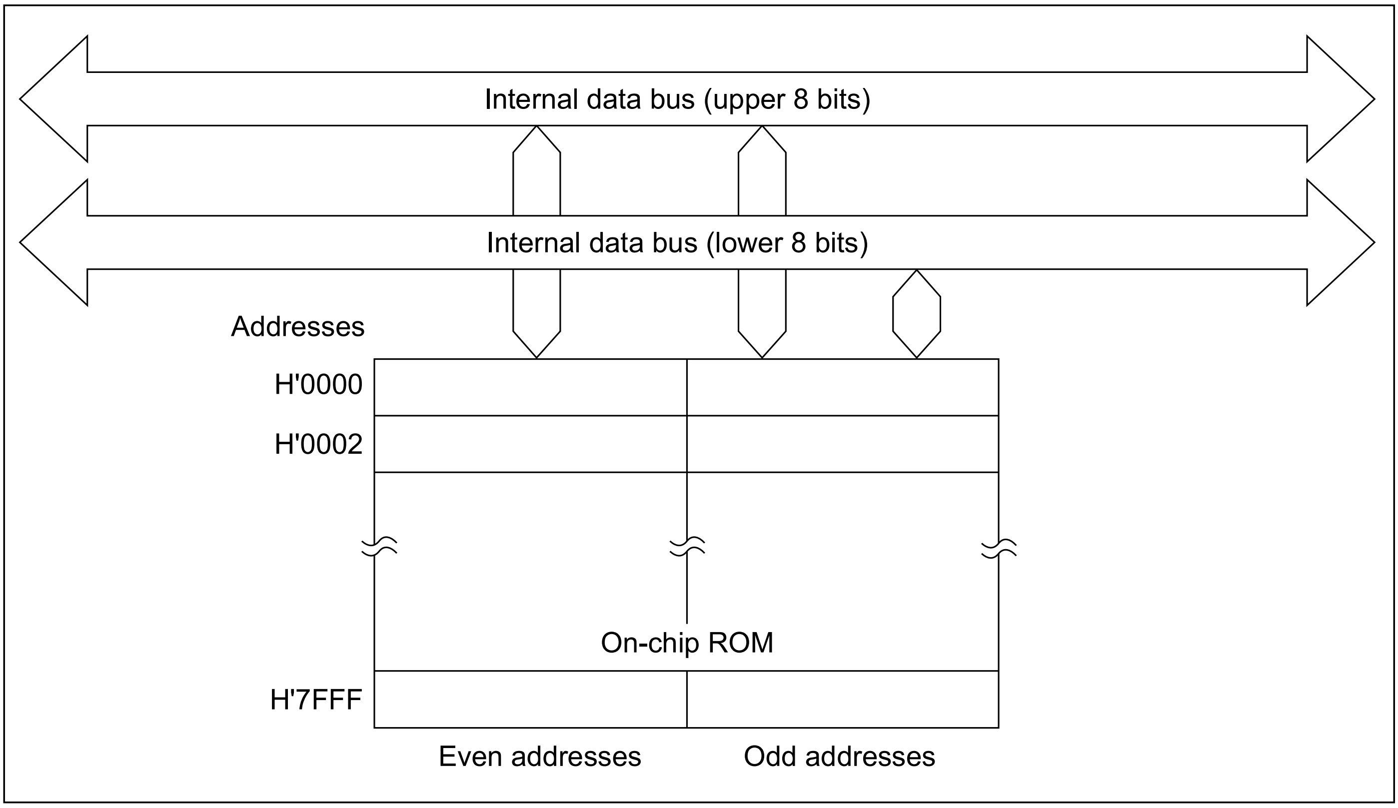

Figure 17-1 Block Diagram of On-Chip ROM

17.2 PROM Mode

17.2.1 PROM Mode Setup

The PROM version of the H8/532 has a PROM mode in which the usual microcomputer functions are halted to allow the on-chip PROM to be programmed. The programming method is the same as for the HN27C256.

To select the PROM mode, apply the signal inputs listed in table 17-2.

Table 17-2 Selection of PROM Mode

Pin	Input
Mode pins (MD_2, MD_1, and MD_0)	Low
STBY pin	Low
$P6_1$ and $P6_0$	High

17.2.2 Socket Adapter Pin Arrangements and Memory Map

The H8/532 can be programmed with a general-purpose PROM writer by attaching a socket adapter as listed in table 17-3. The socket adapter depends on the type of package. Figure 17-2 shows the socket adapter pin arrangements by giving the correspondence between H8/532 pins and HN27C256 pin functions. Figure 17-3 is a memory map.

Table 17-3 Socket Adapter

Package	Socket Adapter
84-Pin PLCC (CP-84)	HS538ESC01H
84-Pin windowed LCC (CG-84)	HS538ESG01H
80-Pin plastic QFP (FP-80A)	HS538ESH01H

H8/532

FP-80A	CG-84, CP-84	
10	21	$\overline{RES}$
11	22	NMI
13	25	$P3_0$
14	26	$P3_1$
15	27	$P3_2$
16	28	$P3_3$
17	29	$P3_4$
18	30	$P3_5$
19	31	$P3_6$
20	32	$P3_7$
21	33	$P4_0$
22	34	$P4_1$
23	35	$P4_2$
24	36	$P4_3$
25	37	$P4_4$
26	38	$P4_5$
27	39	$P4_6$
28	40	$P4_7$
30	43	$P5_0$
31	44	$P5_1$
32	45	$P5_2$
33	46	$P5_3$
34	47	$P5_4$
35	48	$P5_5$
36	49	$P5_6$
37	50	$P5_7$
38	51	$P6_0$
39	52	$P6_1$
60	74	AV_{CC}
5	16	V_{CC}
42	55	V_{CC}
6	17	MD_0
7	18	MD_1
8	19	MD_2
9	20	$\overline{STBY}$
51	65	AV_{SS}
12	2	V_{SS}
29	24	V_{SS}
71	41	V_{SS}
—	42	V_{SS}
—	64	V_{SS}
—	83	V_{SS}

EPROM socket

	HN27C256 (28 pins)
V_{PP}	1
EA_9	24
EO_0	11
EO_1	12
EO_2	13
EO_3	15
EO_4	16
EO_5	17
EO_6	18
EO_7	19
EA_0	10
EA_1	9
EA_2	8
EA_3	7
EA_4	6
EA_5	5
EA_6	4
EA_7	3
EA_8	25
$\overline{OE}$	22
EA_{10}	21
EA_{11}	23
EA_{12}	2
EA_{13}	26
EA_{14}	27
$\overline{CE}$	20
V_{CC}	28
V_{SS}	14

V_{PP}: Programming power (12.5V)
E_7 to E_0: Data input/output
EA_{14} to EA_0: Address input
$\overline{OE}$: Output enable
$\overline{CE}$: Chip enable

Note: All pins not shown in this figure should be left open.

Figure 17-2 Socket Adapter Pin Arrangements

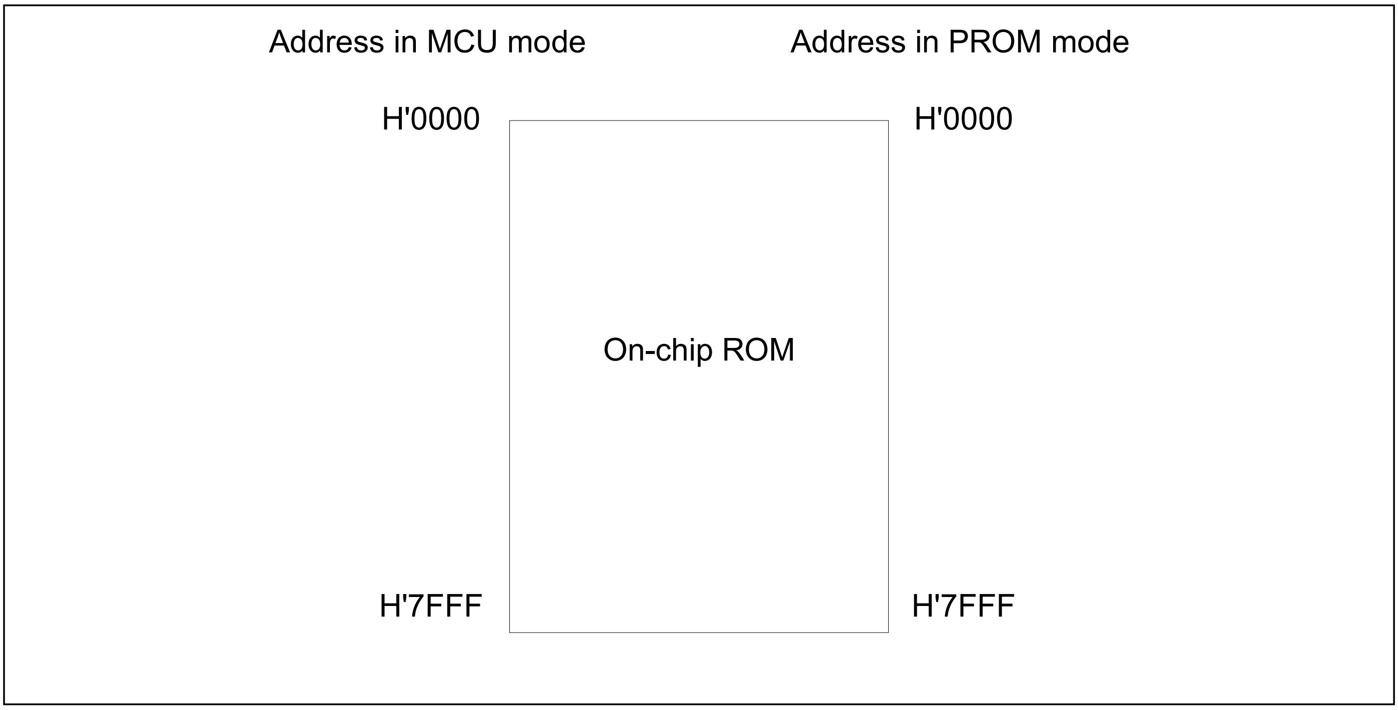

Figure 17-3 Memory Map in PROM Mode

17.3 Programming

The write, verify, and inhibited sub-modes of the PROM mode are selected as shown in table 17-4.

Table 17-4 Selection of Sub-Modes in PROM Mode

	Pins					
Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	V_{PP}	V_{CC}	O_7 to O_0	A_{14} to A_0
Write	Low	High	V_{PP}	V_{CC}	Data input	Address input
Verify	High	Low	V_{PP}	V_{CC}	Data output	Address input
Programming inhibited	High	High	V_{PP}	V_{CC}	High-impedance	Address input

Note: The V_{PP} and V_{CC} pins must be held at the V_{PP} and V_{CC} voltage levels.

The H8/532 PROM uses the same, standard read/write specifications as the HN27C256 and HN27256.

17.3.1 Writing and Verifying

An efficient, high-speed programming procedure can be used to write and verify PROM data. This procedure writes data quickly without subjecting the chip to voltage stress and without sacrificing data reliability. It leaves the data H'FF written in unused addresses.

Figure 17-4 shows the basic high-speed programming flowchart.

Tables 17-5 and 17-6 list the electrical characteristics of the chip in the PROM mode. Figure 17-5 shows a write/verify timing chart.

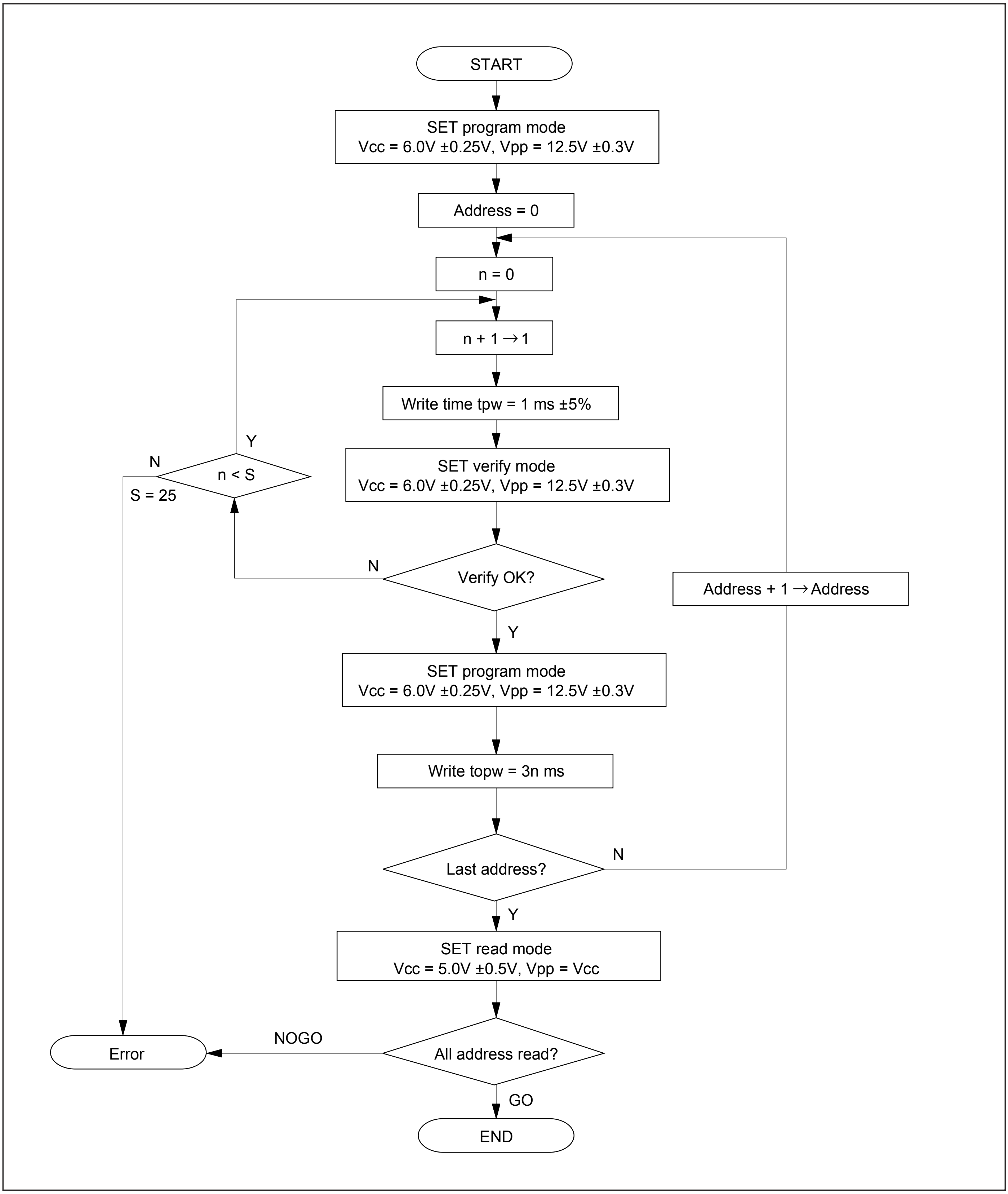

Figure 17-4 High-Speed Programming Flowchart

Table 17-5 DC Characteristics
(When V_{CC} = 6.0V ±0.25V, V_{PP} = 12.5V ±0.3V, V_{SS} = 0V, Ta = 25˚C ±5˚C)

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input High voltage	O_7 to O_0, A_{14} to A_0, $\overline{OE}$, $\overline{CE}$	V_{IH}	2.4	—	V_{CC} + 0.3	V	
Input Low voltage	O_7 to O_0, A_{14} to A_0, $\overline{OE}$, $\overline{CE}$	V_{IL}	–0.3	—	0.8	V	
Input High voltage	O_7 to O_0	V_{OH}	2.4	—	—	V	I_{OH} = –200μA
Input Low voltage	O_7 to O_0	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Input leakage current	O_7 to O_0, A_{14} to A_0, $\overline{OE}$, $\overline{CE}$	$\lvert I_{LI} \rvert$	—	—	2	μA	V_{in} = 5.25V/0.5V
V_{CC} current		I_{CC}	—	—	40	mA	
V_{PP} current		I_{PP}	—	—	40	mA	

Table 17-6 AC Characteristics
(When V_{CC} = 6.0V ±0.25V, V_{PP} = 12.5V ±0.3V, Ta = 25˚C ±5˚C)

Item	Symbol	Min	Typ	Max	Unit	Measurement Conditions
Address setup time	t_{AS}	2	—	—	μs	See figure 17-5*
$\overline{OE}$ setup time	t_{OES}	2	—	—	μs	
Data setup time	t_{DS}	2	—	—	μs	
Address hold time	t_{AH}	0	—	—	μs	
Data hold time	t_{DH}	2	—	—	μs	
Data output disable time	t_{DF}	—	—	130	μs	
V_{PP} setup time	t_{VPS}	2	—	—	μs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{OE}$ pulse width for overwrite-programming	t_{OPW}	2.85	—	78.75	ms	
V_{CC} setup time	t_{VCS}	2	—	—	μs	
Data output delay time	t_{OE}	0	—	500	ns	

* Input pulse level: 0.8V to 2.2V
Input rise/fall time ≤ 20ns
Timing reference levels: input—1.0V, 2.0V; output—0.8V, 2.0V

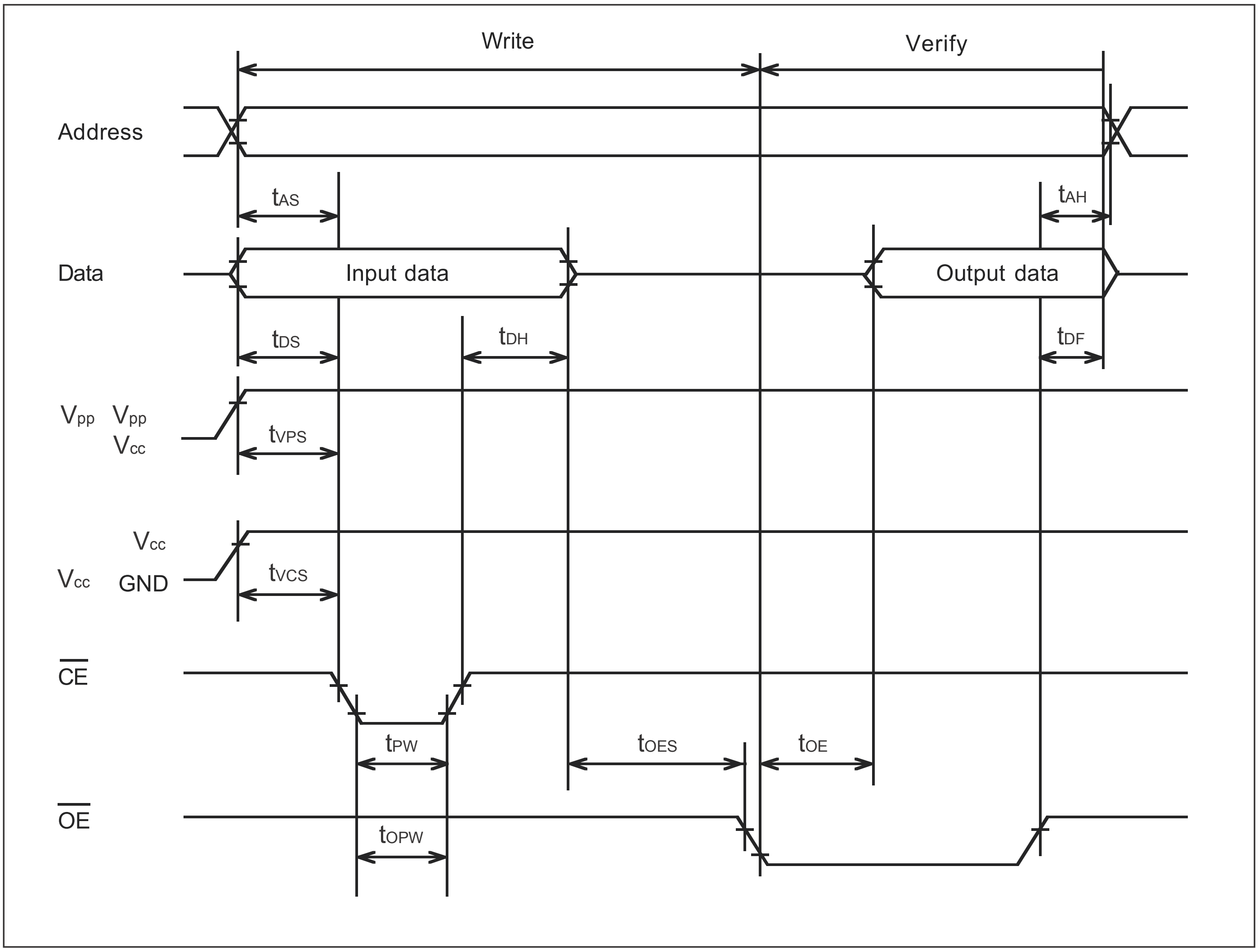

Figure 17-5 PROM Write/Verify Timing

17.3.2 Notes on Writing

1. **Write with the specified voltages and timing. The programming voltage (Vpp) in the PROM mode is 12.5V.**

Caution: Applied voltages in excess of the specified values can permanently destroy to the chip. Be particularly careful about the PROM writer's overshoot characteristics.

If the PROM writer is set to Intel specifications or Hitachi HN27256 or HN27C256 specifications, Vpp will be 12.5V.

2. **Before writing data, check that the socket adapter and chip are correctly mounted in the PROM writer.** Overcurrent damage to the chip can result if the index marks on the PROM writer, socket adapter, and chip are not correctly aligned.

3. **Don't touch the socket adapter or chip while writing.** Touching either of these can cause contact faults and write errors.

17.3.3 Reliability of Written Data

An effective way to assure the data holding characteristics of the programmed chips is to bake them at 150°C, then screen them for data errors. This procedure quickly eliminates chips with PROM memory cells prone to early failure.

Figure 17-6 shows the recommended screening procedure.

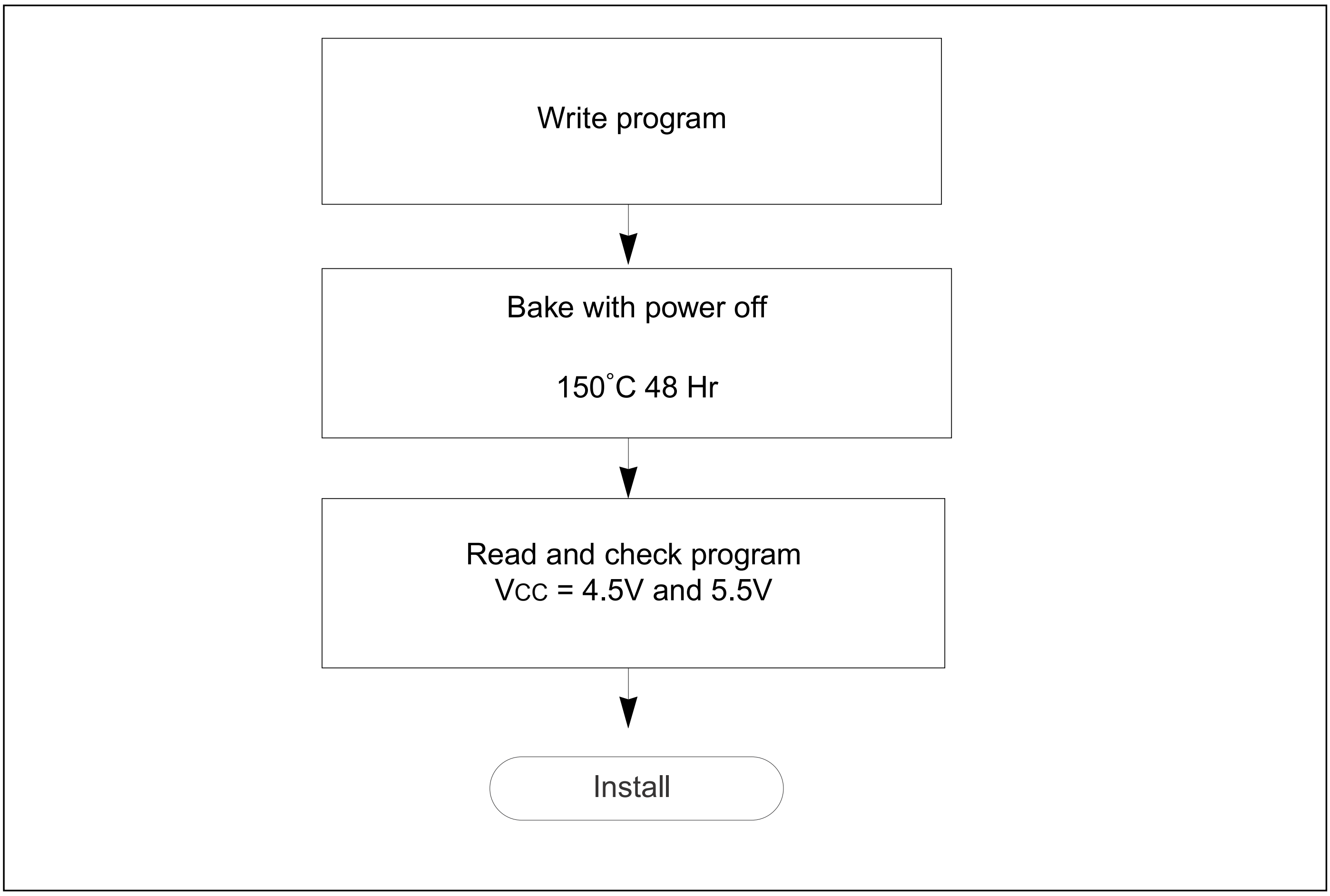

Figure 17-6 Recommended Screening Procedure

If a series of write errors occur while the same PROM writer is in use, stop programming and check the PROM writer and socket adapter for defects, using a microcomputer with a windowed package and on-chip EPROM.

Please inform Hitachi of any abnormal conditions noted during programming or in screening of program data after high-temperature baking.

17.3.4 Erasing of Data

The windowed package enables data to be erased by illuminating the window with ultraviolet light. Table 17-7 lists the erasing conditions.

Table 17-7 Erasing Conditions

Item	Value
Ultraviolet wavelength	253.7nm
Minimum illumination	$15W\cdot s/cm^2$

The conditions in table 17-7 can be satisfied by placing a $12000\mu W/cm^2$ ultraviolet lamp 2 or 3 centimeters directly above the chip and leaving it on for about 20 minutes.

17.4 Handling of Windowed Packages

1. **Glass Erasing Window:** Rubbing the glass erasing window of a windowed package with a plastic material or touching it with an electrically charged object can create a static charge on the window surface which may cause the chip to malfunction.

   If the erasing window becomes charged, the charge can be neutralized by a short exposure to ultraviolet light. This returns the chip to its normal condition, but it also reduces the charge stored in the floating gates of the PROM, so it is recommended that the chip be reprogrammed afterward.

   Accumulation of static charge on the window surface can be prevented by the following precautions:

   (1) When handling the package, ground yourself. Don’t wear gloves. Avoid other possible sources of static charge.

   (2) Avoid friction between the glass window and plastic or other materials that tend to accumulate static charge.

   (3) Be careful when using cooling sprays, since they may have a slight ion content.

   (4) Cover the window with an ultraviolet-shield label, preferably a label including a conductive material. Besides protecting the PROM contents from ultraviolet light, the label protects the chip by distributing static charge uniformly.

2. **Handling after Programming:** Fluorescent light and sunlight contain small amounts of ultraviolet, so prolonged exposure to these types of light can cause programmed data to invert.