SERVICE MANUAL
17MB70

DATE	VERSION	CHANGE	RELEASED BY
14.10.2010	V1.0	Draft	Emre YILDIZILI

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1. INTRODUCTION

17MB70-2 mainboard is based on Broadcom concept IC. This IC combines DVB-T COFDM terrestrial and PAL/SECAM demodulators, HDMI receivers, a transport processor, a digital audio processor, graphics processing, Ethernet MAC and PHY, digital processing of analog video and audio, analog video digitizer and DAC functions, stereo high-fidelity audio DACs, a 400-MHz dual-threaded MIP processor, and a peripheral control unit providing a variety of television control functions. This IC also features an advanced video decoder capable of supporting high-definition AVC, VC-1, and DVB-T MPEG-2 streams.

Main IC Features:

• Advanced multiformat decoder supporting the following:
  - H.264/AVC Main and High Profile to Level 4.1 (HD), Level 3.1 (SD)
  - HD/SD AVS Jizhun Profile Levels 2.0, 4.0, and 6.0
  - VC-1 Advanced Profile @ Level 3, simple and main profiles
  - HD/SD MPEG-2 Main Profile at Main and High levels
  - MPEG still image decode
  - HD DivX® 3.11/4.11/5.x/6x/Home Theater
• 3D/2D OpenGL® ES 1.0- compliant graphics core
• Integrated Video Processing:
  - 3D Color management
  - Digital, Analog, and Mosquito Noise Reduction
  - 1080i motion adaptive deinterlacing with 3:2/2:2 pull-down
  - True 10-bit video carried through system
• Dual HDMI 1.3a receivers
• Extensive audio support:
  - AAC+ Level 2, AAC-HE
  - Dolby® Digital, Dolby Digital Plus, Trusurround XT®
  - MPEG I layers 1, 2, and 3 (MP3)
  - Windows Media® and Windows Media Pro audio
  - Audio DACs, input switch, and equalizer
• Ethernet MAC and PHY
• Integrated DVB-T COFDM terrestrial demodulator:
  - Standards compliance: ETSI EN 300 744, Nordig Unified v1.0.3, DTG D-Book 5 compliant
  - Excellent Doppler performance
  - Active impulse noise suppression
• Integrated PAL/SECAM Demodulator
• PAL decoder with a 3D/2D comb
• Direct PC input support up to 1600 x 1200 UXGA
• Integrated dual-link LVDS transmitters
• Dual USB 2.0
• A 400-MHz 32-bit MIPS dual CPU with two 32-KB instruction caches
and a combined 64-KB data cache with 128-KB L2 cache

Sound system output is supplying 2x8W (10%THD) for stereo 8Ω speakers

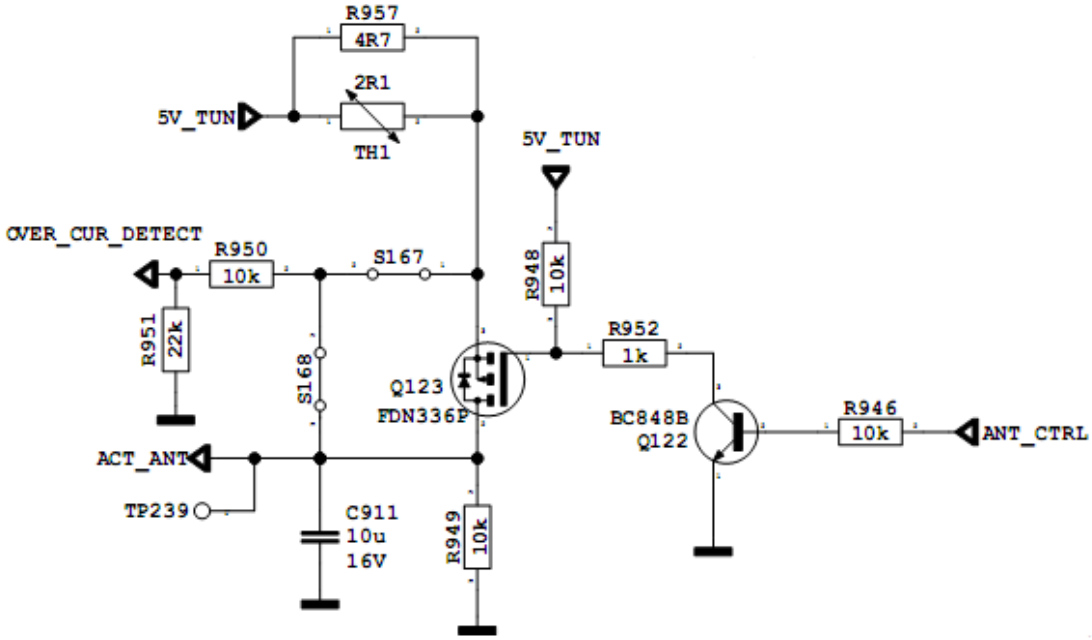
Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF @ 75Ohm(Common)
- 1 Side AV (CVBS, R/L_Audio)
- 2 SCART socket(Common)
- 1 YPbPr (Common)
- 1 Side S-Video(Common)
- 1 PC input(Common)
- 4 HDMI 1.3 input(Common)
- 1 Common interface(Common)
- 1 Optic S/PDIF output(Common)
- 1 Stereo audio input for PC(Common)
- 1 Subwoofer output(Common)
- 1 Headphone(Common)
- 2 USB(Common)
- 1 Bluray/DVD(Optional)
- 1 Ethernet-RJ45 (Common)
- 1 External Touchpad(Common)

2. TUNER

FT 2112/3/8/9 are newly developed Half-NIM modules designed for both digital (DVB-T / T2 and DTMB for terrestrial China) and analog TV reception in compliance with the European ATV standards for analogue, as well as with the terrestrial standard ETS 300 744 for DVB-T and the new terrestrial standard ETS 302 755 for DVB-T2. It consists of a 3-band RF tuner, which receives RF signal and down-converts it to an IF frequency of 36MHz for digital and 38.9MHz for analog IF. The analogue IF output can directly drive a SAW filter. A digital IF Stage, which consists of one SAW filter & gain-controllable IF that offers a sufficient output level to be connected directly to an A/D converter.

In active antenna option, the following circuit are used. ANT_CTRL pin is controlled by microcontroller. If ANT_CTRL is low, ANT_PWR will be low. If ANT_CTRL is high, ANT_PWR will be high. OVER_CUR_DETECT pin is a monitor for short circuit in antenna. OVER_CUR_DETECT is low, ANT_CTRL will be low, so ANT_PWR will be low. Finally, short circuit protection is done by circuits and microcontroller.



Active Antenna Circuit

1.1. Features of FT2112

• Digital DVB-T T2, DTMB & analogue (48.25MHz to 863.25MHz) reception
• Single 5V supply voltage only
• Built-in 5-33V DC-DC converter
• Single power supply to the RF tuner & IF VGA amplifier section
• Bus Control switch-able RF AGC function:
a) Wide Band AGC for optimum strong signal performance
b) Conventional AGC for optimum analog reception
• RF AGC information via I2C Bus
• Tuner power standby mode via I2C Bus
• Small size (56 mm x 29 mm x 10 mm)
• I2C (SDA & SCL) bus control interface
• ROHS compliant

1.2.Tuner Pinning

Pin	Function	Remark
1	Ant_Pwr	Antenna power 5V
2	--	--
3	RF AGC	External RF AGC Input
4	Vt	For Tuner Process Use only
5	AS	Tuner Address Select
6	SCL	I²C Clock
7	SDA	I²C Data
8	Vcc	Voltage Supply +5V
9	IF AGC	IF Amplifier AGC Control 0 - 3V
10	D-IF out +	Digital IF Output Balanced
11	D-IF out -	Digital IF Output Balanced
12	IF out	IF Output

3. AUDIO AMPLIFIER STAGES

A. MAIN AMPLIFIER (TPA3110)

a. General Description

17MB70 uses TPA 3110 15-W filter-free stereo Class-D audio power amplifier for main audio output. The TPA3110D2 is a 15-W (per channel) efficient, Class-D audio power amplifier for driving bridged-tied stereo speakers. Advanced EMI Suppression Technology enables the use of inexpensive ferrite bead filters at the outputs while meeting EMC requirements. SpeakerGuard™ speaker protection circuitry includes an adjustable power limiter and a DC detection circuit. The adjustable power limiter allows the user to set a "virtual" voltage rail lower than the chip supply to limit the amount of current through the speaker. The DC detect circuit measures the frequency and amplitude of the PWM signal and shuts off the output stage if the input capacitors are damaged or shorts exist on the inputs.

The TPA3110D2 can drive stereo speakers as low as 4 Ω. The high efficiency of the TPA3110D2, 90%, eliminates the need for an external heat sink when playing music. The outputs are also fully protected against shorts to GND, VCC, and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature.

b. Features

• 15-W/ch into an 8-Ω Loads at 10% THD+N From a 16-V Supply

• 10-W/ch into 8-Ω Loads at 10% THD+N From a 13-V Supply

• 30-W into a 4-Ω Mono Load at 10% THD+N From a 16-V Supply

• 90% Efficient Class-D Operation Eliminates Need for Heat Sinks

• Wide Supply Voltage Range Allows Operation from 8 V to 26 V

• Filter-Free Operation

• SpeakerGuard™ Speaker Protection Includes Adjustable Power Limiter plus DC Protection

• Flow Through Pin Out Facilitates Easy Board Layout

• Robust Pin-to-Pin Short Circuit Protection and Thermal Protection with Auto Recovery Option

• Excellent THD+N / Pop-Free Performance

• Four Selectable, Fixed Gain Settings

• Differential Inputs

c. Absolute Ratings

			UNIT
V_{CC}	Supply voltage	AVCC, PVCC	–0.3 V to 30 V
V_I	Interface pin voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL, $\overline{FAULT}$	–0.3 V to V_{CC} + 0.3 V
		PLIMIT	–0.3 V to GVDD + 0.3 V
		RINN, RINP, LINN, LINP	–0.3 V to 6.3 V
	Continuous total power dissipation		See Dissipation Rating Table
T_A	Operating free-air temperature range		–40°C to 85°C
T_J	Operating junction temperature range(2)		–40°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
R_L	Minimum Load Resistance	BTL: PVCC > 15 V	4.8
		BTL: PVCC ≤ 15 V	3.2
		PBTL	3.2
ESD	Electrostatic discharge	Human body model (3) (all pins)	±2 kV
		Charged-device model (4) (all pins)	±500 V

d. Recommended Operating Conditions

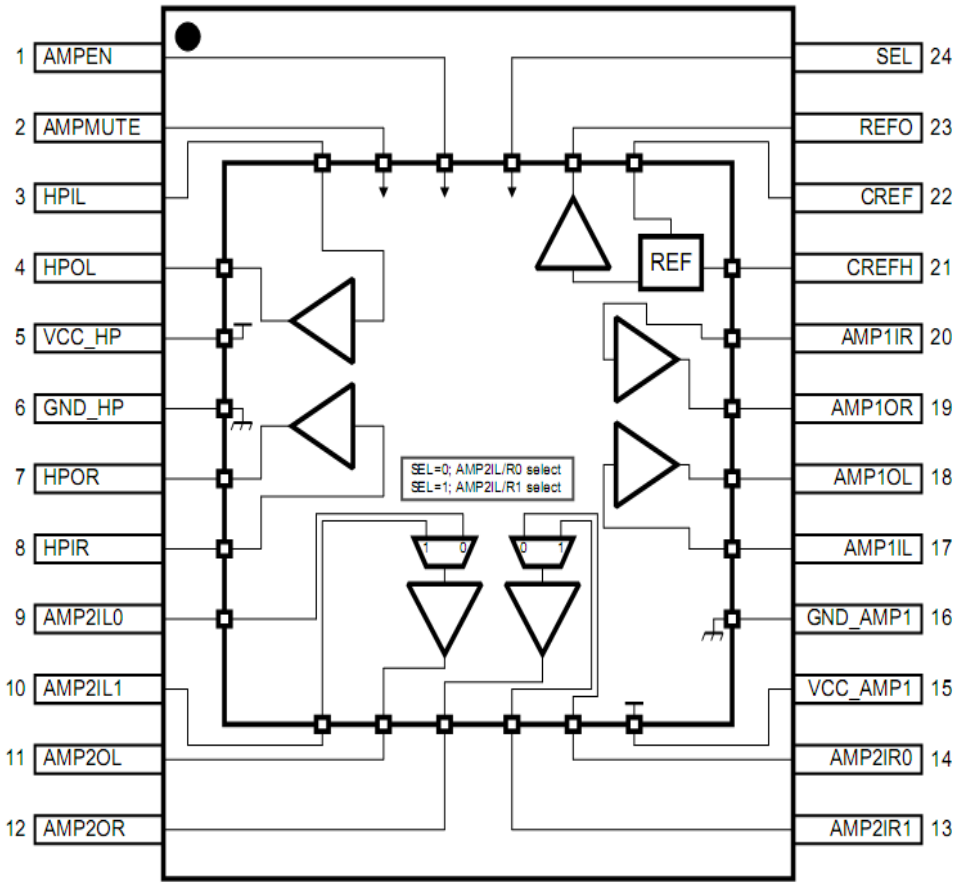
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	8	26	V
V_{IH}	High-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL		0.8	V
V_{OL}	Low-level output voltage	$\overline{FAULT}$, $R_{PULL-UP}$=100k, V_{CC}=26V		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, GAIN0, GAIN1, PBTL, V_I = 2V, V_{CC} = 18 V		50	μA
I_{IL}	Low-level input current	$\overline{SD}$, GAIN0, GAIN1, PBTL, V_I = 0.8 V, V_{CC} = 18 V		5	μA
T_A	Operating free-air temperature		–40	85	°C

e. Pin Functions

PIN NAME	PIN Number	I/O/P	DESCRIPTION
$\overline{SD}$	1	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
$\overline{FAULT}$	2	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{FAULT}$ pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVCC.
LINP	3	I	Positive audio input for left channel. Biased at 3V.
LINN	4	I	Negative audio input for left channel. Biased at 3V.
GAIN0	5	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
GAIN1	6	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
AVCC	7	P	Analog supply
AGND	8		Analog signal ground. Connect to the thermal pad.
GVDD	9	O	High-side FET gate drive supply. Nominal voltage is 7V. Also should be used as supply for PLIMIT function
PLIMIT	10	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
RINN	11	I	Negative audio input for right channel. Biased at 3V.
RINP	12	I	Positive audio input for right channel. Biased at 3V.
NC	13		Not connected
PBTL	14	I	Parallel BTL mode switch
PVCCR	15	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
PVCCR	16	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
BSPR	17	I	Bootstrap I/O for right channel, positive high-side FET.
OUTPR	18	O	Class-D H-bridge positive output for right channel.
PGND	19		Power ground for the H-bridges.
OUTNR	20	O	Class-D H-bridge negative output for right channel.
BSNR	21	I	Bootstrap I/O for right channel, negative high-side FET.
BSNL	22	I	Bootstrap I/O for left channel, negative high-side FET.
OUTNL	23	O	Class-D H-bridge negative output for left channel.
PGND	24		Power ground for the H-bridges.
OUTPL	25	O	Class-D H-bridge positive output for left channel.
BSPL	26	I	Bootstrap I/O for left channel, positive high-side FET.
PVCCL	27	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.
PVCCL	28	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.

B. LINE-OUT and HEAD-PHONE AMPLIFIER STAGE (CXA3813N)

a. Functional Block Diagram



b. Absolute Ratings

Parameter	Symbol	Rating	Condition	Unit.
Supply Voltage	VCC	24.0		V
Operating Temperature Range	T_A	-25~+85		℃
Storage Temparature Range	T_{stg}	-55~+125		℃
Junction Temparature	$T_{J(max)}$	+125		℃
Power Dissipation	P_d	$(T_J(max)-T_A)/\theta_{JA}$ *1		-
Thermal Impedance	θ_{JA}	TBD		℃/W
	θ_{JC}	TBD		℃/W

*1 Glass fabric base epoxy two-layer board, 76mm X 114mm, t=1.6mm

c. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Condition	Unit.
Supply Voltage	VCC	8.0	12.0	14.0		V
Operating Ambient Temperature	T_{opt}	-25	-	+85		℃

d. Pin Functions

Pin No	Pin Name	Direction	Description	Pin No	Pin Name	Direction	Description
1	AMPEN	I	Amp Enable Control Signal Input	13	AMP2IR1	I	AMP2 Rch Selector Input1
2	AMPMUTE	I	Amp Mute Control Signal Input	14	AMP2IR0	I	AMP2 Rch Selector Input0
3	HPIL	I	Headphone Amp Lch Input	15	VCC_AMP1	-	AMP1,2 and Reference Power
4	HPOL	O	Headphone Amp Lch Output	16	GND_AMP1	-	AMP1,2 and Reference Ground
5	VCC_HP	-	Headphone Amp Power	17	AMP1IL	I	AMP1 Lch Input
6	GND_HP	-	Headphone Amp Ground	18	AMP1OL	O	AMP1 Lch Output
7	HPOR	O	Headphone Amp Rch Output	19	AMP1OR	O	AMP1 Rch Output
8	HPIR	I	Headphone Amp Rch Input	20	AMP1IR	I	AMP1 Rch Input
9	AMP2IL0	I	AMP2 Lch Selector Input0	21	CREFH	O	"H" Reference Capacitor
10	AMP2IL1	I	AMP2 Lch Selector Input1	22	CREF	O	Reference Capacitor
11	AMP2OL	O	AMP2 Lch Output	23	REFO	O	All Amp Reference
12	AMP2OR	O	AMP2 Rch Output	24	SEL	I	AMP2 Selector Control Signal Input

C. SUBWOOFER AMPLIFIER STAGE (TPA3112)

a. General Description

The TPA3112D1 is a 25-W efficient, Class-D audio power amplifier for driving a bridge tied speaker. Advanced EMI Suppression Technology enables the use of inexpensive ferrite bead filters at the outputs while meeting EMC requirements. SpeakerGuard speaker protection system includes an adjustable power limiter and a DC detection circuit. The adjustable power limiter allows the user to set a "virtual" voltage rail lower than the chip supply to limit the amount of current through the speaker. The DC detect circuit measures the frequency and amplitude of the PWM signal and shuts off the output stage if the input capacitors are damaged or shorts exist on the inputs. The TPA3112D1 can drive a mono speaker as low as 4Ω. The high efficiency of the TPA3112D1, > 90%, eliminates the need for an external heat sink when playing music. The outputs are fully protected against shorts to GND, VCC, and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature.

b. Features

• 25-W into an 8-Ω Load at < 0.1% THD+N Froma 24V Supply
• 20-W into an 4-Ω Load at 10% THD+N From a12-V Supply
• 94% Efficient Class-D Operation into 8-Ω LoadEliminates Need for Heat Sinks
• Wide Supply Voltage Range Allows Operationfrom 8 to 26 V
• Filter-Free Operation
• SpeakerGuard™ Speaker Protection IncludesAdjustable Power Limiter plus DC Protection
• Flow Through Pin Out Facilitates Easy BoardLayout
• Robust Pin-to-Pin Short Circuit Protection andThermal Protection with Auto-Recovery Option
• Excellent THD+N/ Pop Free Performance
• Four Selectable, Fixed Gain Settings
• Differential Inputs

c. Absolute Ratings

			UNIT
V_{CC}	Supply voltage	AVCC, PVCC	–0.3 V to 30 V
V_I	Interface pin voltage	$\overline{SD}$, $\overline{FAULT}$,GAIN0, GAIN1	–0.3 V to V_{CC} + 0.3 V
		PLIMIT	–0.3 V toGVDD + 0.3 V
		INN, INP	–0.3 V to 6.3 V
	Continuous total power dissipation		See Dissipation Rating Table
T_A	Operating free-air temperature range		–40°C to 85°C
T_J	Operating junction temperature range(2)		–40°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
R_L	Minimum Load Resistance	BTL	3.2
	Electrostatic discharge	Human body model (3) (all pins)	±2 kV
		Charged-device model (4) (all pins)	±500 V

d. Recommended Operating Conditions

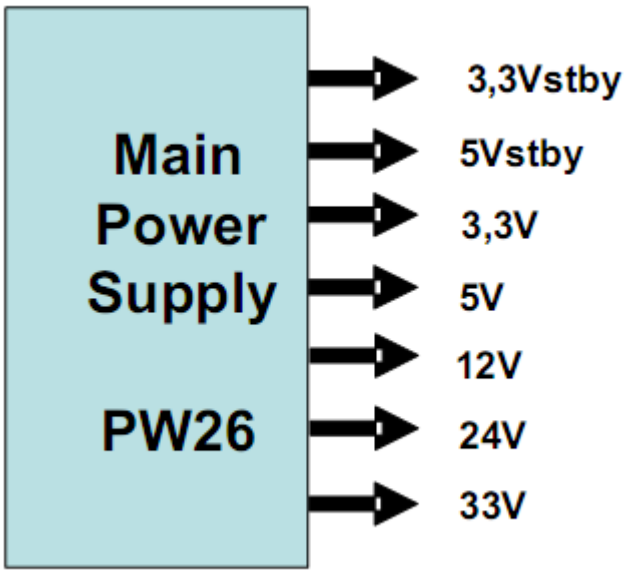
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	8	26	V
V_{IH}	High-level input voltage	$\overline{SD}$, GAIN0, GAIN1	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$, GAIN0, GAIN1		0.8	V
V_{OL}	Low-level output voltage	$\overline{FAULT}$, R_{PULLUP}=100kΩ, V_{CC}=26V		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, GAIN0, GAIN1, V_I = 2, V_{CC} = 18 V		50	μA
I_{IL}	Low-level input current	$\overline{SD}$, GAIN0, GAIN1, V_I = 0.8V, V_{CC} = 18 V		5	μA
T_A	Operating free-air temperature		–40	85	°C

e. Pin Functions

PIN		I/O	DESCRIPTION
NAME	Pin #		
$\overline{SD}$	1	I	Shutdown logic input for audio amp(LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
$\overline{FAULT}$	2	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{FAULT}$ pin to $\overline{SD}$ pin. Otherwise both the short circuit faults and dc detect faults must be reset by cycling PVCC.
GND	3		Connect to local ground
GND	4		Connect to local ground
GAIN0	5	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
GAIN1	6	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
AVCC	7	P	Analog supply.
AGND	8		Analog supply ground. Connect to the thermal pad.
GVDD	9	O	High-side FET gate drive supply. Nominal voltage is 7V. May also be used as supply for PLILMIT divider. Add a 1μF cap to ground at this pin.
PLIMIT	10	I	Power limit level adjust. Connect directly to GVDD pin for no power limiting. Add a 1μF cap to ground at this pin.

PIN NAME	Pin #	I/O	DESCRIPTION
INN	11	I	Negative audio input. Biased at 3V.
INP	12	I	Positive audio input. Biased at 3V.
NC	13		Not connected
AVCC	14	P	Connect AVCC supply to this pin
PVCC	15	P	Power supply for H-bridge. PVCC pins are also connected internally.
PVCC	16	P	Power supply for H-bridge. PVCC pins are also connected internally.
BSP	17	I	Bootstrap I/O for positive high-side FET.
OUTP	18	O	Class-D H-bridge positive output.
PGND	19		Power ground for the H-bridges.
OUTP	20	O	Class-D H-bridge positive output.
BSP	21	I	Bootstrap I/O for positive high-side FET.
BSN	22	I	Bootstrap I/O for negative high-side FET.
OUTN	23	O	Class-D H-bridge negative output.
PGND	24		Power ground for the H-bridges.
OUTN	25	O	Class-D H-bridge negative output.
BSN	26	I	Bootstrap I/O for negative high-side FET.
PVCC	27	P	Power supply for H-bridge. PVCC pins are also connected internally.
PVCC	28	P	Power supply for H-bridge. PVCC pins are also connected internally.

4. POWER STAGE



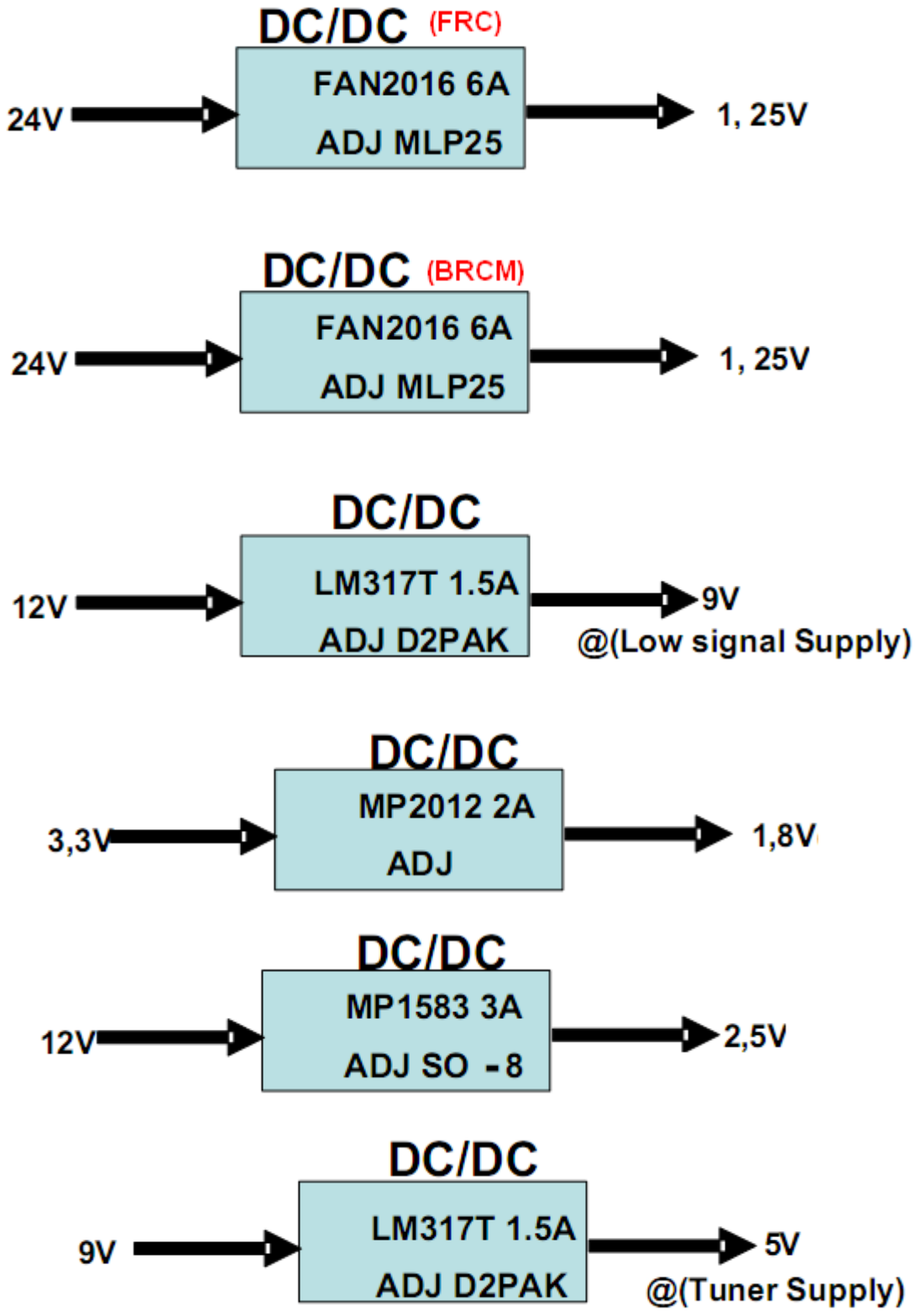
17MB70 general power managment block diagram is shown below. 17PW26 power board is used in 32" 17MB70 TV sets.

3,3V stby, 5V stby, 3,3V, 5V, 12V, 24V and 33V can be generated by PW26.

Below blocks are generated by step-downs and regulators on MB70 board.

Power Blocks on MB70:

Below blocks are generated by step-downs and regulators on MB70 board.



FAIRCHILD FAN2110 (U19-U20)

a) General Description

Features

- Wide Input Voltage Range: 3V-24V
- Wide Output Voltage Range: 0.8V to 80% V_{IN}
- 10A Output Current
- 1% Reference Accuracy Over Temperature
- Over 93% Peak Efficiency
- Programmable Frequency Operation: 200KHz to 600KHz
- Fully Synchronous Operation with Integrated Schottky Diode on Low-Side MOSFET Boosts Efficiency
- Internal Bootstrap Diode
- Power-Good Signal
- Starts up on Pre-Bias Outputs
- Accepts Ceramic Capacitors on Output
- External Compensation for Flexible Design
- Programmable Current Limit
- Under-Voltage, Over-Voltage, and Thermal Shutdown Protections
- Internal Soft-Start
- 5x6mm, 25-Pin, 3-Pad MLP Package

Applications

- Servers & Telecom
- Graphics Cards & Displays
- Computing Systems
- Point-of-Load Regulation

Description

The FAN2110 TinyBuck™ is a highly efficient, small footprint, constant frequency, 10A integrated synchronous Buck regulator.

The FAN2110 contains both synchronous MOSFETs and a controller/driver with optimized interconnects in one package, which enables designers to solve high-current requirements in a small area with minimal external components. Integration helps to minimize critical inductances making component layout simpler and more efficient compared to discrete solutions.

The FAN2110 provides for external loop compensation, programmable switching frequency, and current limit. These features allow design flexibility and optimization. High frequency operation allows for all ceramic solutions.

The summing current mode modulator uses lossless current sensing for current feedback and over-current protection. Voltage feedforward helps operation over a wide input voltage range.

Fairchild's advanced BiCMOS power process, combined with low-$R_{DS(ON)}$ internal MOSFETs and a thermally efficient MLP package, provide the ability to dissipate high power in a small package.

Output over-voltage, under-voltage, and thermal shutdown protections help protect the device from damage during fault conditions. FAN2110 also prevents pre-biased output discharge during startup in point-of-load applications.

Pin Configuration

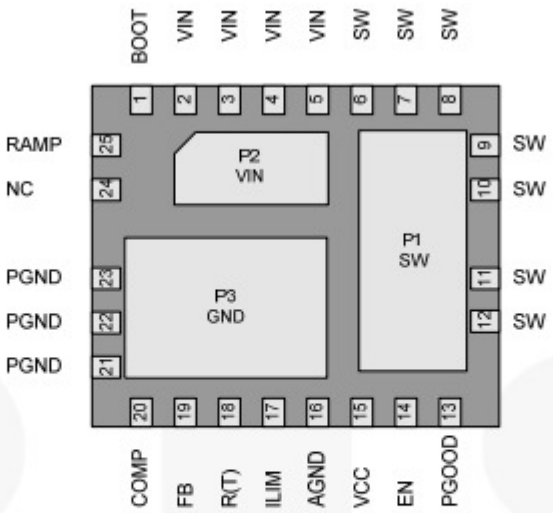


Figure 3. MLP 5x6mm Pin Configuration (Bottom View)

Pin Definitions

Pin #	Name	Description
P1, 6-12	SW	**Switching Node**. Junction of high-side and low-side MOSFETs.
P2, 2-5	VIN	**Power Conversion Input Voltage**. Connect to the main input power source.
P3, 21-23	PGND	**Power Ground**. Power return and Q2 source.
1	BOOT	**High-Side Drive BOOT Voltage**. Connect through capacitor (C_{BOOT}) to SW. The IC includes an internal synchronous bootstrap diode to recharge the capacitor on this pin to V_{CC} when SW is LOW.
13	PGOOD	**Power-Good Flag**. An open-drain output that pulls LOW when FB is outside the limits specified in electrical specs. PGOOD does not assert HIGH until the fault latch is enabled.
14	EN	**ENABLE**. Enables operation when pulled to logic HIGH or left open. Toggling EN resets the regulator after a latched fault condition. This input has an internal pull-up when the IC is functioning normally. When a latched fault occurs, EN is discharged by a current sink.
15	VCC	**Input Bias Supply for IC**. The IC's logic and analog circuitry are powered from this pin. This pin should be decoupled to AGND through a > 2.2µF X5R / X7R capacitor.
16	AGND	**Analog Ground**. The signal ground for the IC. All internal control voltages are referred to this pin. Tie this pin to the ground island/plane through the lowest impedance connection.
17	ILIM	**Current Limit**. A resistor (R_{ILIM}) from this pin to AGND can be used to program the current-limit trip threshold lower than the internal default setting.
18	R(T)	**Oscillator Frequency**. A resistor (R_T) from this pin to AGND sets the PWM switching frequency.
19	FB	**Output Voltage Feedback**. Connect through a resistor divider to the output voltage.
20	COMP	**Compensation**. Error amplifier output. Connect the external compensation network between this pin and FB.
24	NC	**No Connect**. This pin is not used.
25	RAMP	**Ramp Amplitude**. A resistor (R_{RAMP}) connected from this pin to V_{IN} sets the ramp amplitude and provides voltage feedforward functionality.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter	Conditions	Min.	Max.	Unit
VIN to PGND			28	V
VCC to AGND	AGND=PGND		6	V
BOOT to PGND			35	V
BOOT to SW		-0.5	6.0	V
SW to PGND	Continuous	-0.5	24.0	V
	Transient (t < 20ns, f ≤ 600KHz)	-5	30	V
All other pins		-0.3	V_{CC}+0.3	V
ESD	Human Body Model, JEDEC JESD22-A114	2.0		KV
	Charged Device Model, JEDEC JESD22-C101	2.5		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Bias Voltage	VCC to AGND	4.5	5.0	5.5	V
V_{IN}	Supply Voltage	VIN to PGND	3		24	V
T_A	Ambient Temperature	FAN2110MPX	-10		+85	°C
		FAN2110EMPX	-40		+85	°C
T_J	Junction Temperature				+125	°C
f_{SW}	Switching Frequency		200		600	kHz

Thermal Information

Symbol	Parameter		Min.	Typ.	Max.	Unit
T_{STG}	Storage Temperature		-65		+150	°C
T_L	Lead Soldering Temperature, 10 Seconds				+300	°C
θ_{JC}	Thermal Resistance: Junction-to-Case	P1 (Q2)		4		°C/W
		P2 (Q1)		7		°C/W
		P3		4		°C/W
θ_{J-PCB}	Thermal Resistance: Junction-to-Mounting Surface[1]			35		°C/W
P_D	Power Dissipation, T_A=25°C[1]				2.8	W

MP1583 (U38)

DESCRIPTION

The MP1583 is a step-down regulator with abuilt-in internal Power MOSFET. It achieves 3A of continuous output current over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. An adjustable soft-start reduces the stress on the input source at startup. In shutdown mode the regulator draws 20µA of supply current. The MP1583 requires a minimum number of external components, providing a compact solution.

FEATURES

- 3A Output Current
- Programmable Soft-Start
- 100mΩ Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 20µA Shutdown Mode
- Fixed 385KHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.75V to 23V Operating Input Range
- Output Adjustable from 1.22V to 21V
- Under-Voltage Lockout

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

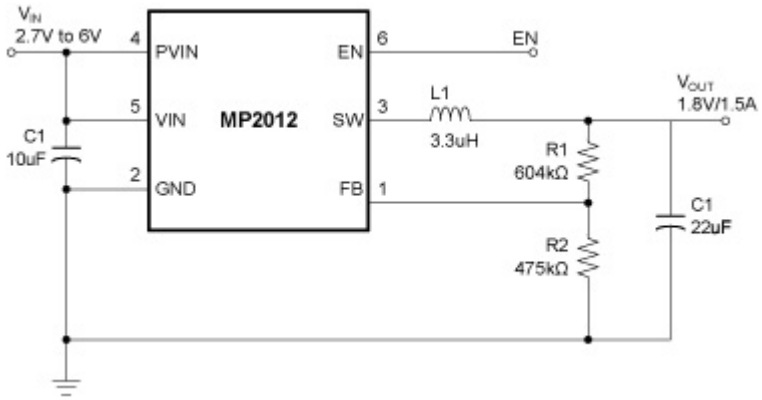
Parameters	Symbol	Condition	Min	Typ	Max	Units
Shutdown Supply Current		V_{EN} = 0V		20	30	µA
Supply Current		V_{EN} = 2.8V, V_{FB} =1.4V		1.0	1.2	mA
Feedback Voltage	V_{FB}	4.75V ≤ V_{IN} ≤ 23V	1.194	1.222	1.250	V
Error Amplifier Voltage Gain	A_{VEA}			400		V/V
Error Amplifier Transconductance	G_{EA}	ΔI_{COMP} = ±10µA	500	800	1120	µA/V
High-Side Switch On-Resistance	$R_{DS(ON)1}$			0.1		Ω
Low-Side Switch On-Resistance	$R_{DS(ON)2}$			10		Ω
High-Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V		0	10	µA
Current Limit			4.0	4.9	6.0	A
Current Sense to COMP Transconductance	G_{CS}			3.8		A/V
Oscillation Frequency	f_S		335	385	435	KHz
Short Circuit Oscillation Frequency	D_{MAX}	V_{FB} = 0V	25	40	55	KHz
Maximum Duty Cycle		V_{FB} = 1.0V		90		%
Minimum Duty Cycle		V_{FB} = 1.5V			0	%
EN Shutdown Threshold Voltage			0.9	1.2	1.5	V
Enable Pull Up Current		V_{EN} = 0V	1.1	1.8	2.5	µA
EN UVLO Threshold		V_{EN} Rising	2.37	2.54	2.71	V
EN UVLO Threshold Hysteresis				210		mV
Soft-Start Period		C_{SS} = 0.1µF		10		ms
Thermal Shutdown				160		°C

MP2012 (U39)

The MP2012 is a fully integrated, internally compensated 1.2MHz fixed frequency PWM step-down converter. It is ideal for powering portable equipment that runs from a single cell Lithium-Ion (Li+) Battery, with an input range from 2.7V to 6V. The MP2012 can provide up to 1.5A of load current with output voltage as low as 0.8V. It can also operate at 100% duty

cycle for low dropout applications. With peak current mode control and internal compensation, the MP2012 is stable with ceramic capacitors and small inductors. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. MP2012 is available in the small 6-pin 3mmx3mm QFN package.

- 2.7-6V Input Operation Range
- Output Adjustable from 0.8V to VIN
- 1µA Max Shutdown Current.
- Up to 95% Efficiency
- 100% Duty Cycle for Low Dropout Applications
- 1.2MHz Fixed Switching Frequency
- Stable with Low ESR Output Ceramic Capacitors
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Short Circuit Protection
- Available in 6-pin 3x3mm QFN



LM1117 (U21-U22-U23-U24)

General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317.

The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V.

The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within ±1%.

The LM1117 series is available in SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10µF tantalum capacitor is required at the output to improve the transient response and stability.

Features

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 Package
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
  - — LM1117 0°C to 125°C
  - — LM1117I −40°C to 125°C

Applications

- 2.85V Model for SCSI-2 Active Termination
- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators
- Battery Charger
- Battery Powered Instrumentation

5. MICROCONTROLLER(Broadcom)

BCM3556

a) General Description

The BCM3556 is the next generation of System-on-a-Chip (SoC) Digital Television (DTV) products from Broadcom® with 1080p60 input and output capability targetedfor the EU Market. It combines a high level of integration with best-of-class picture quality, enabling TV manufacturers to reduce overall system cost (BOM) and improve picture quality, all with a single SoC.

The BCM3556 combines DVB-T COFDM terrestrial and PAL/SECAM demodulators, two DVI/HDMI receivers, a transport processor, a digital audio processor, 3D/2D graphics processing, Ethernet MAC and PHY, digital processing of analog video and audio, analog video digitizer and DAC functions, stereo high-fidelity audio DACs, a 400-MHz dual-threaded MIPS processor, and a peripheral control unit providing a variety of television control functions. The BCM3556 also features an advanced video decoder capable of supporting high-definition AVC, VC-1, and DVB-T MPEG-2 streams.

The integration of the DVB-T COFDM terrestrial demodulator reduces the overall cost of the external tuner module, resulting in cost savings for the customer. The BCM3556also integrates four 10-bit ADCs with integrated front-end analog muxing that accept four CVBS inputs, three S-video inputs, three component inputs, one PC input, one full SCART input with fast blanking, and one Sound IF (SIF) input at the same time without the requirement for any off-chip muxing ICs. The BCM3556 offers two HDMI 1.3a receivers, a motion adaptive deinterlacer, HD Analog Noise Reduction, and an analog video decoder with 3D comb for PAL and Y/C separation for SECAM.

The multiformat video decoder in the BCM3556 is capable of supporting high-definition AVC, VC-1, and DVB-T MPEG-2 streams. AVC support is up to High Profile Level 4.1. New tools in the AVC Fidelity Range extensions are supported, including 8x8 transform and spatial prediction modes and adaptive quantization matrix. The video decoder also supports high-definition VC-1 (Advanced Profile Level 3, Main, and Simple profiles) and DVB-Tcompliant MPEG-2, Main Profile at Main and High Levels. The BCM3556 has an advanced programmable audio processor capable of decoding a broad range of formats including Dolby Digital, Dolby Digital Plus, AAC 5.1, AAC+ Level 2, AAC+ Level 4, WMA, and MPEG-1 Layer 1, 2, and 3 with simultaneous pass-through support.
The BCM3556 also supports 3D SRS Audio and includes an analog audio decoder for BTSC and A2 formats. The BCM3556 also integrates an analog audio switch that accepts six stereo inputs. In addition, the SoC supports SPDIF and I2S inputs. One SPDIF, two I2S, and three analog audio outputs are available.

The SoC family also has an integrated advanced Picture Enhancement Processor (PEP) to improve sharpening and perform picture post-processing functions (e.g., autoflesh, green boost, black and blue stretch). The PEP engine is fully programmable and can be optimized by the TV manufacturer to meet their respective quality requirements. Also integrated is a video encoder for NTSC and an advanced 2D/3D graphics for OSD acceleration.

The BCM3556 supports direct PC inputs up to UXGA 1600x1200 formats with autophase and automode detection and supports dual LVDS outputs to support 1080p60 panels.

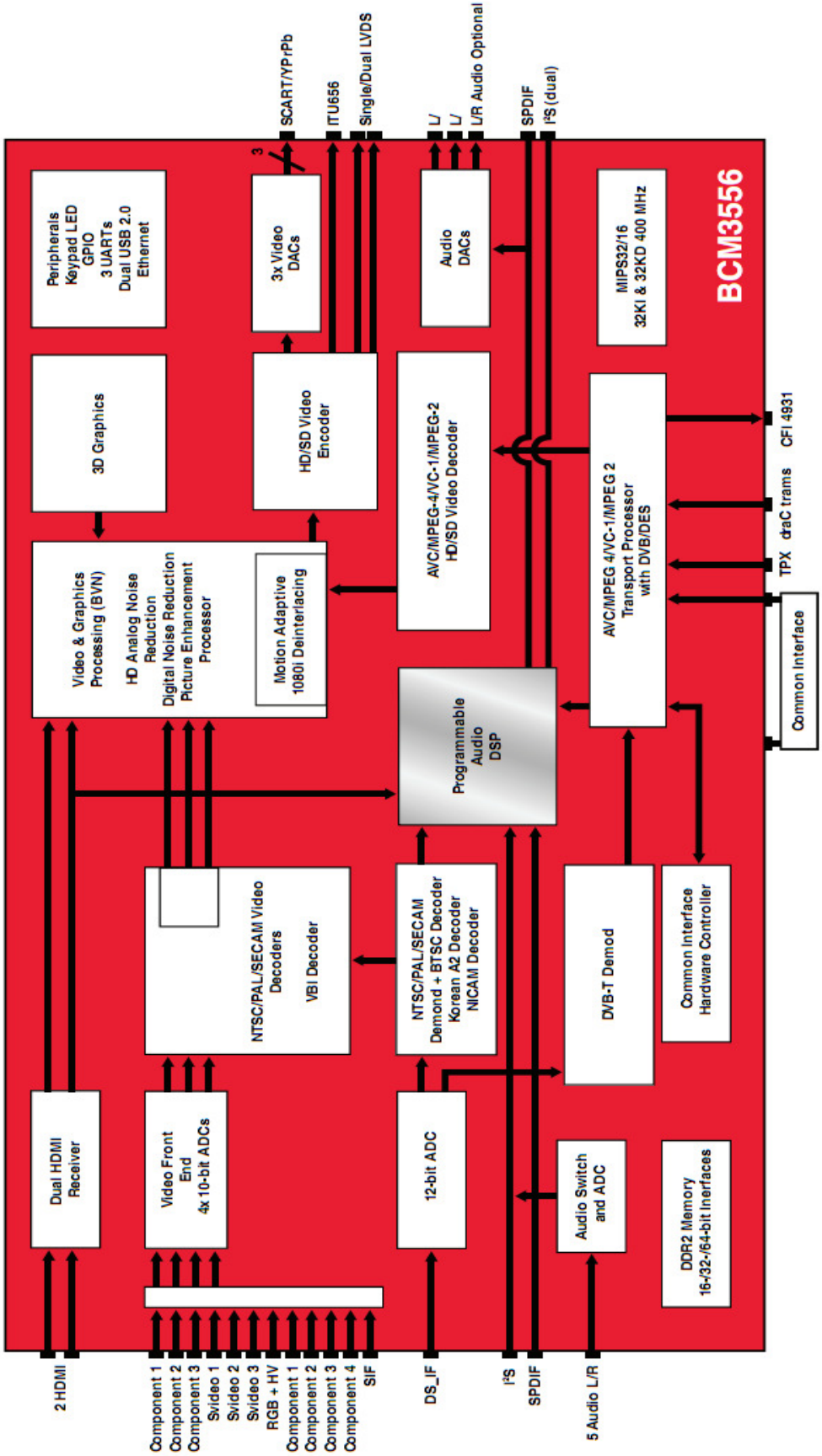
The BCM3556 integrates a 400-MHz 32-bit MIPS dual CPU with two 32-KB instructioncaches and a combined 64-KB data cache with a 128-KB L2 cache, and a 32-bit 800/1066-MHz DDR2. The BCM3556 also supports an 8-bit external NAND Flash interface and SPI Flash interface for booting. Integrated peripherals include two USB2.0 ports, three UARTs, controllers for SPI, BSC, keypad, LED and IR Tx/Rx, and an Ethernet port with MAC and integrated PHY.

The BCM3556 is available in several package options: WXGA and FHD, PIP and non-PIP, or MPEG-only and combined AVC/MPEG-2.

b) Features

• Advanced multiformat decoder supporting the following:
  - H.264/AVC Main and High Profile to Level 4.1 (HD), Level 3.1 (SD)
  - HD/SD AVS Jizhun Profile Levels 2.0, 4.0, and 6.0
  - VC-1 Advanced Profile @ Level 3, simple and main profiles
  - HD/SD MPEG-2 Main Profile at Main and High levels
  - MPEG still image decode
  - HD DivX® 3.11/4.11/5.x/6x/Home Theater
• 3D/2D OpenGL® ES 1.0- compliant graphics core
• Integrated Video Processing:
  - 3D Color management
  - Digital, Analog, and Mosquito Noise Reduction
  - 1080i motion adaptive deinterlacing with 3:2/2:2 pull-down
  - True 10-bit video carried through system
• Dual HDMI 1.3a receivers
• Extensive audio support:
  - AAC+ Level 2, AAC-HE
  - Dolby® Digital, Dolby Digital Plus, Trusurround XT®
  - MPEG I layers 1, 2, and 3 (MP3)
  - Windows Media® and Windows Media Pro audio
  - Audio DACs, input switch, and equalizer
• Ethernet MAC and PHY
• Integrated DVB-T COFDM terrestrial demodulator:
  - Standards compliance: ETSI EN 300 744, Nordig Unified v1.0.3, DTG D-Book 5 compliant
  - Excellent Doppler performance
  - Active impulse noise suppression
• Integrated PAL/SECAM Demodulator
• PAL decoder with a 3D/2D comb
• Direct PC input support up to 1600 x 1200 UXGA
• Integrated dual-link LVDS transmitters
• Dual USB 2.0
• A 400-MHz 32-bit MIPS dual CPU with two 32-KB instruction caches and a combined 64 KB data cache with 128-KB L2 cache

c) BCM3556 - Block Diagram



6. SATELLITE RECEIVER (Broadcom)

BCM4505

a) General Description

The BCM4505 is a fully integrated satellite receiver single-chip solution targeted at multituner advanced modulation satellite receiver systems and ideally suited for new generation satellite receivers and integrated multifunction Home Media Centers. The BCM4505 integrates a CMOS tuner and advanced modulation decoder supporting DVB-S2 Broadcast, DVB-S, DIRECTV, and 8PSK Turbo applications. The highly integrated tuner section is based on existing volume-production Broadcom technologies and a direct-conversion technology to reduce external components and increase performance.The BCM4505 is designed to support the full 1-45 Msps DVB operating range with support for 250 to 2150 MHz input frequencies. It contains two 8-bit A/D converters, all-digital variable-rate QPSK/8PSK receivers, an advanced modulation LDPC/BCH and Turbo FEC decoder, and a DVB-S compliant FEC decoder. All required RAM is integrated and all required clocks are generated on-chip from a single reference crystal. The baseband IQ analog waveforms from the tuner section are sampled by the integrated 8-bit A/D converters and resampled by the integrated interpolative digital filter banks.

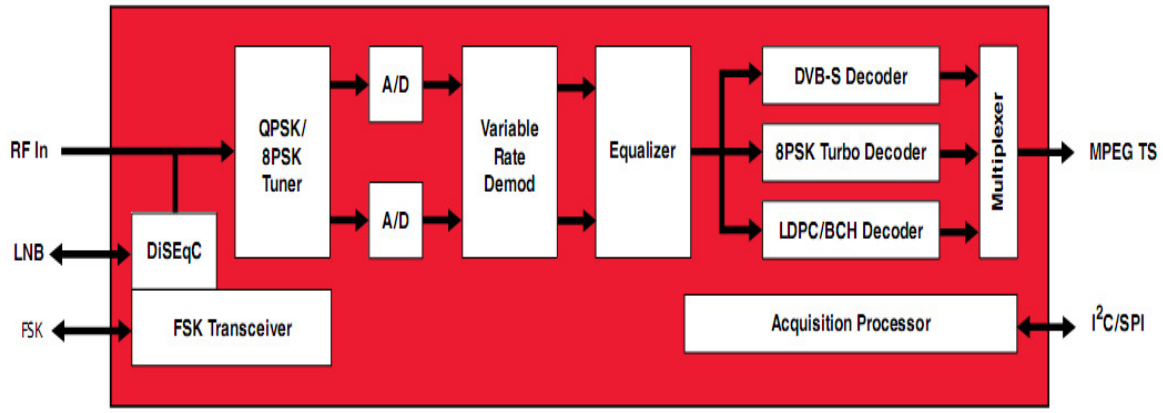
Optimized soft decisions are then fed into either a DVB-S-compliant FEC decoder, or an advanced-modulation DVB-S2 LDPC/BCH or Turbo decoder. The final error-corrected output is delivered in MPEG-2 transport format. The output clock is generated by an on-chip PLL for low-jitter operation and glueless integration with Broadcom's high definition audio video subsystems, such as the BCM7401 and the BCM7402. The communication link sections include an on-chip microcontroller for all system configuration, acquisition, control, monitoring and diagnostics functions, as well as an integrated DiSEqC 2.x controller for 2-way communication with an LNB, and a single FSK transceiver for communication with ODUs that support multiple LNB configurations over a single coax connection.The BCM94505 reference design is available for easy system design and testing using the BCM4505 advanced modulation receiver chip.

b) Features

- Dual direct conversion satellite tuners
    - Direct conversion architecture in standard CMOS process
    - Supports QPSK and 8PSK demodulation
    - Input frequency range: 250 to 2150 MHz
    - Integrated 8-bit A/D converters
- Integrated advanced demodulation decoder
    - DVB-S2 Broadcast, DVB-S, 8PSK Turbo
- Data Rates:
    - DVB-S: 1-45 Msps
    - DVB-S2: 1-45 Msps
    - 8PSK Turbo: 2-30 Msps
- Code Rates: 1/4, 1/3, 2/5, 1/2,3/5, 2/3, 3/4 , 5/6, 7/8, 8/9, 9/10
- Integrated DiSEqC 2.x transceivers

• On-chip microcontroller for acquisition and tracking
• 128-pin epLQFP package

c) BCM4505 - Block Diagram



7. VIDEO BACK-END PROCESSOR (Trident)

PNX5120EH

a) General Description

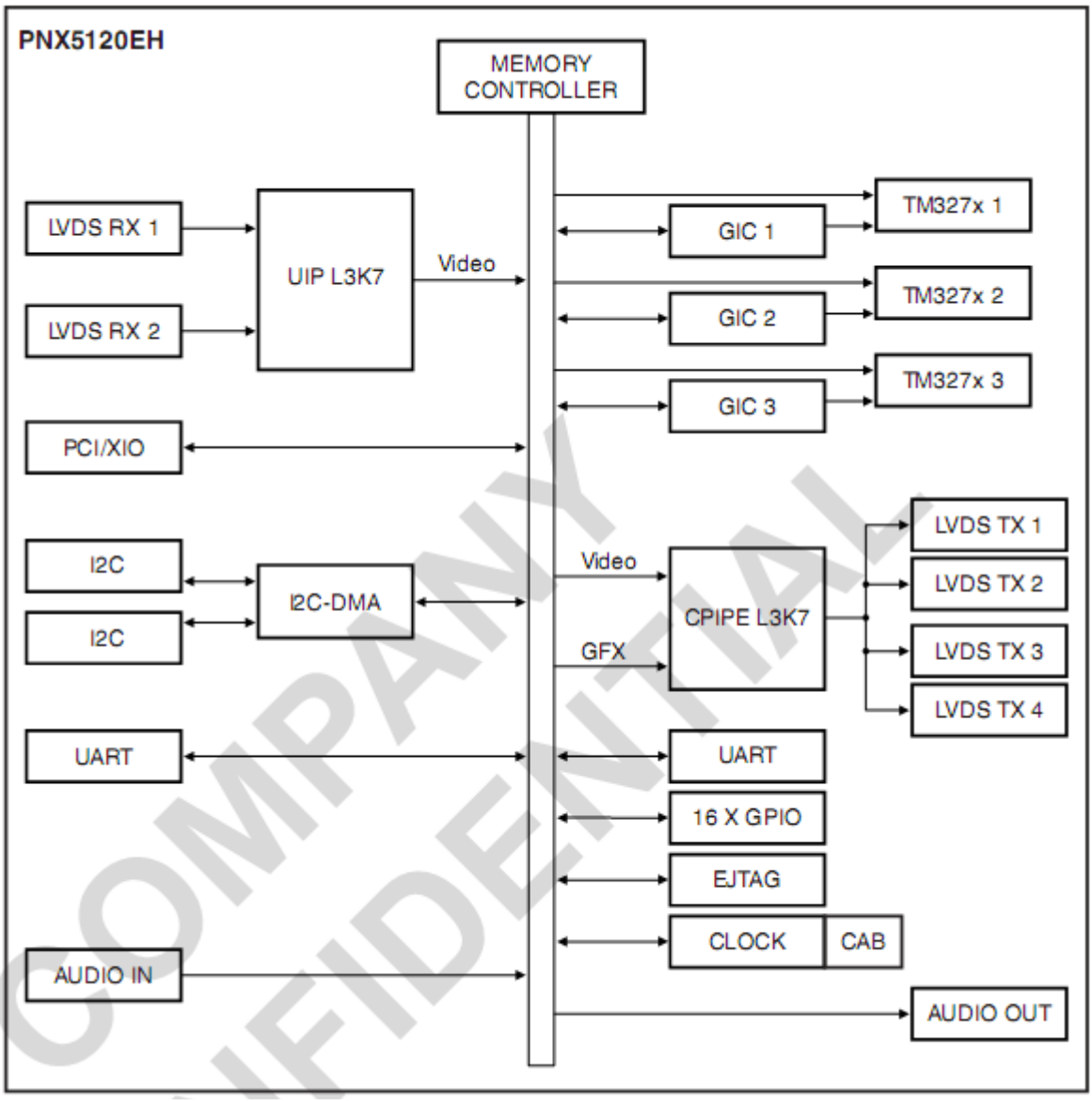
The PNX5120EH is an advanced video picture improvement IC and the world's first solution, NXP's Motion Accurate Picture Processing (MAPP), to combine movie judder cancellation, motion sharpness and vivid color management in a single device. Aimed primarily at digital and hybrid flat panel televisions in the mid-end and high-end European,Asian and U.S. consumer markets, it complies with relevant industry standards.LCD TVs represent a huge and growing market, and the PNX5120EH offers manufacturers a unique combination of richer color, dynamic motion, sensational sharpness, deep contrast, and full HD resolution. Moreover, you can easily tailor that balance via the Automatic Picture Control tool (delivered by NXP as part of a separate System Design-in Toolkit) to meet your own image quality requirements.

b) Features

- Single 27 MHz crystal clock input for all internal generated clocks
- Three TriMedia TM3271 400 MHz, 32-bit VLIW media-processing cores with:
  - five instructions per clock cycle
  - 32 kB instruction cache
  - 64 kB data cache
- Integrated DDR2 SDRAM controller, 32-bit wide, up to 366 MHz clock (DDR2-800), supporting 32 MB, 64 MB, 128 MB, and 256 MB single-rank memory configurations
- Separately licensed, the PNX5120EH comes with an easy-to-use System Design-in Toolkit (SDT), which includes the NXP Picture Quality Tuning Tool, firmware image containing the NXP proprietary Picture Improvement features, and GPL-licensed U-Boot Bootloader software.

- DDR2-400 to DDR2-800 data rates supported
- PCI/XIO (V2.2) operating at 33 MHz
- Two UARTs
- Two I2C DMA interfaces (100 kHz/400 kHz); the second I2C can be used as a debugging interface
- 16 GPIO pins
- Five PWM outputs
- Support for 8-bit NOR flash up to 64 MB
- Support for 8-bit/16-bit NAND flash up to 128 MB

c) PNX5120EH - Block Diagram



8. FPGA (Spartan-3E)

XC3S1200E

a) General Description

The Spartan™-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates, The Spartan-3E family builds on the success of the earlier Spartan-3 family by increasing the amount of logic per I/O, significantly reducing the cost per logic cell. New features improve system performance and reduce the cost of configuration. These Spartan-3E enhancements, combined with advanced 90 nm process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry. Because of their exceptionally low cost, Spartan-3E FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment. The Spartan-3E family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

b) Features

• Very low cost, high-performance logic solution for high-volume, consumer-oriented applications
• Proven advanced 90-nanometer process technology
• Multi-voltage, multi-standard SelectIO™ interface pins
    - Up to 376 I/O pins or 156 differential signal pairs
    - LVCMOS, LVTTL, HSTL, and SSTL single-ended signal standards
    - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
    - 622+ Mb/s data transfer rate per I/O
    - True LVDS, RSDS, mini-LVDS, differential HSTL/SSTL differential I/O
    - Enhanced Double Data Rate (DDR) support
    - DDR SDRAM support up to 333 Mb/s
• Abundant, flexible logic resources
    - Densities up to 33,192 logic cells, including optional shift register or distributed RAM support
    - Efficient wide multiplexers, wide logic
    - Fast look-ahead carry logic
    - Enhanced 18 x 18 multipliers with optional pipeline
    - IEEE 1149.1/1532 JTAG programming/debug port
• Hierarchical SelectRAM™ memory architecture
    - Up to 648 Kbits of fast block RAM
    - Up to 231 Kbits of efficient distributed RAM
• Up to eight Digital Clock Managers (DCMs)
    - Clock skew elimination (delay locked loop)
    - Frequency synthesis, multiplication, division
    - High-resolution phase shifting
    - Wide frequency range (5 MHz to over 300 MHz)

• Eight global clocks plus eight additional clocks per each half of device, plus abundant low-skew routing
• Configuration interface to industry-standard PROMs
    - Low-cost, space-saving SPI serial Flash PROM
    - x8 or x8/x16 parallel NOR Flash PROM
    - Low-cost Xilinx Platform Flash with JTAG
• Complete Xilinx ISE™ and WebPACK™ development system support
• MicroBlaze™ and PicoBlaze™ embedded processor cores
• Fully compliant 32-/64-bit 33 MHz PCI support
• Low-cost QFP and BGA packaging options
    - Common footprints support easy density migration
    - Pb-free packaging options

9. PIXELLENCE II

a) General Description

PixellenceII IC is a real-time image processing chip. It is mainly a co-processor sitting at the back of the video ASSP (i.e. concept IC) in a typical TV chassis. PixellenceII gets the picture that will otherwise be transmitted to the panel in RGB format and applies Vestel patented image and video processing algorithms to further enhance the picture. After processing, the video is transmitted to the 50/60 Hz panel serially through LVDS links and in RGB format.

PixellenceII IC supports Full HD (1920x1080) and WXGA (1366x768) resolutions with 10-bit or 8-bit processing modes. PixellenceII is also configurable to other common resolutions such as 1920x1280, 1680x1050, 1440x900, 1280x1024, 1024x768, 1920x1200, 1600x900.

The PixellenceII IC incorporates following Vestel patented algorithms, functions and interfaces:

Algorithms:
- Skin-tone detection and correction
- Color Saturation
- Dynamic Contrast Enhancement
- Sharpness & CTI
- De-ringing
- De-blocking
- Temporal Noise Reduction
- Spatial Noise Reduction
- Video Analysis Block

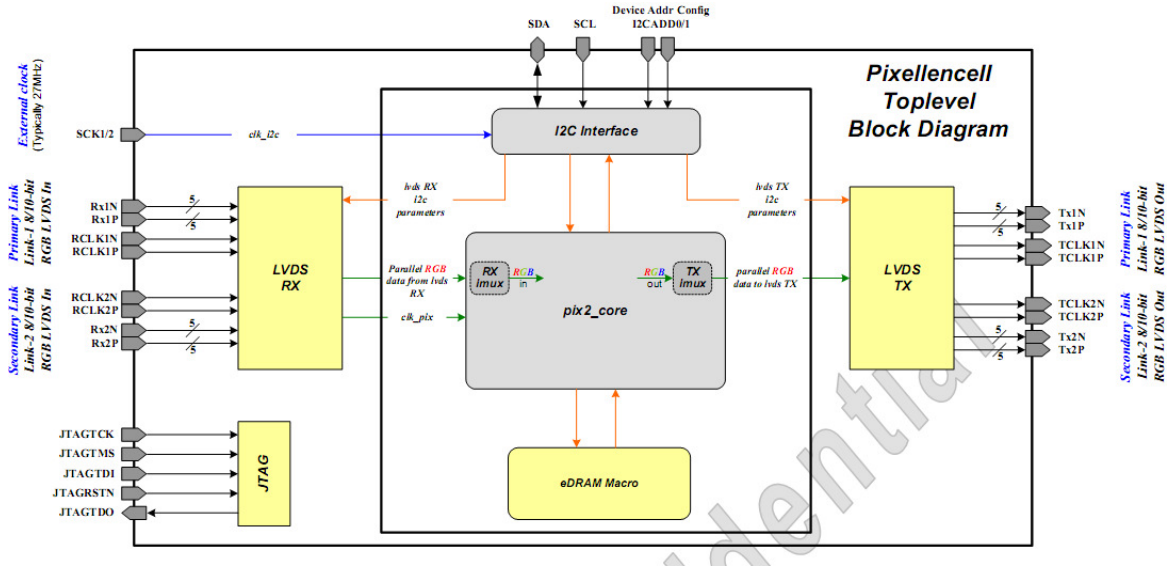
Functions:
- Color Space Conversion
- Color Up-sampling, Color Down-sampling
- Gamma Correction
- OSD Detection Logic
- Display Mode Logic
- Logo

Interfaces:

- I2C
- JTAG
- Dual-Link LVDS Receiver with Spread Spectrum clocking tolerance
- Dual-Link LVDS Transmitter with Spread Spectrum clocking tolerance
- Miscellaneous function signals (8-bit GPO port)

b) Block Diagram

Main blocks of Pix2Frame are LVDS Rx, Tx and pix2_top modules. Major blocks of pix2_top module are PixellenceII Core video enhancement engine, I2C Slave interface and embedded Dynamic RAM (eDRAM, 64Mbit) macro.



10. 1Gb F-die DDR2-1066 SDRAM (U41-U42-U8-U9)

Samsung K4T1G084QF

a) Key Features

Speed	DDR2-1066 7-7-7	Units
CAS Latency	7	tCK
tRCD(min)	13.125	ns
tRP(min)	13.125	ns
tRC(min)	58.125	ns

• JEDEC standard VDD = 1.8V ± 0.1V Power Supply
•VDDQ = 1.8V ± 0.1V
• 533MHz fCK for 1066Mb/sec/pin
• 8 Banks
• Posted CAS
• Programmable CAS Latency: 4, 5, 6, 7
• Programmable Additive Latency: 3, 4, 5. 6

• Write Latency(WL) = Read Latency(RL) -1
• Burst Length: 4 , 8(Interleave/nibble sequential)
• Programmable Sequential / Interleave Burst Mode
• Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
• Off-Chip Driver(OCD) Impedance Adjustment
• On Die Termination
• Special Function Support
    - PASR(Partial Array Self Refresh)
    - 50ohm ODT
    - High Temperature Self-Refresh rate enable
• Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C
• All of products are Lead-free, Halogen-free, and RoHS compliant

The 1Gb DDR2 SDRAM is organized as a 16Mbit x 8 I/Os x 8 banks, 8Mbit x 16 I/Os x 8 banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 1066Mb/sec/pin (DDR2-1066) for general applications.

The chip is designed to comply with the following key DDR2 SDRAM features such as posted CAS with additive latency, write latency = read latency - 1, Off-Chip Driver(OCD) impedance adjustment and On Die Termination. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and CK falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and DQS) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a RAS/CAS multiplexing style. For example, 1Gb(x8) device receive 14/10/3 addressing.

The 1Gb DDR2 device operates with a single 1.8V ± 0.1V power supply and 1.8V ± 0.1V VDDQ.

The 1Gb DDR2 device is available in 60ball FBGA(x8) and 84ball FBGA(x16).

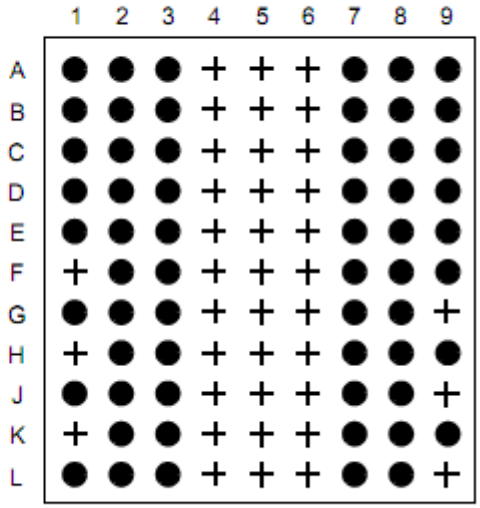
b) Pinning

	1	2	3	4	5	6	7	8	9
A	V_{DD}	NU/$\overline{RDQS}$	V_{SS}				V_{SSQ}	$\overline{DQS}$	V_{DDQ}
B	DQ6	V_{SSQ}	DM/RDQS				DQS	V_{SSQ}	DQ7
C	V_{DDQ}	DQ1	V_{DDQ}				V_{DDQ}	DQ0	V_{DDQ}
D	DQ4	V_{SSQ}	DQ3				DQ2	V_{SSQ}	DQ5
E	V_{DDL}	V_{REF}	V_{SS}				V_{SSDL}	CK	V_{DD}
F		CKE	$\overline{WE}$				$\overline{RAS}$	$\overline{CK}$	ODT0
G	BA2	BA0	BA1				$\overline{CAS}$	$\overline{CS}$	
H		A10/AP	A1				A2	A0	V_{DD}
J	V_{SS}	A3	A5				A6	A4	
K		A7	A9				A11	A8	V_{SS}
L	V_{DD}	A12	NC				NC	A13	

Ball Locations (x8)

● Populated ball
+ Ball not populated

Top view
(See the balls through package)



c) Electrical Characteristics

Symbol	Parameter	Rating			Units	NOTE
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	4
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	4
V_{REF}	Input Reference Voltage	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	mV	1,2
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3

11. 32M x 16 bit DDRII Synchronous DRAM (U28-U29)

EtronTech EM68B16CWPA

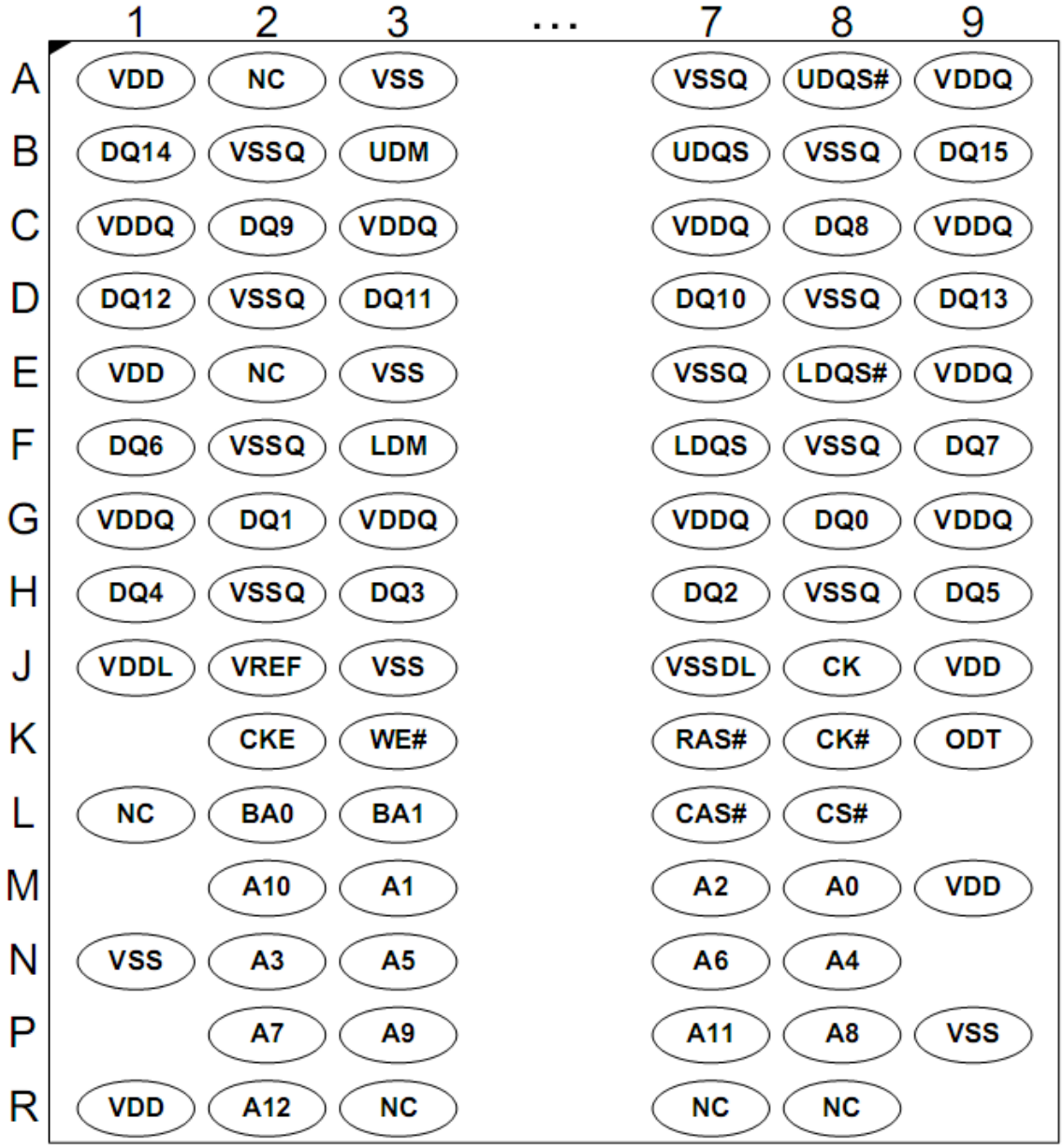
a) Key Features

• JEDEC Standard Compliant
• JEDEC standard 1.8V I/O (SSTL_18-compatible)
• Power supplies: VDD & VDDQ = +1.8V ± 0.1V
• Operating temperatue: 0 – 85 °C
• Supports JEDEC clock jitter specification
• Fully synchronous operation
• Fast clock rate: 333/400MHz
• Differential Clock, CK & CK#
• Bidirectional single/differential data strobe
-DQS & DQS#

• 4 internal banks for concurrent operation
• 4-bit prefetch architecture
• Internal pipeline architecture
• Precharge & active power down
• Programmable Mode & Extended Mode registers
• Posted CAS# additive latency (AL): 0, 1, 2, 3, 4, 5
• WRITE latency = READ latency - 1 tCK
• Burst lengths: 4 or 8
• Burst type: Sequential / Interleave
• DLL enable/disable
• Off-Chip Driver (OCD)
    -Impedance Adjustment
    -Adjustable data-output drive strength
• On-die termination (ODT)
• RoHS compliant
• Auto Refresh and Self Refresh
• 8192 refresh cycles / 64ms
• Package: 84-ball 10x12.5x1.2mm (max) FBGA
    - Pb and Halogen Free

The EM68B16C is a high-speed CMOS Double-Data-Rate-Two (DDR2), synchronous dynamic random-access memory (SDRAM) containing 512 Mbits in a 16-bit wide data I/Os. It is internally configured as a quad bank DRAM, 4 banks x 8Mb addresses x 16 I/Os The device is designed to comply with DDR2 DRAM key features such as posted CAS# with additive latency, Write latency = Read latency -1, Off-Chip Driver (OCD) impedance adjustment, and On Die Termination(ODT). All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and CK# falling) All I/Os are synchronized with a pair of bidirectional strobes (DQS and DQS#) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in RAS #, CAS# multiplexing style. Accesses begin with the registration of a Bank Activate command, and then it is followed by a Read or Write command. Read and write accesses to the DDR2 SDRAM are 4 or 8-bit burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Operating the four memory banks in an interleaved fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. A sequential and gapless data rate is possible depending on burst length, CAS# latency, and speed grade of the device.

b) Pinning


1 2 3 ... 7 8 9
A VDD NC VSS VSSQ UDQS# VDDQ
B DQ14 VSSQ UDM UDQS VSSQ DQ15
C VDDQ DQ9 VDDQ VDDQ DQ8 VDDQ
D DQ12 VSSQ DQ11 DQ10 VSSQ DQ13
E VDD NC VSS VSSQ LDQS# VDDQ
F DQ6 VSSQ LDM LDQS VSSQ DQ7
G VDDQ DQ1 VDDQ VDDQ DQ0 VDDQ
H DQ4 VSSQ DQ3 DQ2 VSSQ DQ5
J VDDL VREF VSS VSSDL CK VDD
K CKE WE# RAS# CK# ODT
L NC BA0 BA1 CAS# CS#
M A10 A1 A2 A0 VDD
N VSS A3 A5 A6 A4
P A7 A9 A11 A8 VSS
R VDD A12 NC NC NC

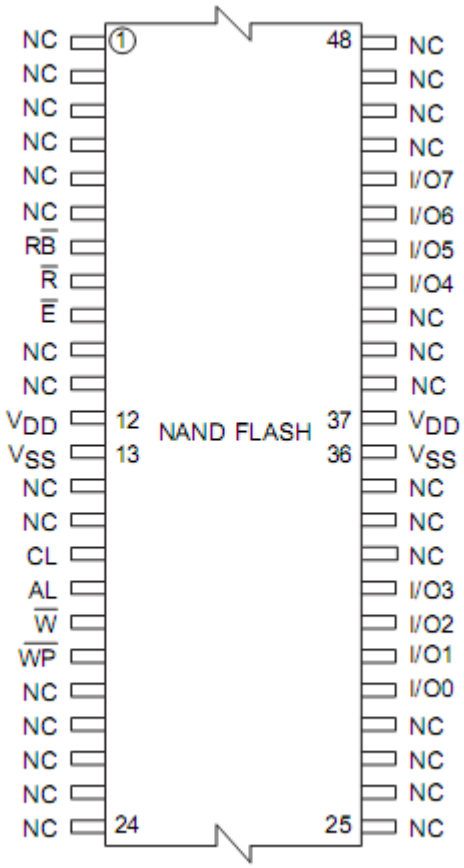
12. 4Gbit NAND Flash Memory (U35)

ST NAND04G-B2D

a) Key Features

■ High density NAND Flash Memory
– Up to 8 Gbit memory array
– Cost-effective solution for mass storage applications
■ NAND interface
– x8 or 16x bus width
– Multiplexed address/data
■ Supply voltage: 1.8 V or 3.0 V device
■ Page size
– x8 device: (2048 + 64 spare) bytes
– x16 device: (1024 + 32 spare) words
■ Block size
– x8 device: (128K + 4 K spare) bytes
– x16 device: (64K + 2 K spare) words
■ Multiplane architecture
– Array split into two independent planes
– Program/erase operations can be performed on both planes at the same time
■ Page read/program
– Random access: 25 µs (max)
– Sequential access: 25 ns (min)
– Page program time: 200 µs (typ)
– Multiplane page program time (2 pages): 200 µs (typ)
■ Copy back program with automatic error detection code (EDC)
■ Cache read mode
■ Fast block erase
– Block erase time: 1.5 ms (typ)
– Multiblock erase time (2 blocks): 1.5 ms (typ)
■ Status Register
■ Electronic signature
■ Chip Enable ‘don’t care’
■ Serial number option
■ High density NAND Flash Memory
– Up to 8 Gbit memory array
– Cost-effective solution for mass storage applications
■ NAND interface
– x8 or 16x bus width
– Multiplexed address/data
■ Supply voltage: 1.8 V or 3.0 V device
■ Page size
– x8 device: (2048 + 64 spare) bytes
– x16 device: (1024 + 32 spare) words
■ Block size
– x8 device: (128K + 4 K spare) bytes
– x16 device: (64K + 2 K spare) words
■ Multiplane architecture
– Array split into two independent planes
– Program/erase operations can be performed on both planes at the same time
■ Page read/program
– Random access: 25 µs (max)
– Sequential access: 25 ns (min)
– Page program time: 200 µs (typ)
– Multiplane page program time (2 pages): 200 µs (typ)
■ Copy back program with automatic error detection code (EDC)
■ Cache read mode
■ Fast block erase
– Block erase time: 1.5 ms (typ)
– Multiblock erase time (2 blocks): 1.5 ms (typ)
■ Status Register
■ Electronic signature
■ Chip Enable ‘don’t care’
■ Serial number option

b) Pinning



Signal	Function	Direction
I/O0-7	Data input/outputs, address inputs, or command inputs (x8/x16 devices)	Input/output
I/O8-15	Data input/outputs (x16 devices)	Input/output
AL	Address Latch Enable	Input
CL	Command Latch Enable	Input
$\overline{E}$	Chip Enable	Input
$\overline{R}$	Read Enable	Input
$R\overline{B}$	Ready/Busy (open-drain output)	Output
$\overline{W}$	Write Enable	Input
$\overline{WP}$	Write Protect	Input
V_{DD}	Supply Voltage	Power supply
V_{SS}	Ground	Ground
NC	Not connected internally	N/A
DU	Do not use	N/A

13. 128Mbit NAND Flash Memory (U17)

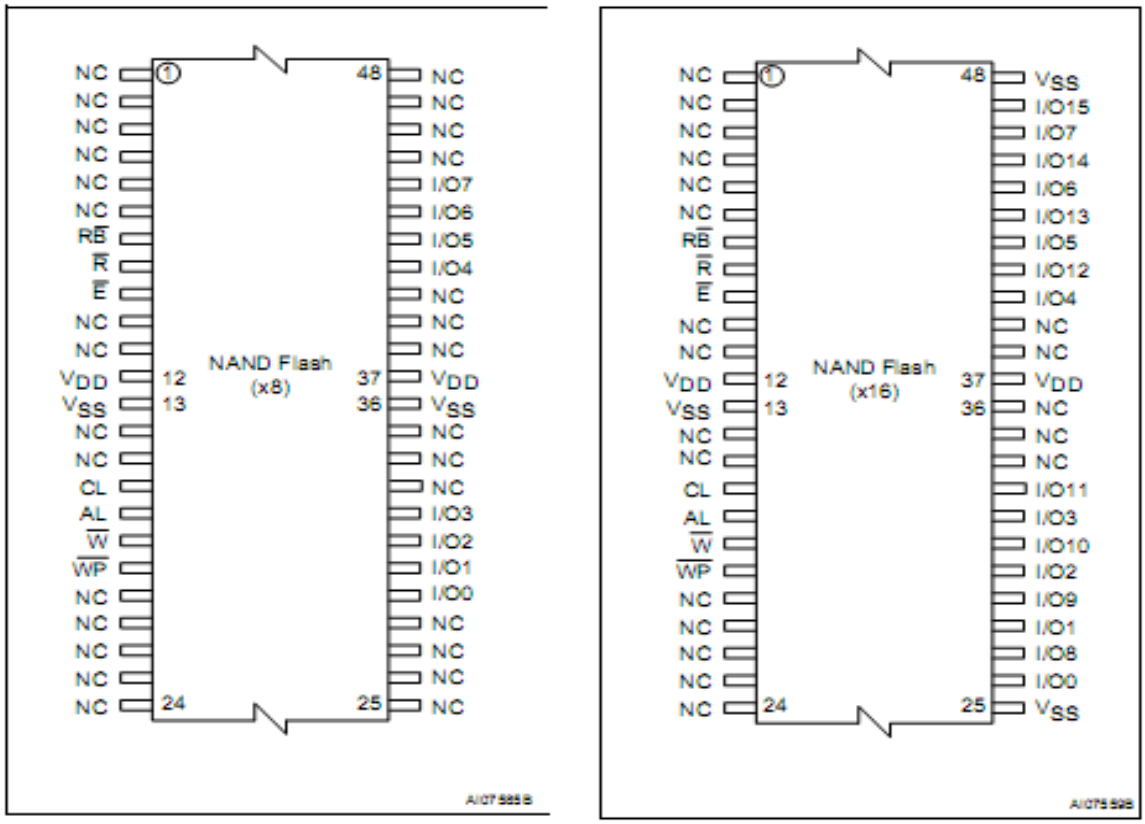
ST NAND128-A

a) Key Features

■ HIGH DENSITY NAND FLASH MEMORIES
– Up to 1 Gbit memory array
– Up to 32 Mbit spare area
– Cost effective solutions for mass storage applications
■ NAND INTERFACE
– x8 or x16 bus width
– Multiplexed Address/ Data
– Pinout compatibility for all densities
■ SUPPLY VOLTAGE
– 1.8V device: VDD = 1.7 to 1.95V
– 3.0V device: VDD = 2.7 to 3.6V
■ PAGE SIZE
– x8 device: (512 + 16 spare) Bytes
– x16 device: (256 + 8 spare) Words
■ BLOCK SIZE
– x8 device: (16K + 512 spare) Bytes
– x16 device: (8K + 256 spare) Words
■ PAGE READ / PROGRAM
– Random access: 12µs (max)
– Sequential access: 50ns (min)
– Page program time: 200µs (typ)
■ COPY BACK PROGRAM MODE
– Fast page copy without external buffering
■ FAST BLOCK ERASE
– Block erase time: 2ms (Typ)
■ STATUS REGISTER
■ ELECTRONIC SIGNATURE
■ CHIP ENABLE 'DON'T CARE' OPTION
– Simple interface with microcontroller
■ SERIAL NUMBER OPTION
■ HARDWARE DATA PROTECTION
– Program/Erase locked during Power Transitions
■ DATA INTEGRITY
– 100,000 Program/Erase cycles
– 10 years Data Retention
■ RoHS COMPLIANCE
– Lead-Free Components are Compliant with the RoHS Directive
■ DEVELOPMENT TOOLS
– Error Correction Code software and hardware models
– Bad Blocks Management and Wear Leveling algorithms
– File System OS Native reference software
– Hardware simulation models

b) Pinning

Signal	Function	Direction
I/O0-7	Data input/outputs, address inputs, or command inputs (x8/x16 devices)	Input/output
I/O8-15	Data input/outputs (x16 devices)	Input/output
AL	Address Latch Enable	Input
CL	Command Latch Enable	Input
$\overline{E}$	Chip Enable	Input
$\overline{R}$	Read Enable	Input
$R\overline{B}$	Ready/Busy (open-drain output)	Output
$\overline{W}$	Write Enable	Input
$\overline{WP}$	Write Protect	Input
V_{DD}	Supply Voltage	Power supply
V_{SS}	Ground	Ground
NC	Not connected internally	N/A
DU	Do not use	N/A

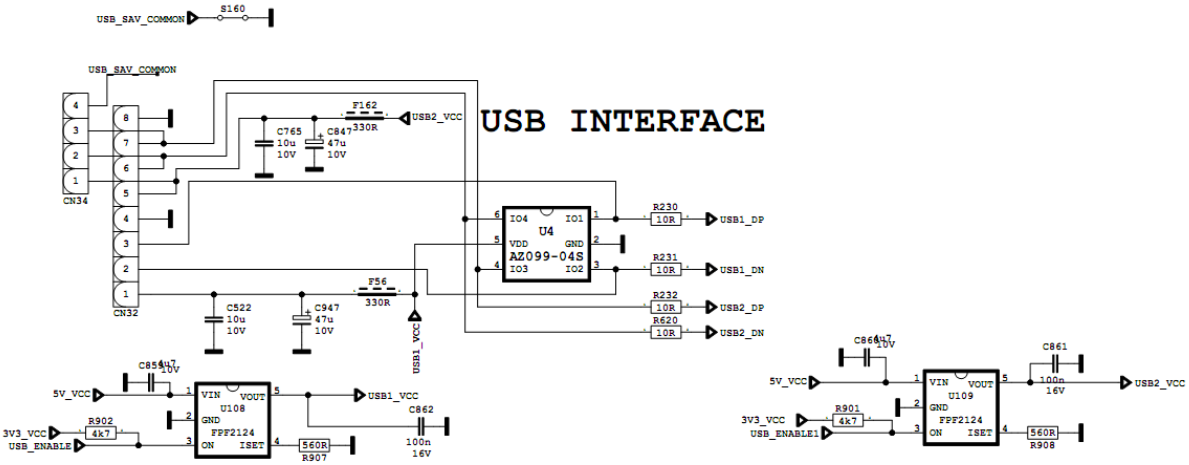


14. USB Interface

USB ports are directly connected concept IC, BCM 3556.

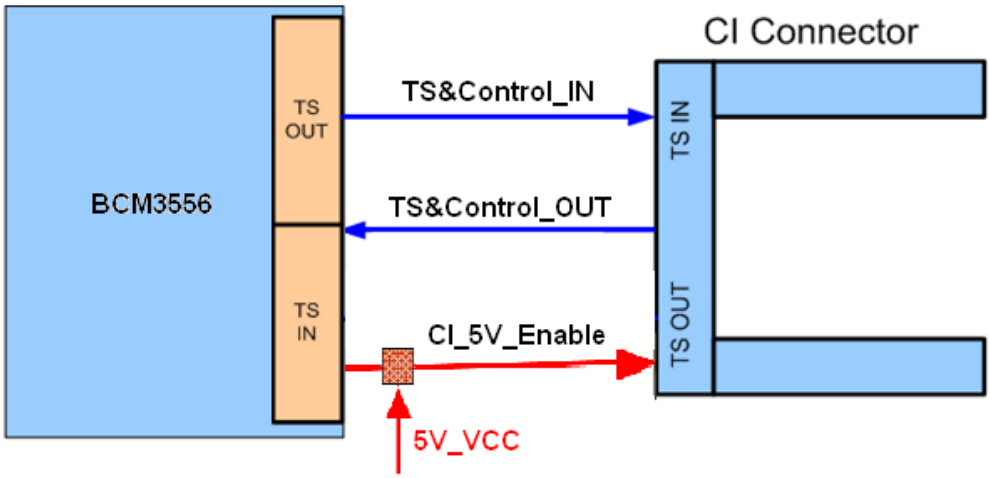
USB ciecuit has 2 main parts:

- Protection IC (U4)
- Over Curent Protection IC (U108-U109)



15. CI Interface

17MB70 Digital CI ve Smart Card Interface Block diagram:



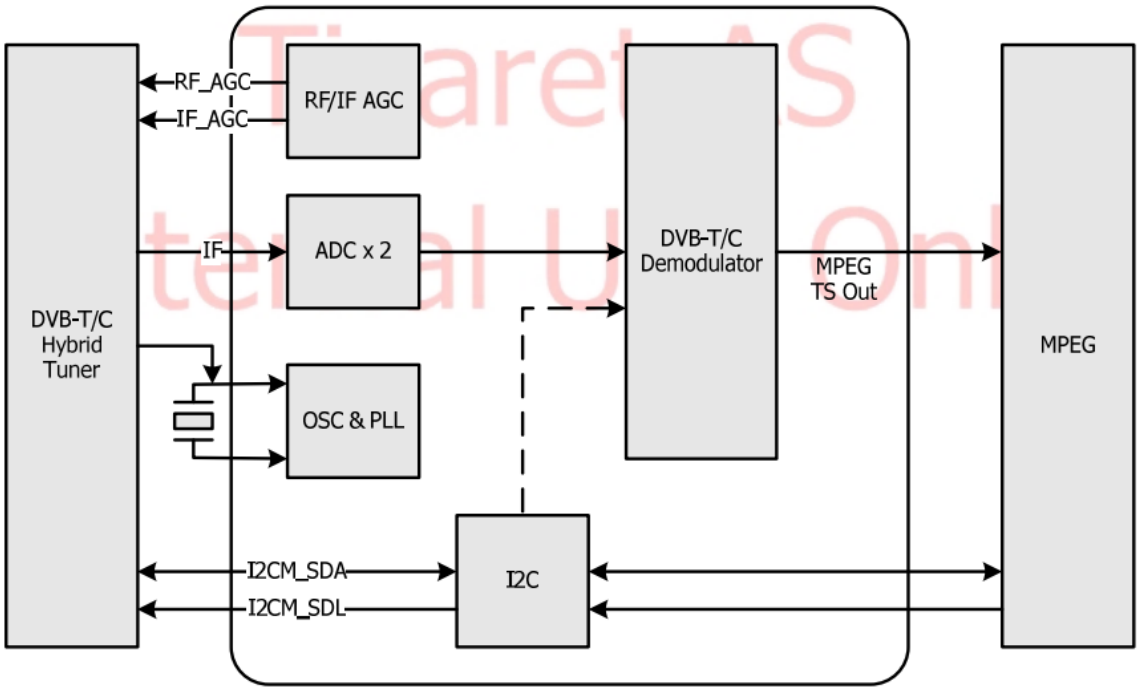
16. DVB-C Demodulator

Mstar MSB122C

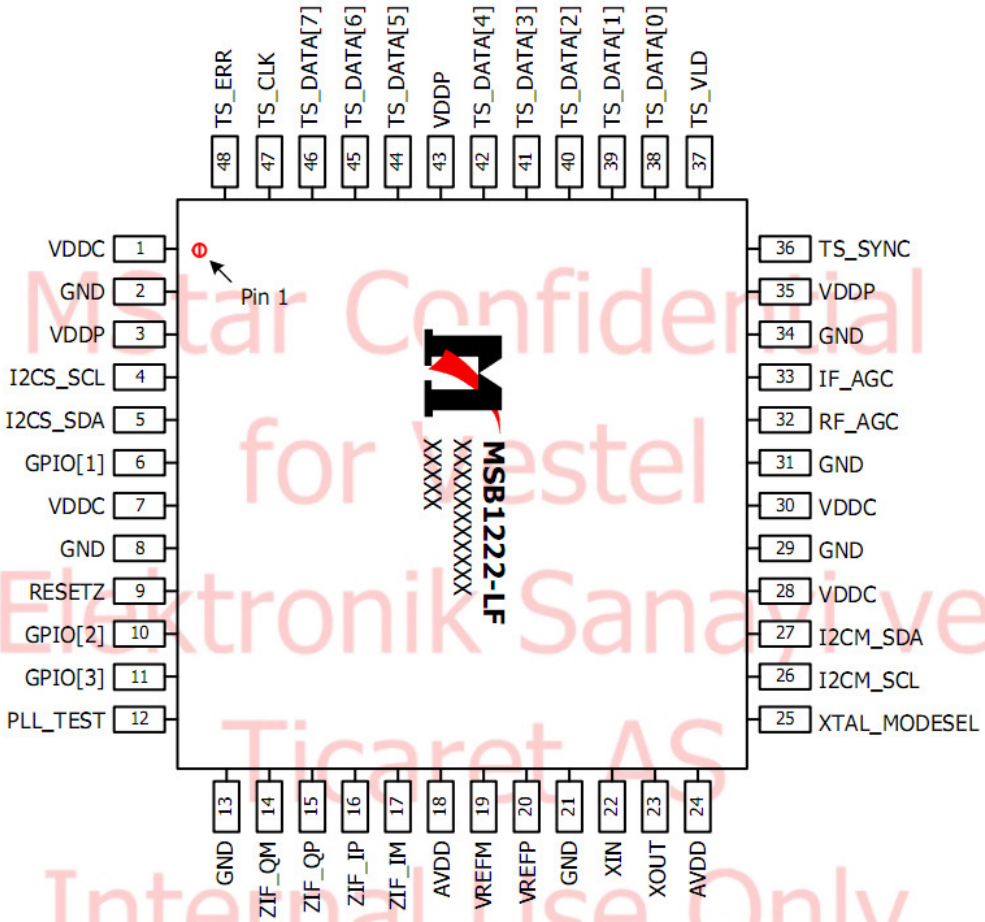
a) Key Features

- DVB-T Demodulator
  - Compliant with DVB-T(ETSI ET 300 744)
  - Supports 2K, 4K, 8K and 1/4, 1/8, 1/16, 1/32 guard interval (GI) and hierarchical, non-hierarchical modes
  - Nordig Unified 1.0.3/2.0, D-Book 5.0, E-Book compliant
  - All digital demodulation and timing recovery loops
  - CCI and ACI rejection capability
  - Impulse-Noise suppression
  - Advanced performance for SFN networks
  - Direct 36MHz, 44MHz IF sampling scheme from tuner
- DVB-C Demodulator
  - Compliant with DVB-C (EN300429) and ITU-T J.83 Annex A/C
  - Supports symbol rates up to 7M Baud
  - Blind acquisition of QAM constellations
  - Single IF filter bandwidth for all symbol rates
- Miscellaneous
  - Configurable parallel/serial MPEG-2 transport stream interface
  - Dual low-power, high-performance ADCs: accept IF, low IF, zero-IF inputs in 5, 6, 7, and 8MHz channel bandwidths from Hybrid tuner
  - Full-digital frequency offset recovery with wide acquisition range (+/-1MHz)
  - IQ imbalance compensation for ZIF
  - Clock generation from a single 20.48/24/28.8MHz crystal or tuner clock output
  - Supports single or dual AGC control
  - Supports I2C interface
  - Operating voltage: 3.3V and 1.2V
  - 48-pin LQFP package

b) Block Diagram



c) Pinning



Analog Interface

Pin Name	Pin Type	Function	Pin
PLL_TEST	Analog Output	PLL Test	12
IF_QM	Analog Input	ADC ZIF Q Negative Input	14
IF_QP	Analog Input	ADC ZIF Q Positive Input	15
IF_IP	Analog Input	ADC ZIF I Positive Input	16
IF_IM	Analog Input	ADC ZIF I Negative Input	17
VREFM	Analog Input	Reference Voltage	19
VREFP	Analog Input	Reference Voltage	20
XIN	Crystal Oscillator Input	Crystal Oscillator Input	22
XOUT	Crystal Oscillator Output	Crystal Oscillator Output	23

I2C Interface

Pin Name	Pin Type	Function	Pin
I2CS_SCL	Input w/ 5V-Tolerant	I2C Slave Clock	4
I2CS_SDA	I/O w/ 5V-Tolerant	I2C Slave Data	5
I2CM_SCL	I/O w/5V-tolerant	I2C Master Clock	26
I2CM_SDA	I/O w/5V-tolerant	I2C Master Data	27

Transport Stream Interface

Pin Name	Pin Type	Function	Pin
TS_SYNC	Output	Transport Stream Packet Start	36
TS_VLD	Output	Transport Stream Data Valid	37
TS_DATA[7:0]	Output	Transport Stream Data Output	46-44, 42-38
TS_CLK	Output	Transport Stream Clock Out	47
TS_ERR	Output	Transport Stream Block Error	48

Misc. Interface

Pin Name	Pin Type	Function	Pin
RESETZ	Input w/ 5V-tolerant	Chip Reset Input; active low	9
XTAL_MODESEL	Input	Crystal Oscillator Mode Select	25
RF_AGC	Output	RF Auto Gain Control (Up Gain Control)	32
IF_AGC	Output	IF Auto Gain Control (Down Gain Control)	33

Power Pins

Pin Name	Pin Type	Function	Pin
VDDC	1.2V Power	Digital Core Power	1, 7, 28, 30
VDDP	3.3V Power	Digital Input/Output Power	3, 35, 43
AVDD	2.8V/3.3V Power	Analog Power	18, 24
GND	Ground	Ground	2, 8, 13, 21, 29, 31, 34

GPIO Interface

Pin Name	Pin Type	Function	Pin
GPIO[1]	I/O w/ 5V-tolerant	General Purpose Input/Output	6
GPIO[2]	I/O w/ 5V-tolerant	General Purpose Input/Output	10
GPIO[3]	I/O w/ 5V-tolerant	General Purpose Input/Output	11

17. DVB-C/T2 Demodulator

Sony CXD2820R

a) Key Features

DESCRIPTION

The Sony CXD2820R is a combined DVB-T2, DVB-T and DVB-C demodulator that conforms to the ETSI EN 302-755 (second generation Terrestrial) ETSI EN 300-744 (Terrestrial) and ETSI EN 300-429 (Cable) standards.

The CXD2820R is a DVB-T2 demodulator offering class-leading performance, optimised BOM requiring no external memory and low processor overhead. It includes a highly integrated dual-core DVB-T and DVB-C demodulator which complies with all relevant European performance standards.

FEATURES DVB-T2

• Supports all DVB-T2 modes, including
• Single and multiple-PLPs
• SISO and MISO transmission
• Simple API
• Fully-automatic acquisition
• Fully-automatic L1-signalling decoding
• Automatic guard-interval detection
• Automatically-calculated constant-rate TS output (using L1 signalling and ISSY)
• Acquisition range ±857kHz
• Stream processor for automatic common- and data-PLP combination
• Null-packet insertion
• Access to channel echo profile and constellation via I2C

FEATURES DVB-C

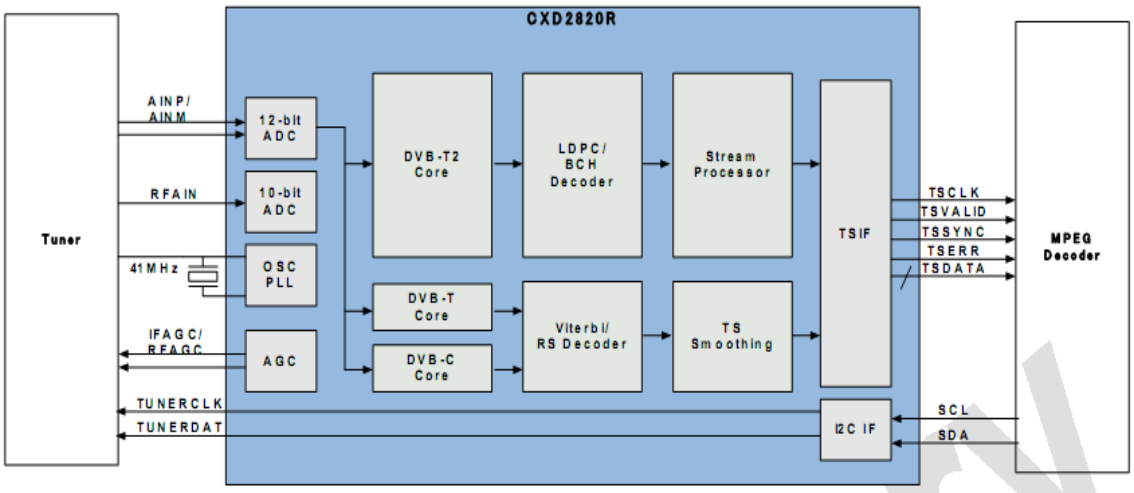
• Wide symbol range, 0.7 to 7.2Msym/s
• Integrated matched filter 0.15 roll-off factor
• Auto Acquisition controller with fast re-acquisition mode, 15ms typ.

• Programmable acquisition range ±500kHz
• 2.8us echo cancellation at 7.2Msym/s
• Low impl. loss 0.4dB @ 64QAM and <1.0dB @ 256QAM typ.
• Enhanced channel scanning performance through improved rejection of non-digital signals
• Access to channel SNR, constellation data and dynamic equaliser tap values via I2C

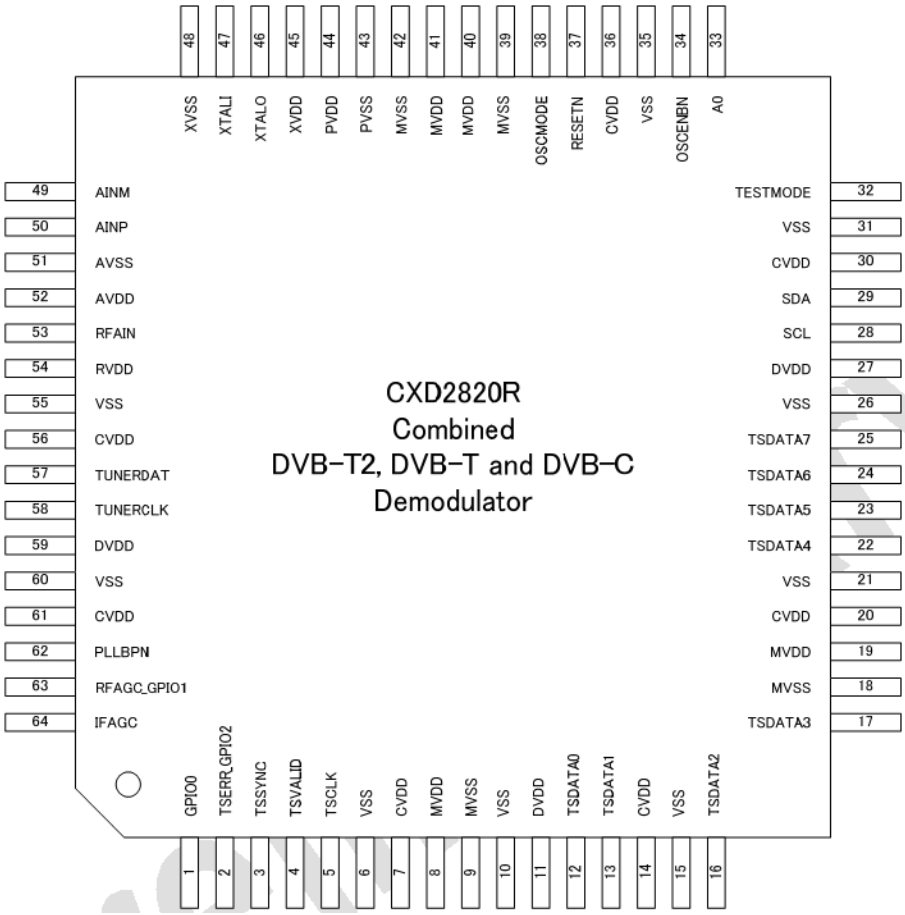
APPLICATIONS
• Set Top Boxes
• IDTV with Digital only or Hybrid Tuner Support
• PC TV
• PVRs and recordable DVD players
• Test equipment

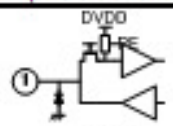
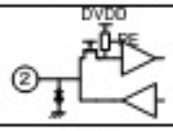
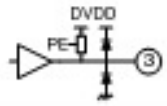
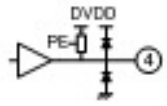
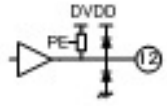
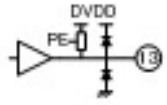
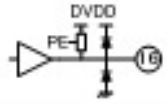
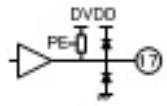
GENERAL FEATURES
• Single, 41MHz crystal (can be shared with CXD2813R analogue demod IC)
• High performance differential signal ADC
• RF power level monitor ADC
• Low IF and high IF (36MHz) mode input
• Fast 400kHz I2C compatible bus interface
• Quiet I2C interface for dedicated tuner control
• Automatic IF AGC and optional programmable
RF AGC/GPIO functions
• Configurable parallel and serial MPEG-2 TS outputs with smoothing buffer
• 3.3V, 2.5V, 1.2V supplies
• Temperature range -20°C to +85°C
• 64 pin exposed-pad LQFP 10mm x 10mm package
• Supplied with full reference design, including software driver, PCB schematic/layouts, GUI and documentation

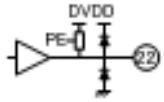
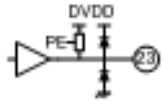
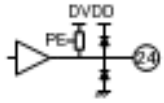
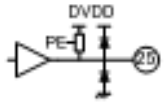
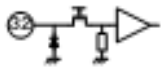
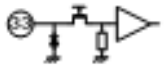
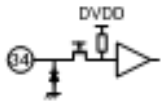
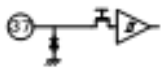
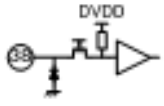
b) Block Diagram

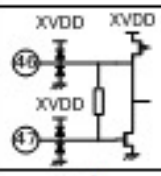
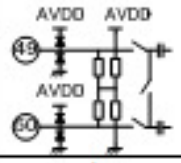
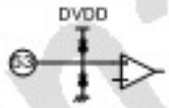
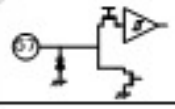
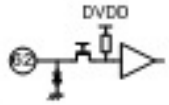
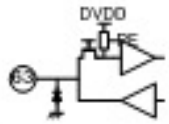
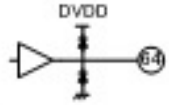


c) Pinning


CXD2820R
Combined
DVB-T2, DVB-T and DVB-C
Demodulator
1 GPIO0
2 TSERR_GPIO2
3 TSSYNC
4 TSVALID
5 TSCLK
6 VSS
7 CVDD
8 MVDD
9 MVSS
10 VSS
11 DVDD
12 TSDATA0
13 TSDATA1
14 CVDD
15 VSS
16 TSDATA2
17 TSDATA3
18 MVSS
19 MVDD
20 CVDD
21 VSS
22 TSDATA4
23 TSDATA5
24 TSDATA6
25 TSDATA7
26 VSS
27 DVDD
28 SCL
29 SDA
30 CVDD
31 VSS
32 TESTMODE
33 A0
34 OSCENBIN
35 VSS
36 CVDD
37 RESETN
38 OSCMODE
39 MVSS
40 MVDD
41 MVDD
42 MVSS
43 PVSS
44 PVDD
45 XVDD
46 XTALO
47 XTALI
48 XVSS
49 AINM
50 AINP
51 AVSS
52 AVDD
53 RFAIN
54 RVDD
55 VSS
56 CVDD
57 TUNERDAT
58 TUNERCLK
59 DVDD
60 VSS
61 CVDD
62 PLLBPN
63 RFAGC_GPIO1
64 IFAGC

Name	No.	I/O	Function	Equivalent Circuit	Note
GPIO0	1	I/O	General purpose I/O		5V tolerant Controllable pull-up
TSERR _GPIO2	2	O	TS error flag General purpose I/O		5V tolerant Controllable pull-up
TSSYNC	3	O	TS sync flag		Controllable pull-up Selectable output current
TSVALID	4	O	TS valid flag		Controllable pull-up Selectable output current
TSCLK	5	O	TS clock output		Controllable pull-up Selectable output current
VSS	6	–	Digital Ground	n/a	
CVDD	7	–	1.2V digital power supply	n/a	
MVDD	8	–	1.2V digital power supply	n/a	Supplies memory power
MVSS	9	–	Digital Ground	n/a	
VSS	10	–	Digital Ground	n/a	
DVDD	11	–	3.3V digital power supply	n/a	
TSDATA0	12	O	TS data output		Controllable pull-up Selectable output current
TSDATA1	13	O	TS data output		Controllable pull-up Selectable output current
CVDD	14	–	1.2V digital power supply	n/a	
VSS	15	–	Digital Ground	n/a	
TSDATA2	16	O	TS data output		Controllable pull-up Selectable output current
TSDATA3	17	O	TS data output		Controllable pull-up Selectable output current
MVSS	18	–	Digital Ground	n/a	
MVDD	19	–	1.2V digital power supply	n/a	Supplies memory power
CVDD	20	–	1.2V digital power supply	n/a	
VSS	21	–	Digital Ground	n/a	

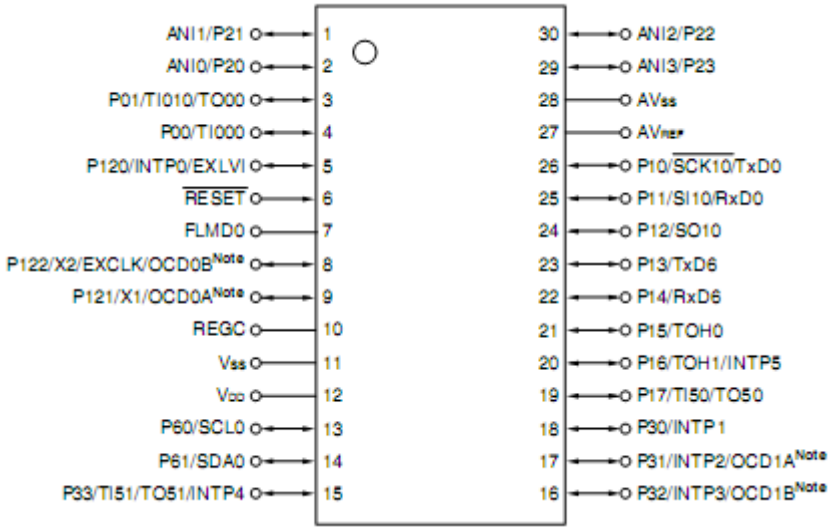
Name	No.	I/O	Function	Equivalent Circuit	Note
TSDATA4	22	O	TS data output		Controllable pull-up Selectable output current
TSDATA5	23	O	TS data output		Controllable pull-up Selectable output current
TSDATA6	24	O	TS data output		Controllable pull-up Selectable output current
TSDATA7	25	O	TS data output		Controllable pull-up Selectable output current
VSS	26	–	Digital Ground	n/a	
DVDD	27	–	3.3V digital power supply	n/a	
SCL	28	I	I^2C clock		5V tolerant
SDA	29	I/O	I^2C data		5V tolerant
CVDD	30	–	1.2V digital power supply	n/a	
VSS	31	–	Digital Ground	n/a	
TESTMODE	32	I	Test mode setting		5V tolerant 1: Test mode 0: Normal mode
A0	33	I	I^2C slave address selection		5V tolerant
OSCENBN	34	I	Oscillator enable		5V tolerant 1: Stop 0: Run
VSS	35	–	Digital Ground	n/a	
CVDD	36	–	1.2V digital power supply	n/a	
RESETN	37	I	Hardware reset		5V tolerant
OSCMODE	38	I	3rd overtone crystal selection		5V tolerant 1: fundamental 0: 3rd overtone
MVSS	39	–	Digital Ground	n/a	
MVDD	40	–	1.2V digital power supply	n/a	Supplies memory power
MVDD	41	–	1.2V digital power	n/a	Supplies memory power

Name	No.	I/O	Function	Equivalent Circuit	Note
			supply		
MVSS	42	–	Digital Ground	n/a	
PVSS	43	–	Analog Ground	n/a	
PVDD	44	–	1.2V analog power supply	n/a	Supplies PLL power
XVDD	45	–	2.5V analog power supply	n/a	Supplies crystal oscillator power
XTALO	46	O	Crystal oscillator output		Leave open when external clock input to XTALI
XTALI	47	I	Crystal oscillator input		External clock input pin
XVSS	48	–	Analog Ground	n/a	
AINM	49	I	IF input (-)		
AINP	50	I	IF input (+)		
AVSS	51	–	Analog Ground	n/a	
AVDD	52	–	2.5V analog power supply	n/a	Supplies IF ADC power
RFAIN	53	I	RF level monitor		
RVDD	54	–	3.3V digital power supply (*1)	n/a	Supplies RF level monitor ADC power
VSS	55	–	Digital Ground	n/a	
CVDD	56	–	1.2V digital power supply	n/a	
TUNERDAT	57	I/O	Tuner I²C data		5V tolerant
TUNERCLK	58	O	Tuner I²C clock		5V tolerant
DVDD	59	–	3.3V digital power supply	n/a	
VSS	60	–	Digital Ground	n/a	
CVDD	61	–	1.2V digital power supply	n/a	
PLLBPN	62	I	PLL bypass		5V tolerant 1: Use PLL 0: Bypass PLL
RFAGC_GPIO1	63	I/O	RFAGC output General purpose I/O		PWM output 5V tolerant Controllable pull-up CAUTION: intermediate voltage input is prohibited.
IFAGC	64	O	IFAGC output		PWM output CAUTION: 5V input is prohibited.

18. LOW POWER&CEC MICROCONTROLLER

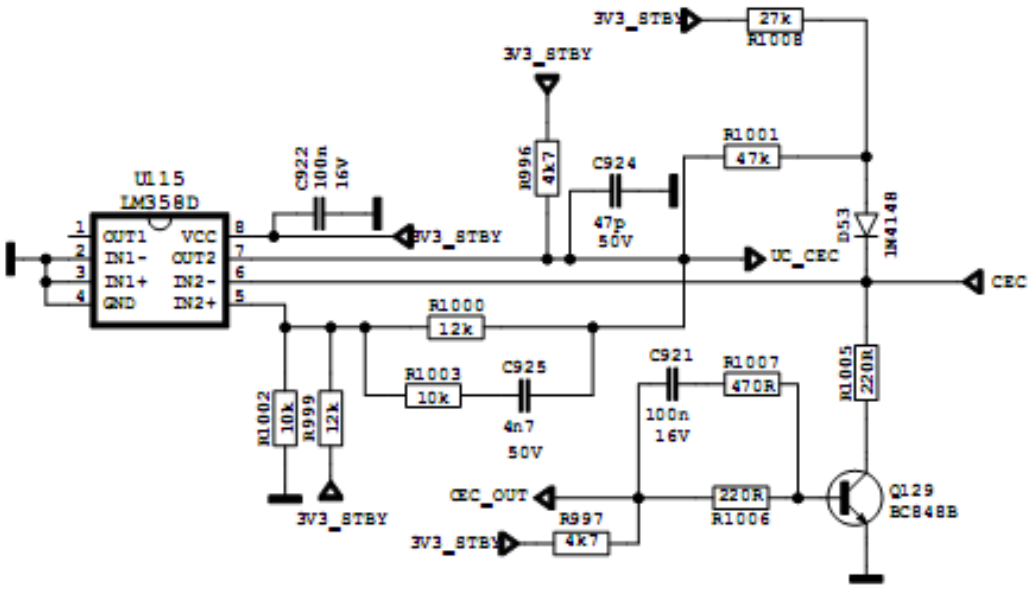
NEC uPD78F0503

Pinning



ANI0 to ANI3:	Analog input	P60, P61:	Port 6
AVREF:	Analog reference voltage	P120 to P122:	Port 12
AVss:	Analog ground	REGC	Regulator capacitance
EVDD Note 1:	Power supply for port	RESET:	Reset
EVss Note 1:	Ground for port	RxD0, RxD6:	Receive data
EXCLK:	External clock input	SCK10:	Serial clock input/output
	(main system clock)	SCL0:	Serial clock input/output
EXLVI:	External potential input	SDA0:	Serial data input/output
	for low-voltage detector	SI10:	Serial data input
FLMD0:	Flash programming mode	SO10:	Serial data output
INTP0 to INTP5:	External interrupt input	TI000, TI010,	
NC Notes 1, 2:	Non-connection	TI50, TI51:	Timer input
OCD0A Note 3,		TO00,	
OCD0B Note 3,		TO50, TO51,	
OCD1A Note 3,		TOH0, TOH1:	Timer output
OCD1B Note 3:	On chip debug input/output	TxD0, TxD6:	Transmit data
P00, P01:	Port 0	VDD:	Power supply
P10 to P17:	Port 1	Vss:	Ground
P20 to P23:	Port 2	X1, X2:	Crystal oscillator (main system clock)
P30 to P33:	Port 3		

CEC Circuit Design for CEC option:



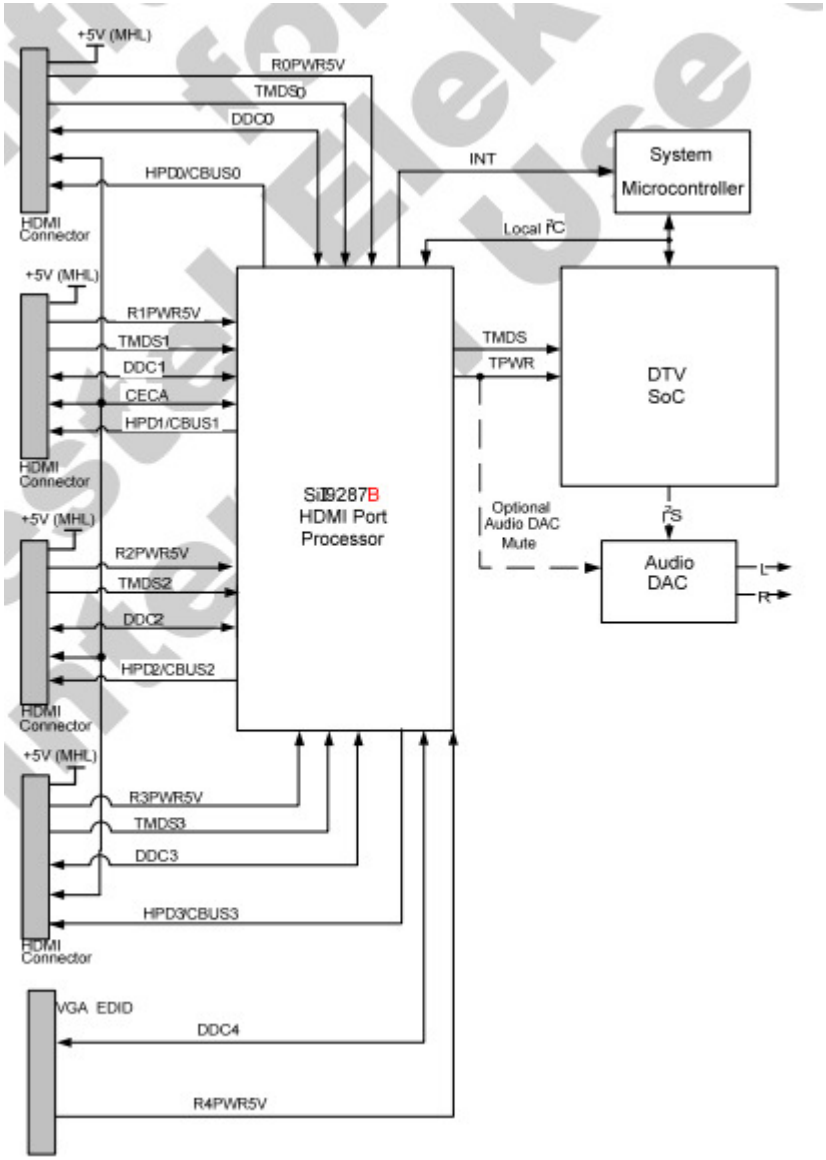
19. HDMI SWITCH

Silicon Image SiI9287B

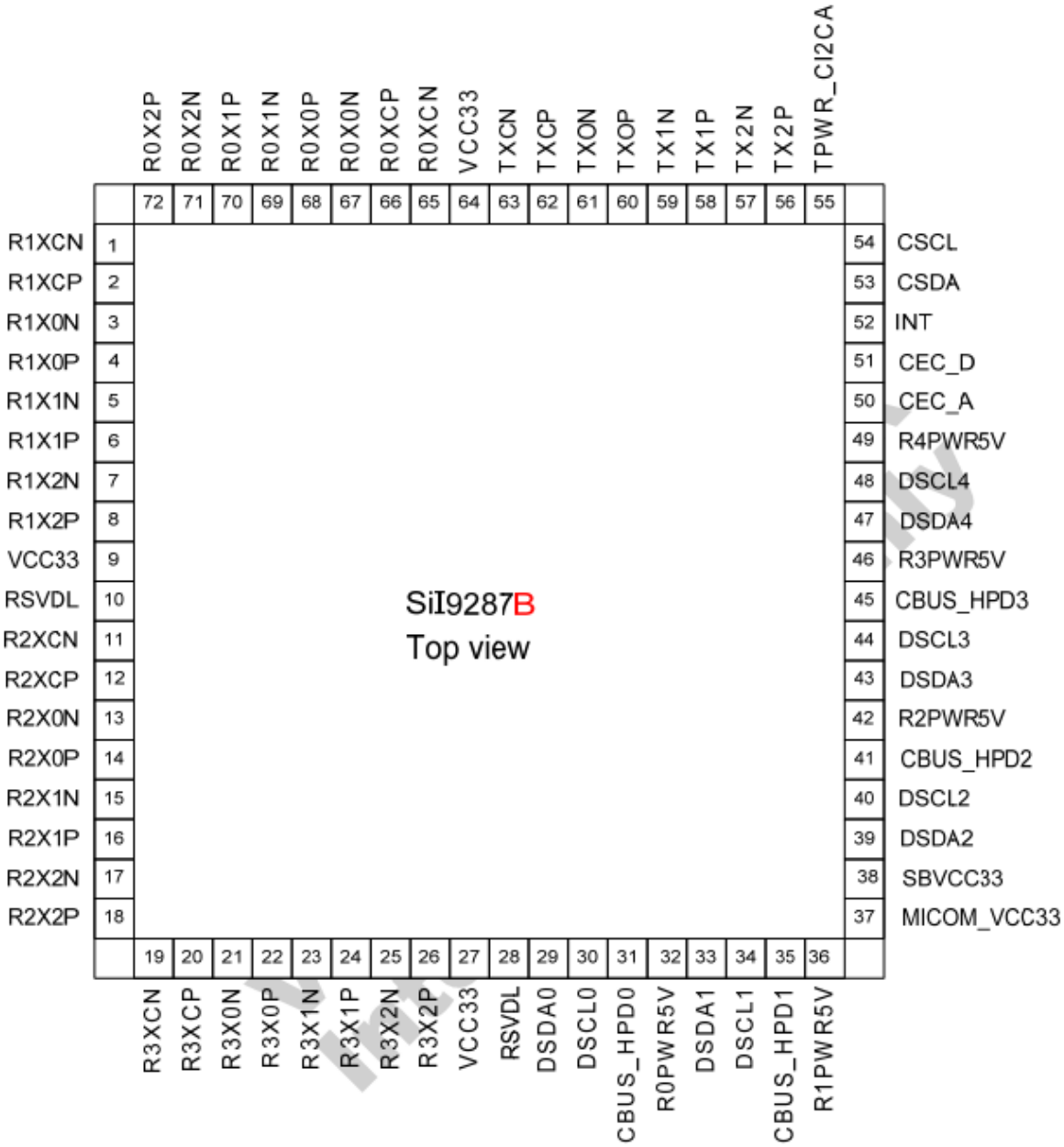
a) Key Features

x Four-input, single-output HDMI port processor
x Improved ESD protection on all signals connected to HDMI connector
x Integrated TMDS receiver and transmitter cores capable of receiving and transmitting at 2.25 Gbps:
x InstaPort™ viewing technology
x MHL support
x Supports video resolutions up to 1080p, 60 Hz, 12-
bit or 720p/1080i, 120 Hz, 12-bit
x Built-in adaptive equalizer provides long cable support even at Deep Color resolutions, enabling the SiI9287B device to work with noisy signals and many sources, making the sink devices highly interoperable
x Receiver fully complies with DVI 1.0, HDCP 1.3 and HDMI 1.3a specifications.

b) Block Diagram



c) Pinning


R0X2P 72
R0X2N 71
R0X1P 70
R0X1N 69
R0X0P 68
R0X0N 67
R0XCP 66
R0XCN 65
VCC33 64
TXCN 63
TXCP 62
TXON 61
TXOP 60
TX1N 59
TX1P 58
TX2N 57
TX2P 56
TPWR_CI2CA 55
R1XCN 1
R1XCP 2
R1X0N 3
R1X0P 4
R1X1N 5
R1X1P 6
R1X2N 7
R1X2P 8
VCC33 9
RSVDL 10
R2XCN 11
R2XCP 12
R2X0N 13
R2X0P 14
R2X1N 15
R2X1P 16
R2X2N 17
R2X2P 18
SiI9287B
Top view
54 CSCL
53 CSDA
52 INT
51 CEC_D
50 CEC_A
49 R4PWR5V
48 DSCL4
47 DSDA4
46 R3PWR5V
45 CBUS_HPD3
44 DSCL3
43 DSDA3
42 R2PWR5V
41 CBUS_HPD2
40 DSCL2
39 DSDA2
38 SBVCC33
37 MICOM_VCC33
19 R3XCN
20 R3XCP
21 R3X0N
22 R3X0P
23 R3X1N
24 R3X1P
25 R3X2N
26 R3X2P
27 VCC33
28 RSVDL
29 DSDA0
30 DSCL0
31 CBUS_HPD0
32 R0PWR5V
33 DSDA1
34 DSCL1
35 CBUS_HPD1
36 R1PWR5V

HDMI Receiver and MHL Port Pins

Pin Name	Pin	Type	Dir	Description
R0X0P	68	TMDS	Input	TMDS input Port 0 data pair for HDMI and MHL.
R0X0N	67			
R0X1P	70	TMDS	Input	TMDS input Port 0 data pairs for HDMI.
R0X1N	69			
R0X2P	72			
R0X2N	71			
R0XCP	66	TMDS	Input	TMDS input Port 0 clock pair for HDMI and MHL.
R0XCN	65			
R1X0P	4	TMDS	Input	TMDS input Port 1 data pair for HDMI and MHL.
R1X0N	3			
R1X1P	6	TMDS	Input	TMDS input Port 1 data pairs for HDMI.
R1X1N	5			
R1X2P	8			
R1X2N	7			
R1XCP	2	TMDS	Input	TMDS input Port 1 clock pair for HDMI and MHL.
R1XCN	1			
R2X0P	14	TMDS	Input	TMDS input Port 2 data pair for HDMI and MHL.
R2X0N	13			
R2X1P	16	TMDS	Input	TMDS input Port 2 data pairs for HDMI.
R2X1N	15			
R2X2P	18			
R2X2N	17			
R2XCP	12	TMDS	Input	TMDS input Port 2 clock pair for HDMI and MHL.
R2XCN	11			
R3X0P	22	TMDS	Input	TMDS input Port 3 data pair for HDMI and MHL.
R3X0N	21			
R3X1P	24	TMDS	Input	TMDS input Port 3 data pairs for HDMI.
R3X1N	23			
R3X2P	26			
R3X2N	25			
R3XCP	20	TMDS	Input	TMDS input Port 3 clock pair for HDMI and MHL.
R3XCN	19			

HDMI Transmitter Port Pins

Signal Name	Pin	Type	Dir	Description
TX0P	60	TMDS	Output	HDMI Output Port Data. TMDS Low Voltage Differential Signal output data pairs.
TX0N	61			
TX1P	58			
TX1N	59			
TX2P	56			
TX2N	57			
TXCP	62	TMDS	Output	HDMI Output Port Clock. TMDS Low Voltage Differential Signal output clock pair.
TXCN	63			

System Switching Pins

Pin Name	Pin	Type	Dir	Description
DSDA0 DSDA1 DSDA2 DSDA3	29 33 39 43	LVTTL Schmitt Open drain 5-V tolerant	Input Output	DDC I^2C Data for respective port. These signals are true open drain, and do not pull-down to ground when power is not applied to the device. These pins require an external pull-up resistor.
DSCL0 DSCL1 DSCL2 DSCL3	30 34 40 44	LVTTL Schmitt Open drain 5-V tolerant	Input	DDC I^2C Clock for respective port. These signals are true open drain, and do not pull-down to ground when power is not applied to the device. These pins require an external pull-up resistor.
R0PWR5V R1PWR5V R2PWR5V R3PWR5V	32 36 42 46	Power	Input	5V Port detection input for respective port. Connect to 5V signal from HDMI input connector. These signals require a 10 Ω series resistor and at least a 1 µF capacitor to ground. A 100 kΩ pull-down resistor is also required for these signals.
CBUS_HPD0 CBUS_HPD1 CBUS_HPD2 CBUS_HPD3	31 35 41 45	LVTTL 5-V tolerant	Output	Hot Plug Detect Output for respective port. Connect to HOTPLUG of HDMI input connector. In MHL mode, this serves as the respective port control bus.
R4PWR5V	49	Power	Input	5V Standby power or 5V power from 5th Receiver port. If this signal is connected to the VGA cable then it requires a 10 ohm series resistor and at least a 1 µF capacitor to ground. If connected to a local power supply the resistor is not needed but a capacitor of at least 1 µF is recommended.

Control Pins

Pin Name	Pin	Type	Dir	Description
CSCL	54	Schmitt Open drain 5-V tolerant	Input	Local Configuration/Status I^2C Clock. Chip configuration/status is accessed using this I^2C port. This pin is a true open drain, so it does not pull to ground if power is not applied.
CSDA	53	LVTTL Schmitt Open drain 5-V tolerant	Input Output	Local Configuration/Status I^2C Data. Chip configuration/status is accessed using this I^2C port. This pin is a true open drain, so it does not pull to ground if power is not applied.
DSCL4	48	LVTTL Schmitt 5-V tolerant	Input	DDC I^2C Clock for VGA port. These signals are true open drain, and do not pull-down to ground when power is not applied to the device. This pin requires an external pull-up resistor.
DSDA4	47	LVTTL Schmitt 5-V tolerant	Input output	DDC I^2C Data for VGA port. These signals are true open drain, and do not pull-down to ground when power is not applied to the device. This pin requires an external pull-up resistor.

Configuration Pins

Pin Name	Pin	Type	Dir	Description
TPWR_CI2CA	55	LVTTL 8 mA 5-V tolerant	Input Output	I^2C Slave Address input / Transmit Power Sense Output. At the end of power-on-reset (POR), this pin is used as an input to latch the I^2C sub-address. The level on this pin is latched when the POR transitions from the asserted state to the de-asserted state. After completion of POR, this pin is used as the TPWR output, indicating that the selected HDMI input port is receiving an active TMDS clock. This pin has an internal pull-up to the MICOMVCC33 power supply. If this signal is pulled-down, a 4.7K ohm resistor should be used.
INT	52	Schmitt Open drain 8 mA 5-V tolerant	Input Output	Interrupt Output. This is an open-drain output and requires an external pull-up resistor.
RSVDL RSVDL	10 28	Reserved pin	—	These pins must be tied to ground with a 10 kΩ or less resistor during normal operation. Connecting directly to ground is recommended.

CEC Pins

Pin Name	Pin	Type	Direction	Description
CEC_A	50	CEC Compliant 5-V tolerant	Input Output	HDMI compliant CEC I/O used for interfacing to CEC devices. This signal is electrically compliant with the CEC specification. It connects to the CEC signal of all HDMI connectors in the system. As an input, this pin acts as a LVTTL Schmitt triggered input and is 5-V tolerant. As an output, the pin acts as an NMOS driver with resistive pull-up. This pin has an internal pull-up resistor.
CEC_D	51	LVTTL Schmitt Open drain 5-V tolerant	Input Output	CEC interface to local system. This pin is an open drain and requires an external pull-up resistor. This pin typically connects to a local CPU if the CEC functions are performed by the CPU directly, and not the CEC controller inside the device.

Power and Ground Pins

Signal Name	Pin	Type	Description
VCC33	9, 27, 64	Power	Analog and digital core VCC. Must be supplied at 3.3 V.
MICOM_VCC33	37	Output	During normal mode, this pin provides 3.3 V power to an external microcontroller. The maximum output current is 30 mA. This pin requires 1 µF capacitor to ground.
SBVCC33	38	Power	3.3 V standby power. If 3.3 V standby mode is not used, this pin should be left as not connected.
ePAD	ePad	Ground	**ePad must be connected to Ground.** All analog and digital ground planes are tied together to the ePad, which ***must*** be connected to Ground.

20. LNB supply and control IC

ST LNBH23L

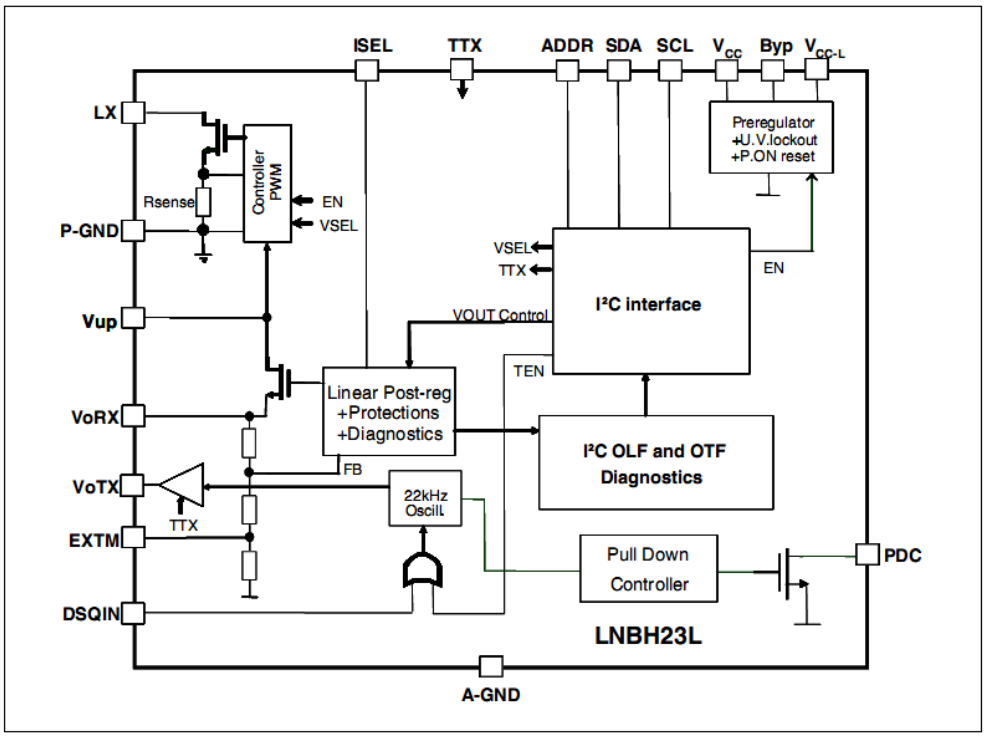
a) Key Features

■ Complete interface between LNB and I²C bus
■ Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93% @0.5 A)
■ Selectable output current limit by external resistor
■ Compliant with main satellite receivers output voltage specification
■ Auxiliary modulation input (EXTM pin) facilitates DiSEqC™ 1.X encoding
■ Accurate built-in 22 kHz tone generator suits widely accepted standards
■ Low-drop post regulator and high efficiency step-up PWM with integrated power NMOS allow low power losses
■ Overload and over-temperature internal protections with I²C diagnostic bits
■ LNB short circuit dynamic protection
■ +/- 4 kV ESD tolerant on output power pins

Applications
■ STB satellite receivers
■ TV satellite receivers
■ PC card satellite receivers

Description
Intended for analog and digital satellite receivers, the LNBH23L is a monolithic voltage regulator and interface IC, assembled in QFN32 5 x 5 specifically designed to provide the 13 / 18 V power supply and the 22 kHz tone signalling to the LNB down-converter in the antenna dish or to the multi-switch box. In this application field, it offers a complete solution with extremely low component count, low power dissipation together with simple design and I²C standard interfacing.

b) Block Diagram



21. Software Update

In MB70 project you can update the main IC software by using USB ports. You can find the SW update procedure below.

1. Software files should copy directly inside of a flash memory(not in a folder).
2. Put flash memory to the tv when tv is powered off.
3. Power on the and wait. TV will power-up itself.
4. If First Time Installition screen comes, it means software update procedure is succesful.
5. You can check the SW release name from service menu.

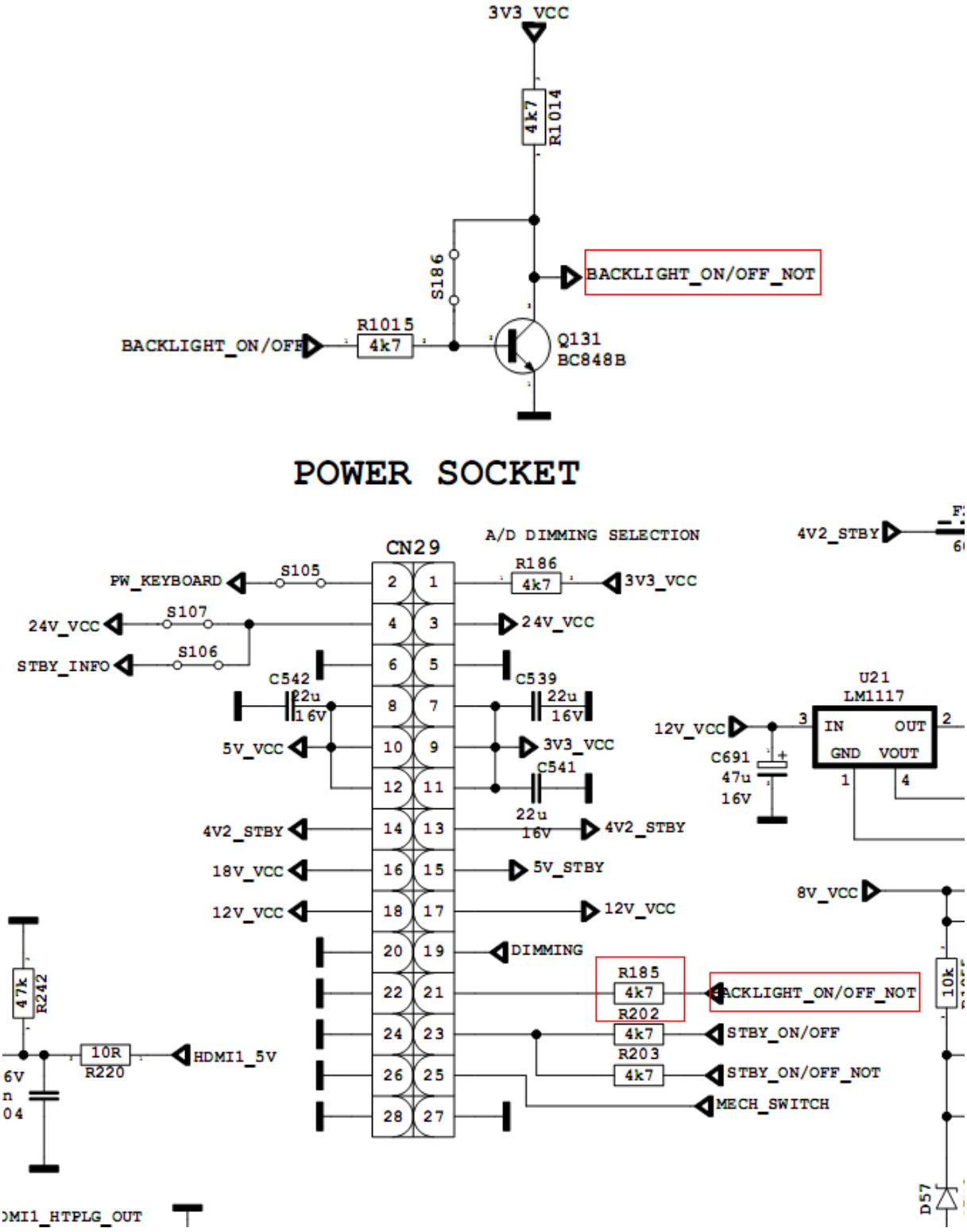
22. Troubleshooting

A. No Backlight Problem

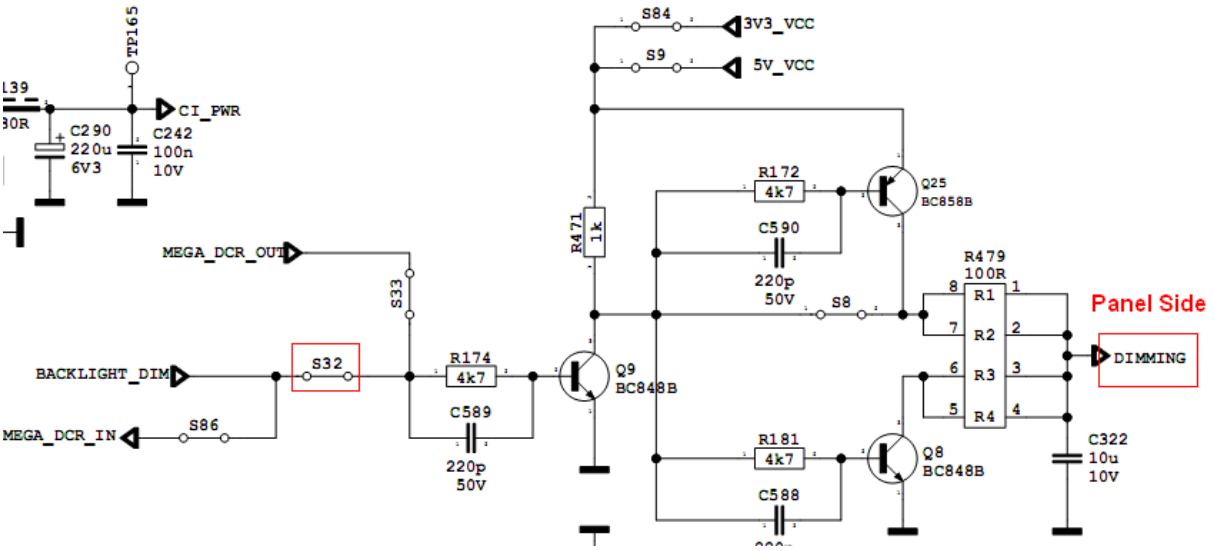
Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible couses: Backlight pin, dimming pin, backlight supply, stby on/off pin

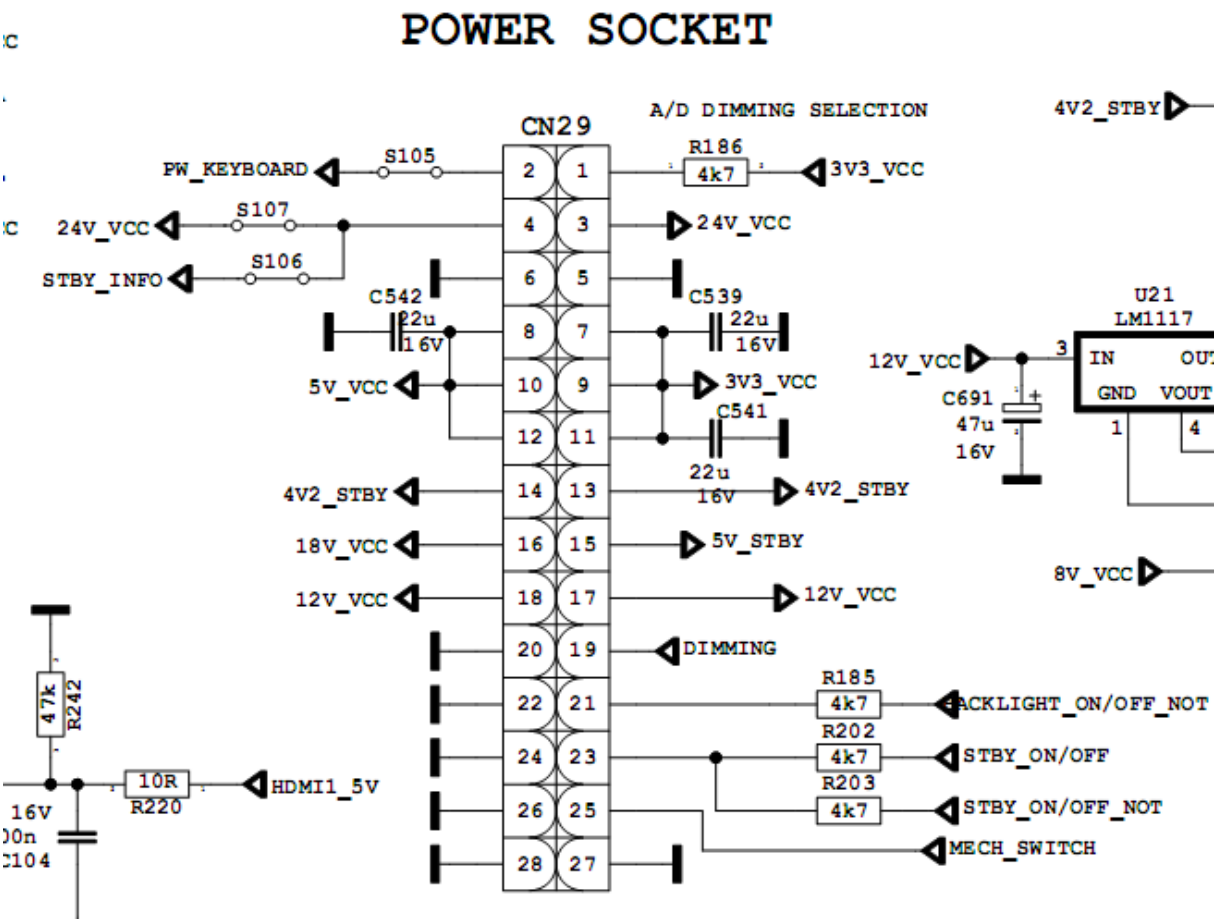
BACKLIGHT_ON/OFF pin should be high when the backlight is ON. R185 must be low when the backlight is OFF. If it is a problem, please check Q131 and the panel cables.



Dimming pin should be high or square wave in open position. If it is low, please check S32 for BRCM side and panel or power cables, connectors.



STBY_ON/OFF_NOT should be high for standby condition, please check R203.

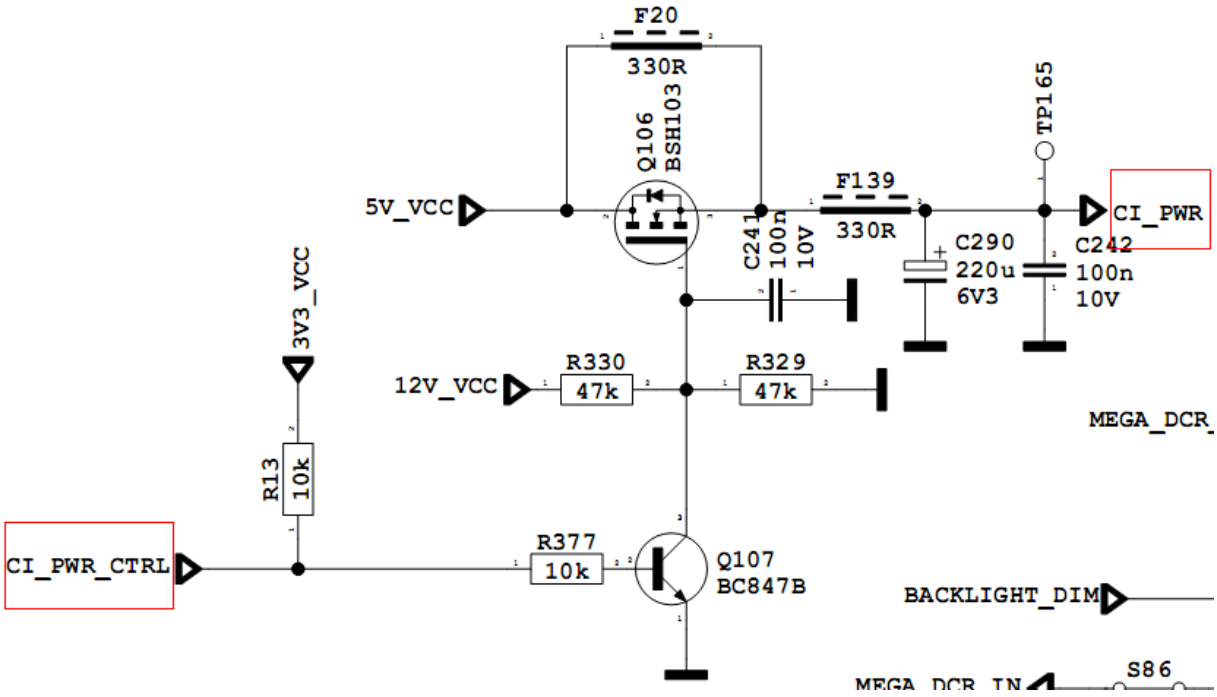


B. CI Module Problem

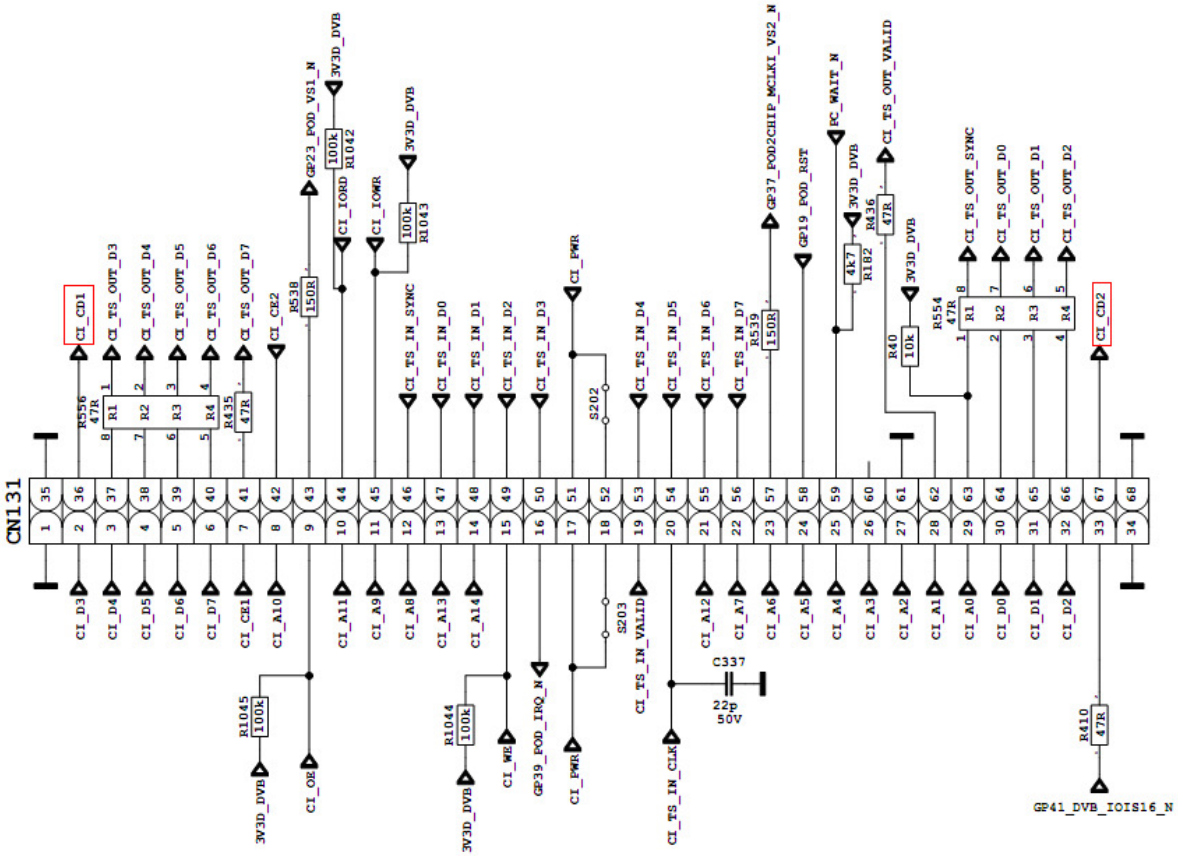
Problem: CI is not working when CI module inserted.

Possible couses: Supply, suply control pin, detect pins, mechanical positions of pins.

- CI supply should be 5V when CI module inserted. If it is not 5V please check CI_PWR_CTRL, this pin should be low.



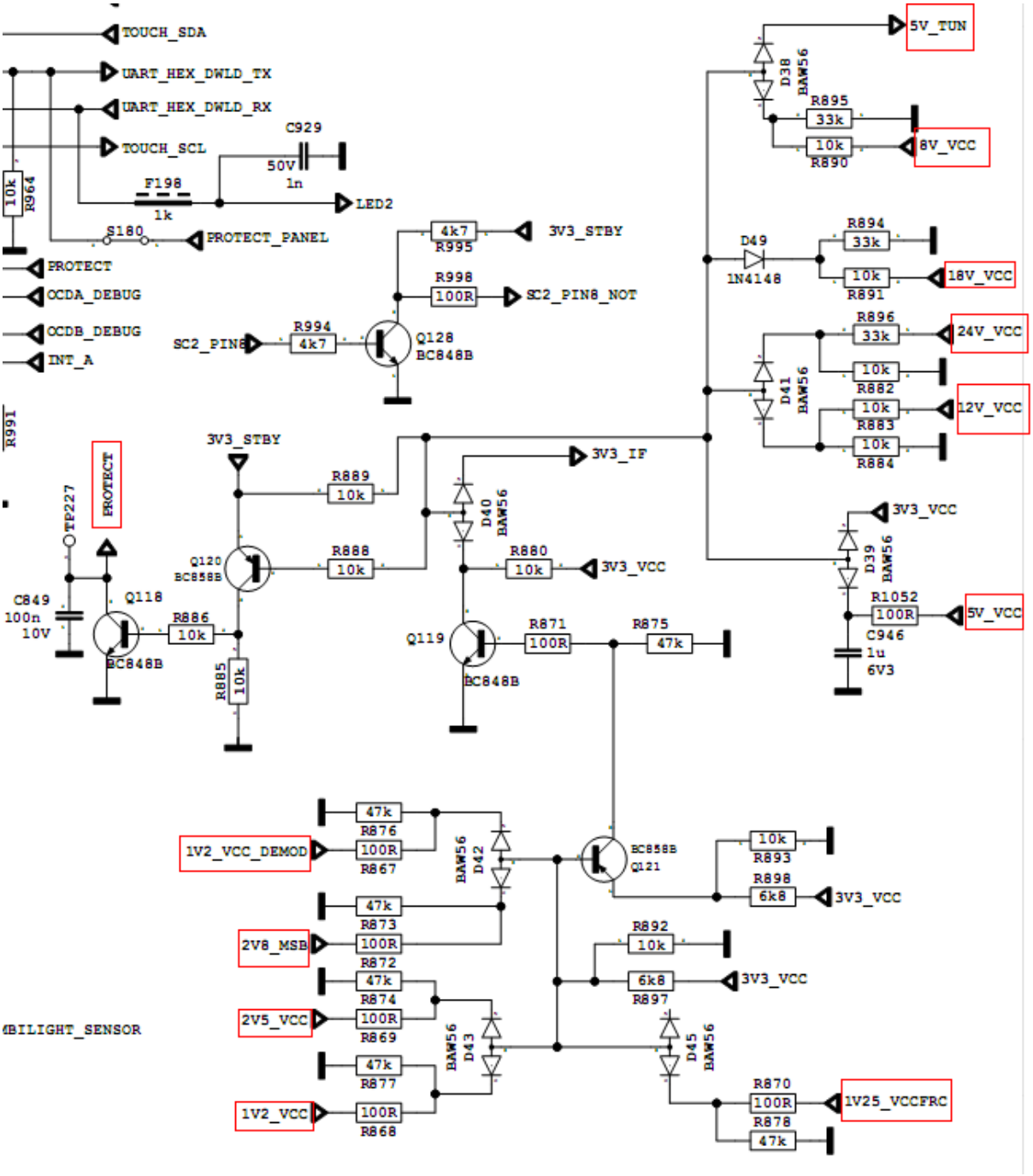
- Please check mechanical position of CI module. Is it inserted properly or not?
- Detect ports should be low. If it is not low please check CI connector pins, CI module pins.



C. Staying in Stand-by Mode

Problem: Staying in stand-by mode, no other operation

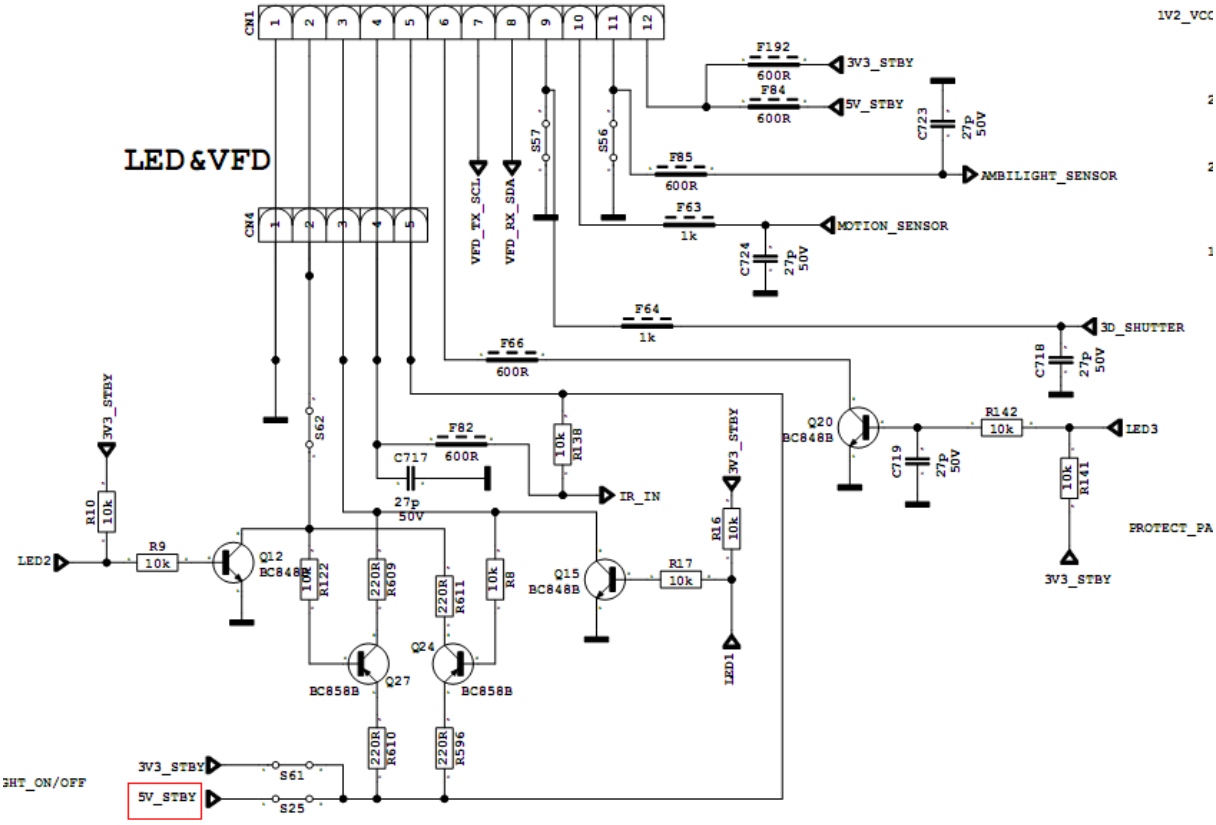
This problem indicates a short on Vcc voltages. Protect pin should be logic high while normal operation. When there is a short circuit protect pin will be logic low. If you detect logic low on protect pin, unplug the TV set and control voltage points with a multimeter to find the shorted voltage to ground.



D. IR Problem

Problem: LED or IR not working

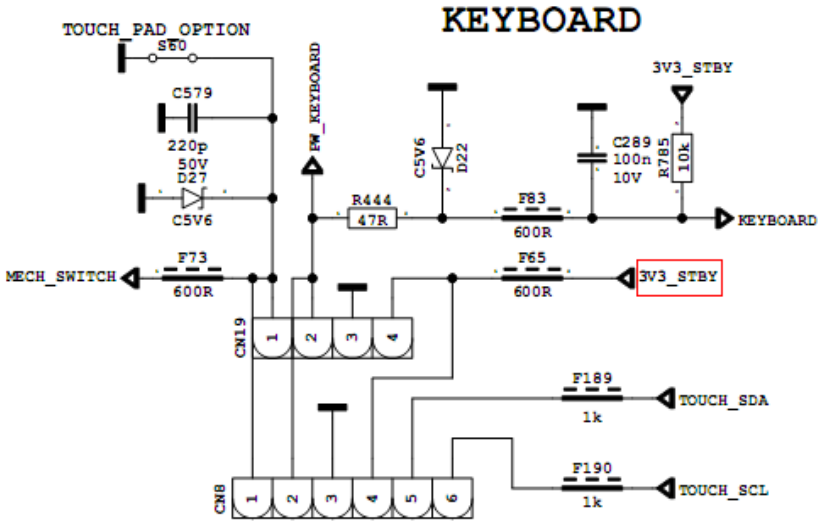
Check LED card supply on MB70 chasis.



E. Keypad Touchpad Problems

Problem: Keypad or Touchpad is not working

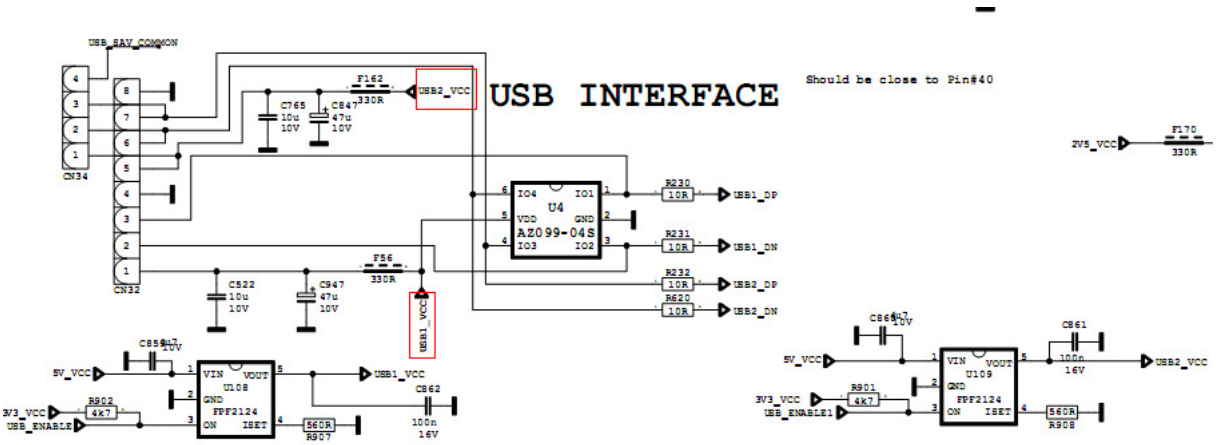
Check keypad supply on MB70.



F. USB Problems

Problem: USB is not working or no USB Detection.

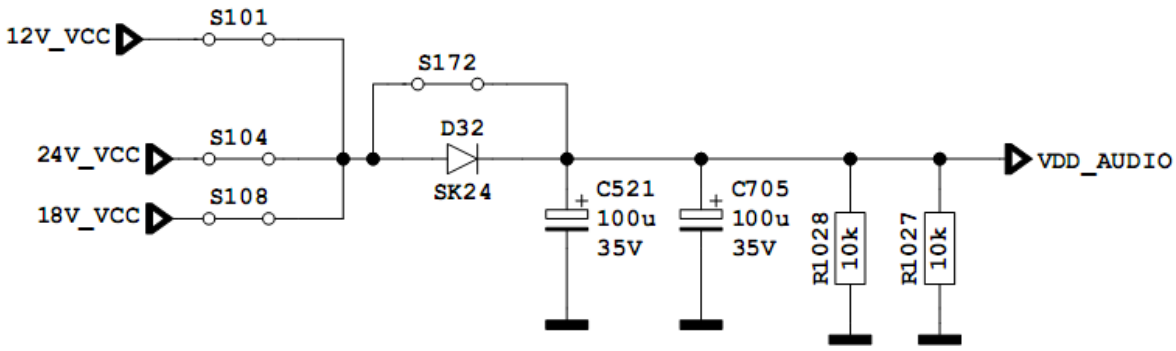
Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.



G. No Sound Problem

Problem: No audio at main TV speaker outputs.

Check supply voltages of VDD_AUDIO, 8V_VCC and 12V_VCC with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3v.



H. Standby On/Off Problem

Problem: Device can not boot, TV hangs in standby mode.

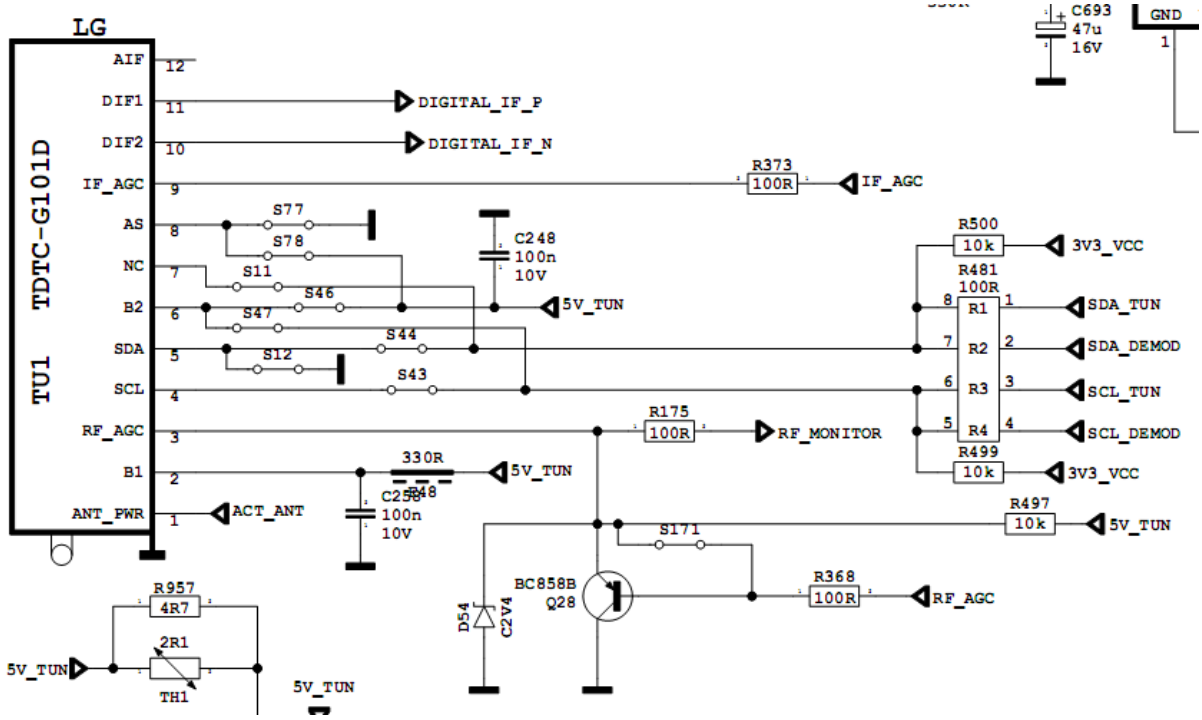
There may be a problem about power supply. Check main supplies with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good

to check SW printouts via Teraterm. These printouts may give a clue about the problem. You can use Scart-1 for terraterm connection.

I. No Signal Problem

Problem: No signal in TV mode.

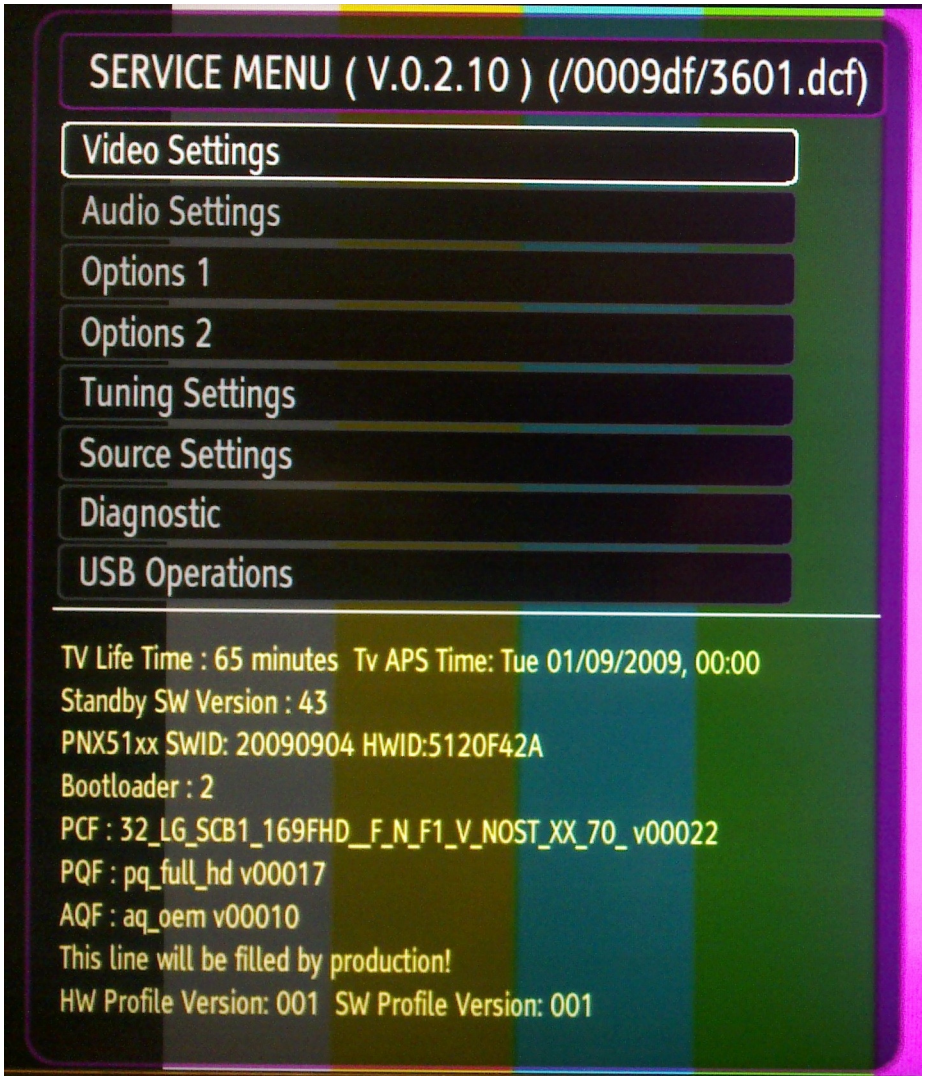
Check tuner supply voltage; 5V_TUN. Check tuner options are correctly set in Service menu. Check AGC voltage at RF_AGC pin of tuner.



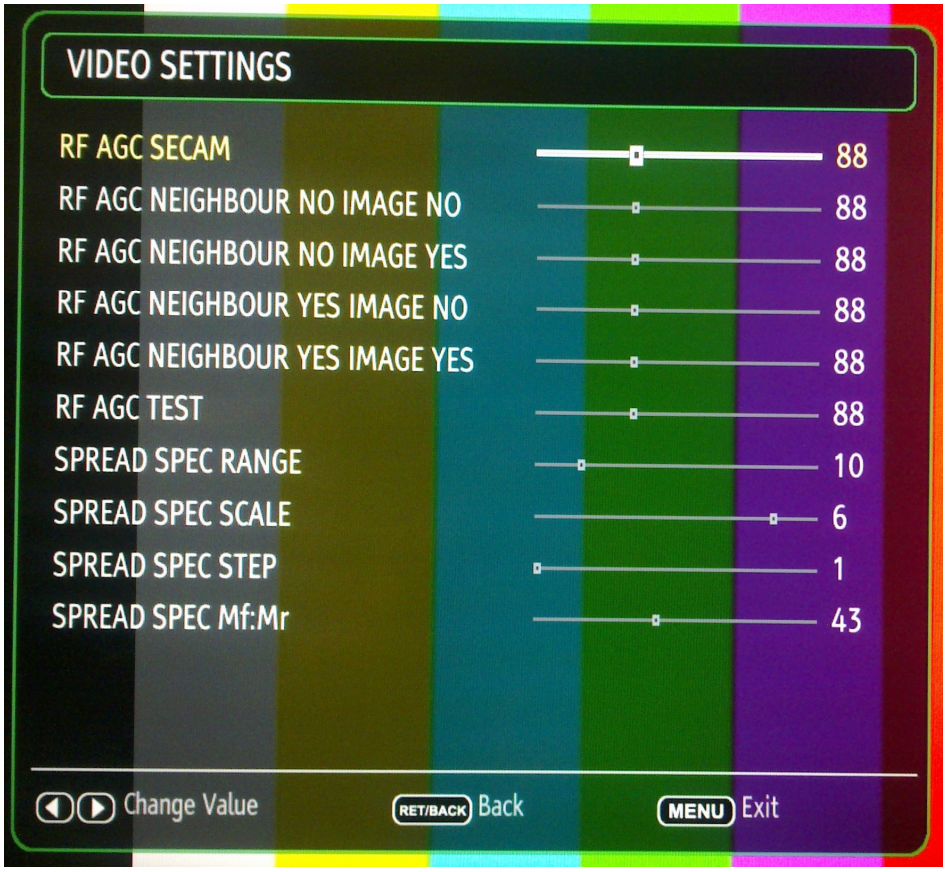
23. Service Menu Settings

In order to reach service menu, First Press **"MENU"** buton, then write "**4725"** by uisng remote controller.

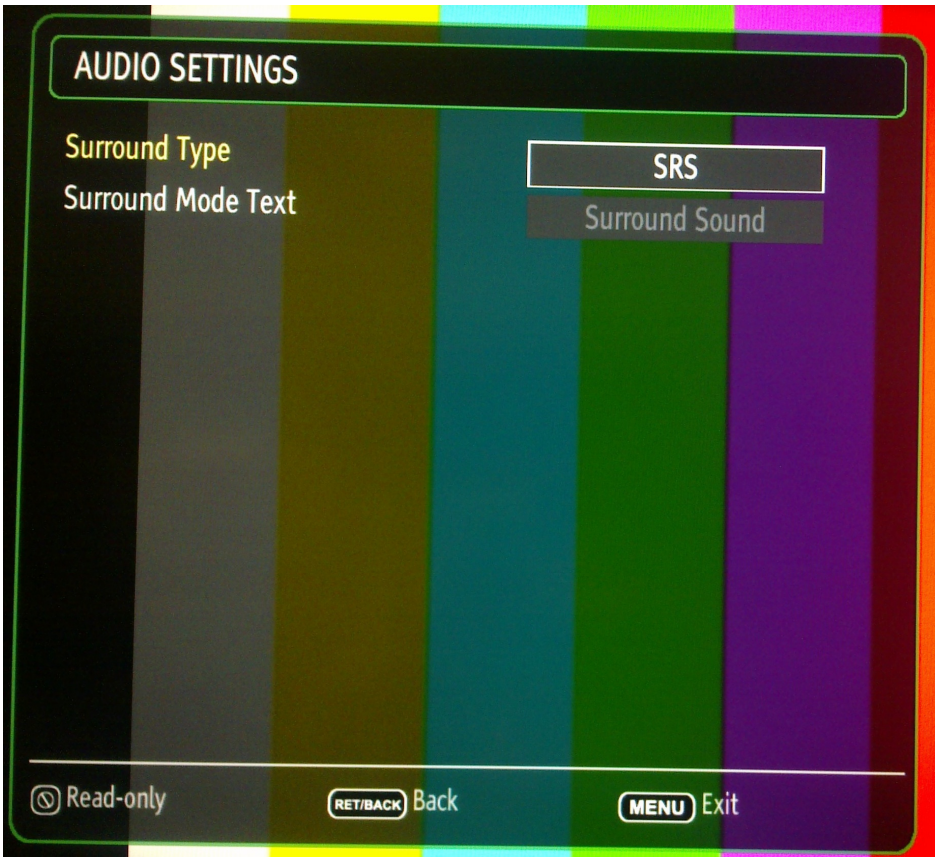
You can see the service menu main screen below. You can check SW releases by using this menu. In addition, you can make changes on video, audio etc. by using video settings, audio settings titles.



Service Menu Main Screen

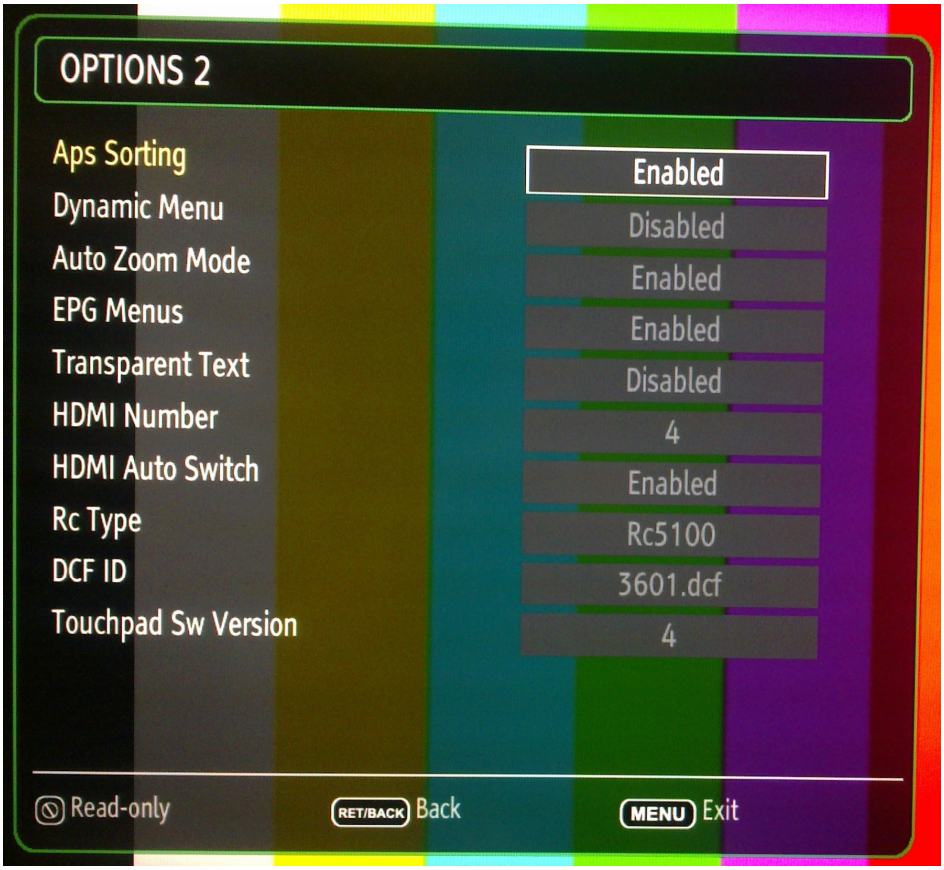


Video Settings

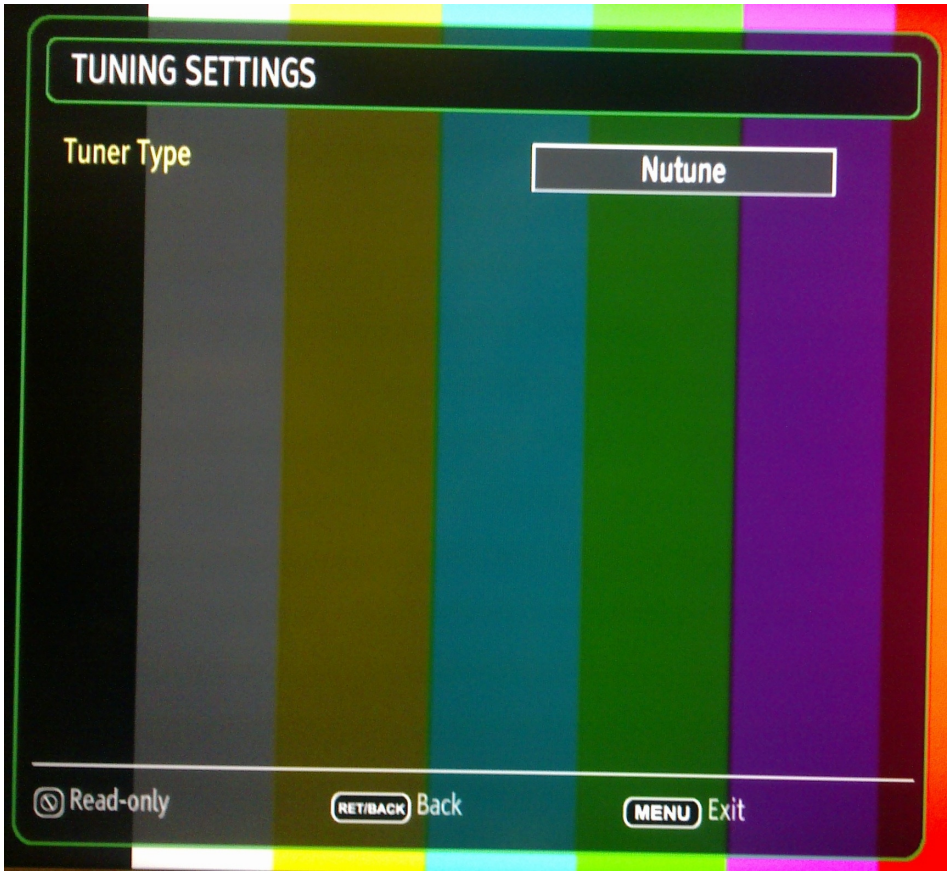


Audio Settings

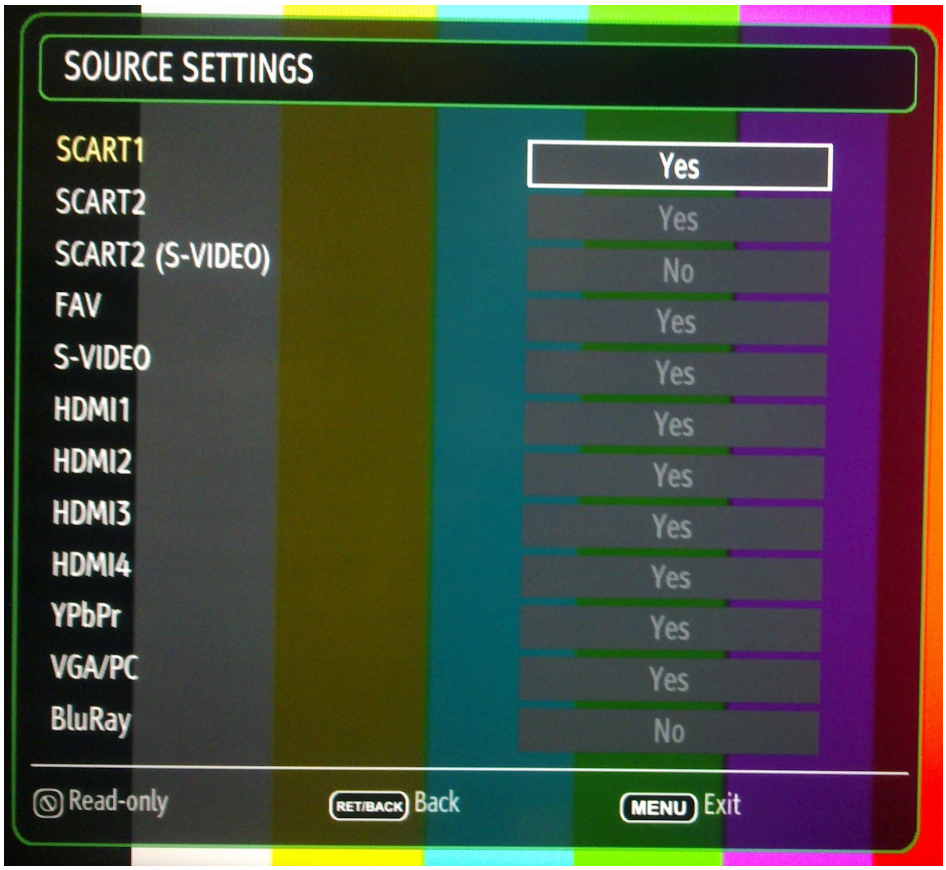
Options-1 Menu



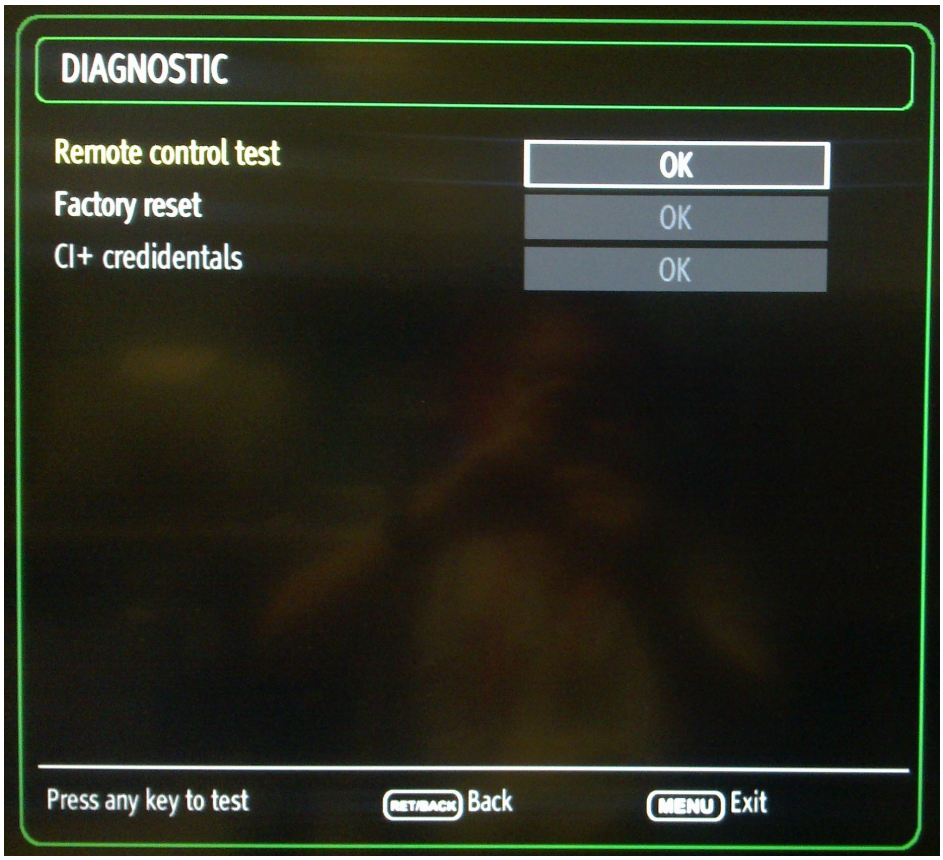
Options-2 Menu



Tuner Settings Menu

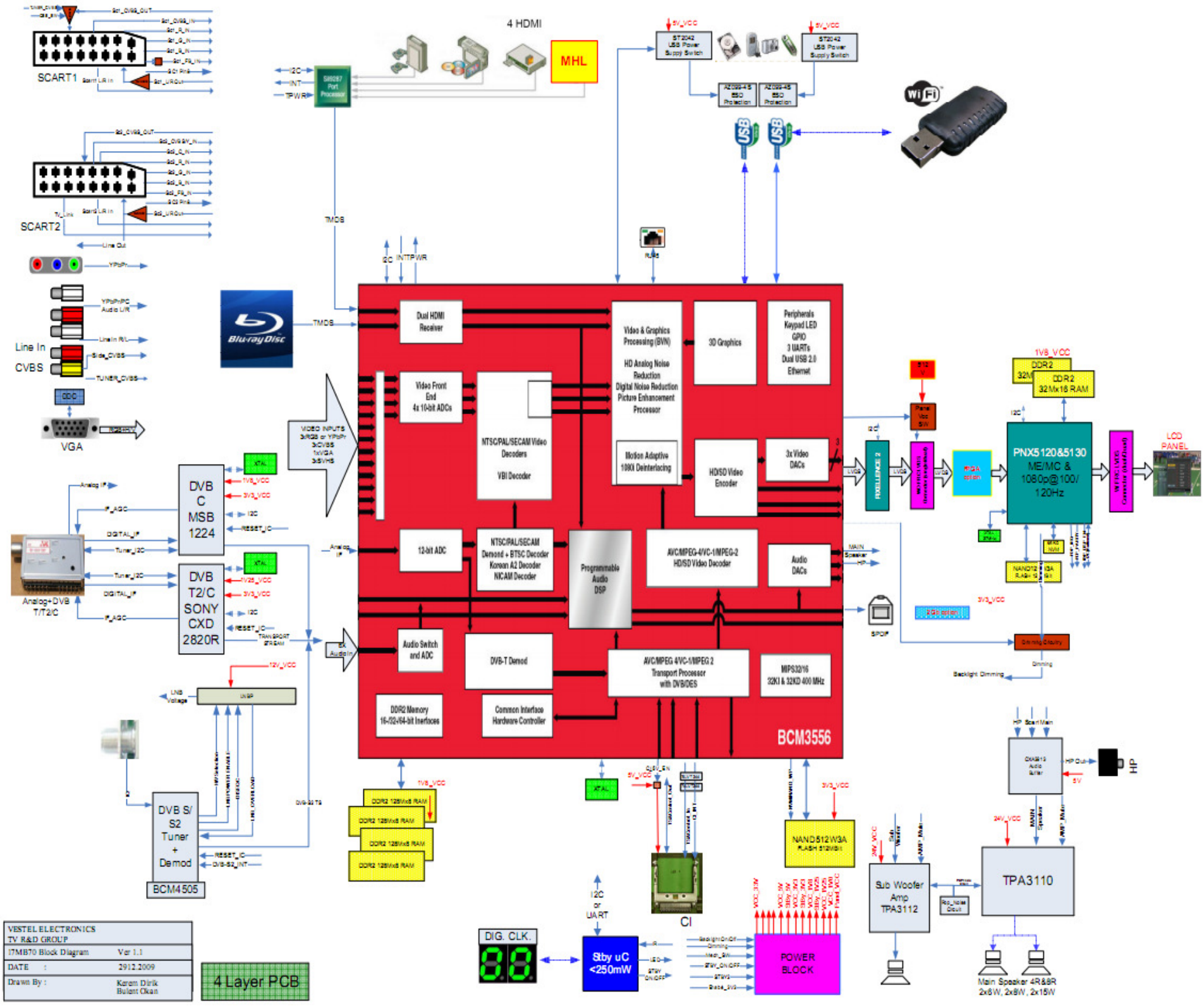


Source Settings Menu



Diagnostic Menu

24. General Block Diagram



VESTEL ELECTRONICS TV R&D GROUP	
17MB70 Block Diagram	Ver 1.1
DATE :	29.12.2009
Drawn By :	Kerem Dirik Bulent Okan

4 Layer PCB